ASHISH GAUTAM, Ph.D.

Postdoctoral Research Associate, Computer Science & Mathematics Division, Oak Ridge National Laboratory

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LinkedIn

PROFESSIONAL SUMMARY

Neuromorphic researcher with over 10 years of combined experience in industry and academia, specializing in the design and development of Spiking Neural Networks (SNNs), their implementation on analog and digital platforms, and large-scale simulation in High Performance Computing (HPC) environments. Demonstrated expertise in building bioinspired hardware-software systems, including ultra-low-power mixed-signal neuromorphic chips, FPGA-based SNN emulators, and HPC-scaled simulation frameworks. Proven success in collaborative research and proposal development as a co-Principal Investigator (co-PI) on DOE, ALCC, and LDRD-funded projects. Passionate about advancing energy-efficient, biologically plausible learning algorithms through innovative hardware-software co-design.

WORK EXPERIENCE

10/2023 – Present
Oak Ridge, TN, USA

Oak Ridge National Laboratory
Postdoctoral Research Associate, CSMD, Data and AI Systems

- Pursuing research in in neuromorphic computing, focusing on Spiking Neural Networks (SNNs), hardware-software co-design, and high-performance computing (HPC).
- Led and supported research proposals. Held leadership roles in organizing conferences and workshops, gave talks, presented posters and papers, mentored students, and participated in program committees and peer-review activities.

11/2021 – 09/2023
Tokyo Japan

The University of Tokyo
Postdoctoral Researcher, Laboratory for Neuromimetic Systems, Institute of Industrial Science.

- Conducted research in the lab of Prof. Takashi Kohno on the design of ultra-low-power biomimetic silicon neuronal networks, leveraging CMOS and FeFET technologies to advance neuromorphic hardware for AI and bio-hybrid applications.
- Led the design and tape-out of multiple mixed-signal neuromorphic chips and contributed to building a comprehensive post-fabrication characterization platform for validating chip functionality and learning performance.

10/2014 – 02/2016
Bengaluru, India

Qualcomm India Pvt. Ltd.
Engineer

- Worked on the layout design and verification of analog, mixed-signal, and RF circuits such as Low Noise Amplifiers (LNAs), mixers, and local oscillators, across advanced technology nodes such as **tsmc 28 nm, tsmc 65 nm, and IBM 180 nm SOI.**
- Managed a team of layout designers and coordinated cross-functional collaboration across global time zones to ensure high-quality deliverables.

05/2012 – 09/2014
Bengaluru, India

Sankalp Semiconductors Pvt/ Ltd.
Engineer II

- Served as a consultant for **Texas Instruments and PMC-Sierra (now Microsemi),** specializing in the layout design and verification of analog, mixed-signal, and RF circuits such as mixers, ADCs/DACs, bandgap references, and digital isolators.

- Worked across process nodes including **tsmc 28 nm, lbc8lv, and 50hpa07**, using tools like **Cadence, Calibre, Assura, K2 Viewer, HFSS, and Assembly Rule Checker**.

🎓 EDUCATION

09/2018 – 11/2021
Tokyo, Japan

Doctor of Philosophy (Ph.D.)
The University of Tokyo
Department of Electrical Engineering & Information Systems
Advisor: Prof. Takashi Kohno
Dissertation Topic: Circuits and an Adaptive Learning Rule for Biologically Plausible Silicon Neuronal Networks

09/2016 – 08/2018
Tokyo, Japan

Master of Science (M.S.)
The University of Tokyo
Department of Electrical Engineering & Information Systems
Advisor: Prof. Takashi Kohno
Dissertation Topic: Low Power Analog Silicon Neuron & Synaptic Circuits

04/2016 – 08/2016
Tokyo, Japan

Research Student
The University of Tokyo
Department of Electrical Engineering & Information Systems

08/2008 – 06/2012
Puducherry, India

Bachelor of Technology (B.Tech)
Pondicherry University, India
Department of Electronics & Instrumentation Engineering

🧠 CORE COMPETENCIES

Neuromorphic Hardware

- *Mixed-signal/Analog VLSI*
  - Led and contributed to the tape-out of multiple chips across advanced technology nodes.
  - Pioneered the first demonstration of on-chip unsupervised spatiotemporal pattern detection using a bio-inspired STDP learning rule.
  - Designed two ultra-low-power conductance-based analog silicon synapse circuits with static power consumption below 2 pW.
- *Digital (FPGA)*
  - Led the development of NeuroCoreX, an open sourced modular FPGA-based SNN emulator written in VHDL with on-chip STDP learning, real-time inference, and built-in visualization capabilities.
- *Novel NVM devices (Beyond CMOS)*
  - Designed an ultra-low power FeFET-based synapse circuit.
  - Proficient in modeling and circuit integration of novel NVM devices such as FeFETs, memristors, and floating-gate transistors.
- *Tools:*
  - Cadence Design Suite, FPGA programming (VHDL), Calibre, Spectre, Verilog-A, Keithley 200A-SCS parameter analyzer to characterize the chip's performance.

HPC-Accelerated Neuromorphic Computing and SNN Co-Design

- *COINFLIPS Project (Frontier Supercomputer):* Integrated0 magnetic tunnel junction (MTJ) model with FORTRAN-based High Energy Physics simulator (PYTHIA) and demonstrated that MTJ based true random number generators RNGs reduced compute time by 40% for application cases such as PYTHIA.
- *Hyper Neuro (Frontier Supercomputer):* Contributed to benchmarking and energy metric validation of the first HPC-scaled SNN simulator called Hyper Neuro (simulating 33 billion neurons).
- *SNN Simulator Co-Design:* Currenly leading the development of an HPC SNN simulation framework for the co-design of biologically plausible, fast, accurate, and energy efficient neuromorphic hardware-compliant SNNs.
- Developed two unsupervised, low-bit synaptic learning rule validated under noisy neural activity patterns.
- *Tools:*
  - Spiking Neural Networks simulation: snnTorch, PyTorch, Python, Numba, Matlab, and Brian2.
  - XPPPAUT to perform bifurcation analysis of the neuron model.

AWARDS

05/2025 **Co-Principal Investigator**
US DOE, ASCR Leadership Computing Challenge (ALCC)
Title: An Exascale Co-Design Framework for Spiking Graph Neural Networks
Award: 420,000 Frontier node hours

12/2024 **Outstanding Postdoc Award**
Computational Science and Mathematics Division, ORNL
- For technical contributions and leadership initiatives across multiple projects and research proposals within the Computational Science and Mathematics Division.

10/2024 **Co-Principal Investigator**
US Department of Energy
Title: ENGAGE: (E)nergy-efficient (N)ovel Al(g)orithms and (A)rchitectures for (G)raph L(e)arning

03/2016 **MEXT Fellowship (April 2016-Sep 2021)**
Government of Japan
Recipient of the MEXT Fellowship awarded by the Government of Japan to pursue graduate studies at The University of Tokyo.

JOURNAL PUBLICATIONS

07/2023 **Gautam, A., and Kohno, T., "Adaptive STDP-based on-chip spike pattern detection"**
Frontiers in Neuroscience (2023)

10/2023 **Gautam, A., and Kohno, T., "Competitive spike pattern detection for neuromorphic systems"**
Journal of Robotics, Networking and Artificial Life (2023)

12/2022 **Gautam, A., and Kohno, T., "Conductance-Based Silicon Synapse Circuit"**
Biomimetics (2022)

09/2021 **Gautam, A., and Kohno, T., "An Adaptive STDP Learning Rule for Neuromorphic Systems"**
Frontiers in Neuroscience (2021)

06/2020 **Gautam, A, and Kohno, T., "Biomimetic Analog Silicon Synaptic Circuit with Tunable Reversal Potential"**
J. Robot. Netw. Artif. Life, 2020

06/2025 **Gautam, A., et al. "NeuroCoreX: An Open-Source FPGA-Based Spiking Neural Network Emulator with On-Chip Learning"**
arXiv preprint arXiv:2506.14138

CONFERENCE PAPERS

06/2025 **Gautam, A., et al. "AI-Powered Knowledge Graphs for Neuromorphic and Energy-Efficient Computing"**
Proceedings of the Great Lakes Symposium on VLSI 2025, June 30 - July 2, 2025, New Orleans, LA, USA.

07/2024 **Gautam, A., et al. "A Suppression-based STDP Rule Resilient to Jitter Noise in Spike Patterns for Neuromorphic Computing"**
The 2024 International Conference on Neuromorphic Systems (ICONS), July 30-Aug 2, 2024, George Mason University, Arlington, VA, USA.

02/2023 **Gautam, A., and Kohno, T., "Adaptive STDP learning with lateral inhibition for neuromorphic systems"**
The 2023 International Conference on Artificial Life and Robotics (ICAROB2023), Feb. 20th-23rd, Beppu, Oita, Japan.

02/2020 **Gautam, A., and Kohno, T., "Experimental results of a biomimetic analog silicon synaptic circuit"**
The 2020 International Conference on Artificial Life and Robotics (ICAROB2020), Feb. 20th-23rd, Beppu, Oita, Japan.

02/2018 **Gautam, A., and Kohno, T., "A low power silicon synapse with tunable reversal potential"**
The 2018 International Conference on Artificial Life and Robotics (ICAROB2018), Feb. 1st-4th, Beppu, Oita, Japan

ABSTRACTS AND INVITED TALKS

09/2024 **Gautam, A., "Optimizing Mixed-Signal Neuromorphic Circuits: Bridging Computational Gaps"**
2024 Neuromorphic Computing for Science Workshop Sponsored by the U.S. Department of Energy, Office of Advanced Scientific Computing Research (ASCR) September 12-13, 2024 Bethesda, MD

07/2024 **Gautam, A., et al. "Beyond Pair-based STDP Learning Rules for Mixed-signal Neuromorphic Chips"**
2024 SIAM Annual Meeting (AN24), July 8–12 , 2024 Spokane, Washington, U.S.

03/2024 **Gautam, A., et al. "Silicon Neuronal Networks for Brainmorphic Computing"**
The 21st Annual World Congress of Society for Brain Mapping and Therapeutics 2024, March 14th to 17th, 2024 at the Los Angeles Convention Center, Los Angeles, California.

03/2024 **Gautam, A., et al. "On-chip spike pattern classification for neuromorphic systems"**
2024 APS March Meeting, March 4–8, 2024; Minneapolis & Virtual

INTELLECTUAL PROPERTY

Open-Source Software Copyright: NeuroCoreX, an FPGA-based neuromorphic processor designed and implemented using VHDL. GitHub: NeuroCoreX.
NeuroCoreX is an open-source codebase that enables the implementation of brain-inspired, energy-efficient neuromorphic computing models on FPGA hardware. Designed to support real-time learning, all-to-all neural connectivity, and flexible network architectures, NeuroCoreX offers a hands-on, accessible platform for exploring biologically inspired models of neural computation. It empowers researchers, students, and developers to implement and experiment with adaptive systems—bringing the power of neuromorphic computing to a broader community through a low-cost, scalable, and reconfigurable framework.

SYNERGISTIC ACTIVITIES

07/2025 **Organizing and Program Committee member for the IEEE/ACM International Conference on Neuromorphic Systems (ICONS) 2025.**

07/2025 **Session chair for two sessions at Great Lakes Symposium on VLSI (GLSVLSI) 2025.**

05/2025 **Program committee member at IEEE COINS: IEEE International Conference on Omni-layer Intelligent systems 2025.**

03/2025 **Program committee member at Neuro Inspired Computational Elements Conference (NICE) 2025.**

01/2025 **Participated in the Bangalore Neuromorphic Engineering Workshop (BNEW) 2025**

12/2024 **Program committee member at IEEE International Conference on Rebooting Computing (ICRC) 2024.**

09/2024 **Program committee member at The 2024 VLSI Design & Test Symposium (VDAT-2024)**

09/2024 **Contributed position paper at 2024 Neuromorphic Computing for Science Workshop Sponsored by the U.S. Department of Energy, Office of Advanced Scientific Computing Research (ASCR)**

07/2024 **Organizing and Program Committee member for the IEEE/ACM International Conference on Neuromorphic Systems (ICONS) 2024.**

12/2023 **Program committee member and oral presentation Judge at IEEE International Conference on Rebooting Computing (ICRC) 2023.**

Reviewer
1. Frontiers in Neuroscience: Neuromorphic Computing.
2. IEEE Transactions on Neural Networks and Learning Systems (IEEETNLS).
3. IEEE Transactions on Very Large Scale Integration (VLSI) Systems

LANGUAGES

English	●●●●●	Hindi	●●●●●
Tamil	●●○○○	Nepali	●●○○○
Japanese	●●○○○		