

Computer Memory Cell Design Based on Coupled Josephson Junction Arrays

Disclosure Number

201603629

Technology Summary

Memory design is considered to be a major bottleneck for exascale computing. The main goal in memory design is reducing access time and access power. In this invention we present a design of cryogenic memory circuit and demonstrate principles of operation of the proposed circuit by implementing mathematical and computational models. In the proposed design, Write and Read operations are implemented on the same circuit to conserve area and decrease latency. Pulse energies required for implementation of memory operation may be very low (in the range of 10-19 J) and delay times between the application of the pulse and circuit response may be lower than 100 ps.

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