Cryogenic Memory Cell Design Based on Small Coupled Arrays of Josephson Junctions

**Achievement:** Proposed cryogenic memory cell design that has a potential to substantially outperform the existing memory cells, achieve much faster access times and lower access and dissipation energies, and reduce the size of the memory cell.

**Significance and Impact:** Designing fast, energy efficient and small size memory circuit is considered one of the major bottlenecks in modern computing. Such memories could profoundly advance development and performance of exascale, quantum, and cryogenic computing.

**Research Details:**
- Memory cell design was presented and demonstrated on an example of small coupled array of Josephson junctions.
- All the basic memory cell operations (Write, Read, and Reset) are implemented on the same circuit.
- Access times and access energies for basic memory operations (Write, Read, and Reset) were calculated and driving current and trigger pulse amplitudes were optimized for better memory cell performance.

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Overview:
We demonstrated a paradigm for cryogenic memory operation and presented a specific example of a circuit that consists of three inductively coupled Josephson junctions. We have employed Josephson junction parameter values that are consistent with the current state-of-the-art Josephson junction fabrication capabilities. For parameter values presented in the paper, memory cell access times are of the order of 10 - 100 ps while access energies are of the order of 0.1 – 5 aJ. The principles of memory cell design and operation described in our papers can in principle be implemented on other Josephson junction based circuits as well.