KAZI ASIFUZZAMAN, Ph.D

asifuzzamank@ornl.gov, 865 341 0320

HIGHLIGHTS

Working as a Research Scientist at Oak Ridge National Laboratory (ORNL), *USA*
PhD in Computer Architecture from Universitat Politecnica de Catalunya, *Spain*
Master's in Electronic Design (SoC & Embedded) from Lund University, *Sweden*
Worked one year on IT systems at Shimizu Densetsu Kogyo Co. Ltd, *Japan*
Bachelor's degree in Computer Engineering from North South University, *Bangladesh*

EDUCATION

PhD in Computer Architecture
[1]Universitat Politecnica de Catalunya (UPC), Spain - 2019
Area of Study: Computer Architecture, HPC, Memory Systems

Master of Science in Electronic Design
[2]Lund University (LU), Sweden - 2013
Area of Study: Embedded Systems, IC Design, DSP, A/D Converter, IPR

Bachelor of Science in Computer Engineering
North South University (NSU), Bangladesh - 2008
Area of Study: Programming, Data Structures, Engineering Mathematics,
Physics, Digital Logic Design, Computer Organization and Architecture

AREA OF EXPERTISE

- System simulation
- x86, ARM architectures
- Performance analysis
- Memory timing analysis
- Novel memory systems
- Microelectronics
- Real-time systems
- Neuromorphic Computing
- GPGPU systems

EXPERIENCE

Oak Ridge National Laboratory, USA

Research Scientist (10/2021 - Present)
Working as a R& D Associate Staff at the Advanced Computing Research Section of the Computing and Computational Sciences Directorate.

Barcelona Supercomputing Center, Spain

Post-doctoral Researcher (08/2019 - 10/2021)

- Analyzed performance and predictability aspects of High Bandwidth Memory.
- Investigated and mitigated source of contention in GPGPU global memory.
- Contributed to develop a software architecture for safe and secure OTA updates.

Doctoral Researcher (05/2014 - 07/2019)

- Quantified performance & WCET implications of MRAM for real-time systems.
- Compared performance on ARM platforms with DDR4 and HBM (ExaNoDe).
- Contributed in a project investigating the impact of processing in memory.
- Analyzed STT-MRAM timing parameters from existing studies and patents.
- Performed HPC system simulations with validated simulation infrastructures.
- Investigated system performance impact of a slower NVM Memory for HPC.

---

[1]UPC ranked 85th among top universities worldwide for Engineering and Technology, QS Ranking 2019.
[2]LU ranked 82nd among top universities worldwide for Engineering and Technology, QS Ranking 2013.

Shimizu Densetsu Kogyo Co. Ltd (SEAVAC), Japan   **SEAVAC**
International Trainee (01/2008-01/2009)
Simultaneously contributed in multiple R&D projects of the company. Developed several applications as per company need, automated business contact registration system using native database design, explored several server configurations and deployed WebELS e-meeting server to provide online meeting services.

THESES

[**PhD**] **Kazi Asifuzzaman**. *"Evaluation of STT-MRAM main memory for HPC and real-time systems"*, Universitat Politecnica de Catalunya, 2019.

[**Masters**] **Kazi Asifuzzaman**. *"Design and Implementation of an Embedded Vision System for Industrial Robots"*, Lund University Publications, Series: LU-CS-EX 2013-27, ISSN: 1650-2884, 2013.

REVIEWER/TPC

- *Associate Editor*, IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), 2023
- *TPC Member*, International Conference on Computer-Aided Design (ICCAD'23)
- *TPC Member*, IEEE Computer Society Annual Symposium on VLSI (ISVLSI'23)
- *RC Member*, Annual Modeling and Simulation Conference (ANNSIM'23)
- *TPC Member*, International Conference on Computer-Aided Design (ICCAD'22)
- *TPC Member*, IEEE International Conference on Computer Design (ICCD'22)
- *Reviewer*, Memories - Materials, Devices, Circuits and Systems Journal, 2022
- *Reviewer*, Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD'21).

ACADEMIC COMMITTEE

Universitat Politectnica de Catalunya (UPC) Served as pre-dissertation tribunal member evaluating PhD thesis of David Trilla Rodriguez; titled: *Non-functional considerations of time-randomized processor architectures*, 2020.

ADVANCED COURSES

International Summer School on Advanced Computer Architecture and Compilation for High Performance and Embedded Systems, Italy, 2018
- Memory systems and Memory-Centric Computing Systems *by Onur Mutlu*
- Distributed Memory Programming and Algorithms *by Johannes Langguth*
- GPU Architectures: From Basic to Advanced Concepts *by Adwait Jog*
- Architectural Support for Virtual Memory *by Abhishek Bhattacharjee*

International Summer School on Advanced Computer Architecture and Compilation for High Performance and Embedded Systems, Italy, 2017
- Advanced Topics in Memory Systems *by Moinuddin Qureshi*
- Reconfigurable Hardware, Tools and Applications *by Michael Hubner*
- High-Performance On-Chip Interconnects for Emerging SoCs *by Tushar Krishna*
- Design and Analysis of Time Critical Systems *by Jan Reineke*

Universitat Politecnica de Catalunya (UPC), Spain
- Modern Memory Systems *by Bruce Jacob*, 2017
- Issues in Computer Architecture and Microarchitecture for Future Computing Machines *by Yale Patt*, 2015

TRAINNING

- **Public Speaking**, 11 December 2018, Barcelona Supercomputing Center, Spain.
- **Project Management for Researchers**, 16 - 22 October 2018 at Barcelona Supercomputing Center, Spain.

PUBLICATIONS

[14] Md Arif Iqbal, Srinivas Rahul Sapireddy, Sumanth Dasari, **Kazi Asifuzzaman**, Mostafizur Rahman *"A review of crosstalk polymorphic circuits and their scalability"*. Memories - Materials, Devices, Circuits and Systems, Vol 7, ISSN 2773-0646, 2023.

[13] Shamiul Alam, **Kazi Asifuzzaman**, Ahmedullah Aziz *"A Novel Scalable Array Design for III-V Compound Semiconductor-based Non-volatile Memory (UltraRAM) with Separate Read-Write Paths"*. Accepted at the 24th International Symposium on Quality Electronic Design (ISQED), 2023.

[12] **Kazi Asifuzzaman**, Narasinga Rao Miniskar, Aaron R Young, Frank Liu, Jeffrey S Vetter *"A survey on processing-in-memory techniques: Advances and challenges"*. Memories - Materials, Devices, Circuits and Systems, Vol 4, 2023.

[11] **Kazi Asifuzzaman**, Monil Mohammad Alaul Haque Monil, Frank Liu, Jeffrey S Vetter *"Evaluating HPC Kernels for Processing in Memory"*. In Proceedings of the Fifth International Symposium on Memory Systems (MEMSYS), USA, 2022.

[10] **Kazi Asifuzzaman**, Narasinga Rao Miniskar, Aaron R Young, Frank Liu, Jeffrey S Vetter *"Heterogeneous Memory System Framework for HPC"*. ASCR Workshop on the Management and Storage of Scientific Data, US Department of Energy, Office of Scientific and Technical Information 2022.

[9] **Kazi Asifuzzaman**, Rommel Sanchez Verdejo, and Petar Radojkovic. *"Performance and Power Estimation of STT-MRAM Main Memory with Reliable System-level Simulation"*. Transactions on Embedded Computing Systems (TECS), 2022.

[8] **Kazi Asifuzzaman**, Mohamed AbuElAla, Mohamed Hassan and Francisco J Cazorla. *"Demystifying the Characteristics of High Bandwidth Memory for Real-Time Systems"*. International Conference on Computer-Aided Design (ICCAD), 2021.

[7] Alvaro Jover-Alvarez, Alejandro J. Calderon, Ivan Rodriguez, Leonidas Kosmidis, **Kazi Asifuzzaman**, Patrick Uven, Kim Gruttner, Tomaso Poggi and Irune Agirre. *"The UP2DATE Baseline Research Platforms"*. In proceedings of the Design Automation and Test in Europe (DATE) Conference, 2021.

[6] **Kazi Asifuzzaman**, Mikel Fernandez, Petar Radojković, Jaume Abella and Francisco J. Cazorla. *"STT-MRAM for Real-Time Embedded Systems: Performance and WCET Implications"*. In Proceedings of the Fifth International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2019.

[5] Milan Radulovic, **Kazi Asifuzzaman**, Darko Zivanovic, Nikola Rajovic, Guillaume Colin de Verdiere, Dirk Pleiter, Manolis Marazakis, Nikolaos Kallimanis, Paul Carpenter, Petar Radojkovic and Eduard Ayguade, *"Mainstream vs. Emerging HPC: Metrics, Trade-offs and Lessons Learned"*. International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), France, 2018.

[4] Rommel S. Verdejo, **Kazi Asifuzzaman**, Milan Radulovic, Petar Radojkovic, Eduard Ayguade and Bruce Jacob. *"Main Memory Latency Simulation: The Missing Link"*. International Symposium on Memory Systems (MEMSYS), USA, 2018.

[3] Milan Radulovic, **Kazi Asifuzzaman**, Paul Carpenter, Petar Radojkovic and Eduard Ayguade. *"HPC benchmarking: scaling right and looking beyond the average"*. Euro-Par: Parallel Processing, 2018.

[2] **Kazi Asifuzzaman**, Rommel Sanchez Verdejo and Petar Radojkovic. *"Enabling a Reliable STT-MRAM Main Memory Simulation"*. International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2017.

[1] **Kazi Asifuzzaman**, Milan Pavlovic, Milan Radulovic, David Zaragoza, Ohseong Kwon, Kyung-Chang Ryoo and Petar Radojkovic. *"Performance Impact of a Slower Main Memory: A case study of STT-MRAM in HPC"*. International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2016.