KAZI ASIFUZZAMAN, PhD

asifuzzamank@ornl.gov, 865 341 0320

SUMMARY

Working as a Research Scientist at Oak Ridge National Laboratory (ORNL), *USA*
PhD in Computer Architecture from Universitat Politecnica de Catalunya, *Spain*
Master's in Electronic Design (SoC & Embedded) from Lund University, *Sweden*
Worked one year on IT systems at Shimizu Densetsu Kogyo Co. Ltd, *Japan*
Bachelor's degree in Computer Engineering from North South University, *Bangladesh*

EDUCATION

PhD in Computer Architecture
[1]Universitat Politecnica de Catalunya (UPC), Spain - 2019
Area of Study: Computer Architecture, HPC, Memory Systems

Master of Science in Electronic Design
[2]Lund University (LU), Sweden - 2013
Area of Study: Embedded Systems, IC Design, DSP, A/D Converter, IPR

Bachelor of Science in Computer Engineering
North South University (NSU), Bangladesh - 2008
Area of Study: Programming, Data Structures, Engineering Mathematics, Physics, Digital Logic Design, Computer Organization and Architecture

AREA OF EXPERTISE

- System simulation
- Memory timing analysis
- Real-time systems
- x86, ARM architectures
- Novel memory systems
- Predictability analysis
- Performance analysis
- Contention analysis
- GPGPU systems

EXPERIENCE

Research Scientist
Oak Ridge National Laboratory, USA (10/2021 - Present)
Working as a Research Associate Staff at the Advanced Computing Research Section of the Computing and Computational Sciences Directorate.

Postdoctoral Researcher
Barcelona Supercomputing Center, Spain (08/2019 - 10/2021)

HBM Analyzed performance and predictability aspects of High Bandwidth Memory (HBM) in high performance real-time systems.

GPGPU Investigated the source of contention in GPGPU global memory and developing techniques to mitigate them.

Up2Date Worked as a part of the EU funded Up2Date project targeting to develop a new software architecture for safe and secure Over-the-Air software updates for Mixed-Criticality Cyber-Physical Systems.

Doctoral Researcher
Barcelona Supercomputing Center, Spain (05/2014 - 07/2019)

HPC Performance Investigated system performance impact of a slower non-volatile (NVM) main memory on production HPC workloads. Funded by *Samsung*.

MRAM for Real-time Quantified performance and WCET implications of STT-MRAM for real-time systems with SocLibSim and DRAMSim2 simulator.

ExaNoDe Compared performance on ARM platforms with DDR4 and HBM as a part of the EU funded ExaNoDe project targeting Exascale computing.

[1]UPC ranked 85th among top universities worldwide for Engineering and Technology, QS Ranking 2019.
[2]LU ranked 82nd among top universities worldwide for Engineering and Technology, QS Ranking 2013.

International Trainee – Research Intern SEAVAC

Shimizu Densetsu Kogyo Co. Ltd (SEAVAC), Japan (01/2008-01/2009)
Simultaneously contributed in multiple R&D projects of the company. Developed several applications as per company need, automated business contact registration system using native database design, explored several server configurations and deployed WebELS e-meeting server to provide online meeting services.

PUBLICATIONS

[9] **Kazi Asifuzzaman**, Rommel Sanchez Verdejo, and Petar Radojkovic. *"Performance and Power Estimation of STT-MRAM Main Memory with Reliable System-level Simulation"*. Accepted to Transactions on Embedded Computing Systems (ACM-TECS), 2022.

[8] **Kazi Asifuzzaman**, Mohamed AbuElAla, Mohamed Hassan and Francisco J Cazorla. *"Demystifying the Characteristics of High Bandwidth Memory for Real-Time Systems"*. Accepted to International Conference on Computer-Aided Design (ICCAD), 2021.

[7] Alvaro Jover-Alvarez, Alejandro J. Calderon, Ivan Rodriguez, Leonidas Kosmidis, **Kazi Asifuzzaman**, Patrick Uven, Kim Gruttner, Tomaso Poggi and Irune Agirre. *"The UP2DATE Baseline Research Platforms"*. In proceedings of the Design Automation and Test in Europe (DATE) Conference, 2021.

[6] **Kazi Asifuzzaman**, Mikel Fernandez, Petar Radojković, Jaume Abella and Francisco J. Cazorla. *"STT-MRAM for Real-Time Embedded Systems: Performance and WCET Implications"*. In Proceedings of the Fifth International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2019.

[5] Milan Radulovic, **Kazi Asifuzzaman**, Darko Zivanovic, Nikola Rajovic, Guillaume Colin de Verdiere, Dirk Pleiter, Manolis Marazakis, Nikolaos Kallimanis, Paul Carpenter, Petar Radojkovic and Eduard Ayguade, *"Mainstream vs. Emerging HPC: Metrics, Trade-offs and Lessons Learned"*. In proceedings of the 30th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Lyon, France, 2018.

[4] Rommel Sanchez Verdejo, **Kazi Asifuzzaman**, Milan Radulovic, Petar Radojkovic, Eduard Ayguade and Bruce Jacob. *"Main Memory Latency Simulation: The Missing Link"*. In Proceedings of the fourth International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2018.

[3] Milan Radulovic, **Kazi Asifuzzaman**, Paul Carpenter, Petar Radojkovic and Eduard Ayguade. *"HPC benchmarking: scaling right and looking beyond the average"*. Euro-Par: Parallel Processing, 2018.

[2] **Kazi Asifuzzaman**, Rommel Sanchez Verdejo and Petar Radojkovic. *"Enabling a Reliable STT-MRAM Main Memory Simulation"*. In Proceedings of the Third International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2017.

[1] **Kazi Asifuzzaman**, Milan Pavlovic, Milan Radulovic, David Zaragoza, Ohseong Kwon, Kyung-Chang Ryoo and Petar Radojkovic. *"Performance Impact of a Slower Main Memory: A case study of STT-MRAM in HPC"*. In Proceedings of the Second International Symposium on Memory Systems (MEMSYS) Washington DC, USA, 2016.

THESES

[**PhD**] **Kazi Asifuzzaman**. *"Evaluation of STT-MRAM main memory for HPC and real-time systems"*, Universitat Politecnica de Catalunya, 2019.

[**Masters**] **Kazi Asifuzzaman**. *"Design and Implementation of an Embedded Vision System for Industrial Robots"*, Lund University Publications, Series: LU-CS-EX 2013-27, ISSN: 1650-2884, 2013.

REVIEWER

- Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2021

ACADEMIC COMMITTEE

- **Universitat Politectnica de Catalunya (UPC)** Served as pre-dissertation tribunal member evaluating PhD thesis of David Trilla Rodriguez; titled: *Non-functional considerations of time-randomized processor architectures*, 2020.

SCIENTIFIC SOCIETIES

- **Affiliated Member**, European Network on High-performance Embedded Architecture and Compilation (HiPEAC).
- **Member**, Institute of Electrical and Electronics Engineers (IEEE).
  - IEEE Council on Electronic Design Automation
  - IEEE Computer Society Technical Community on Computer Architecture
  - IEEE Computer Society Technical Community on Microprogramming and Microarchitecture
  - IEEE Computer Society Technical Community on Parallel Processing
  - IEEE Computer Society Technical Community on Real-Time Systems

ADVANCED COURSES

International Summer School on Advanced Computer Architecture and Compilation for High Performance and Embedded Systems, Italy, 2018

- Memory systems and Memory-Centric Computing Systems *by Onur Mutlu*
- Distributed Memory Programming and Algorithms *by Johannes Langguth*
- GPU Architectures: From Basic to Advanced Concepts *by Adwait Jog*
- Architectural Support for Virtual Memory *by Abhishek Bhattacharjee*

International Summer School on Advanced Computer Architecture and Compilation for High Performance and Embedded Systems, Italy, 2017

- Advanced Topics in Memory Systems *by Moinuddin Qureshi*
- Reconfigurable Hardware, Tools and Applications *by Michael Hubner*
- High-Performance On-Chip Interconnects for Emerging SoCs *by Tushar Krishna*
- Design and Analysis of Time Critical Systems *by Jan Reineke*

Universitat Politecnica de Catalunya (UPC), Spain

- Modern Memory Systems *by Bruce Jacob*, 2017
- Issues in Computer Architecture and Microarchitecture for Future Computing Machines *by Yale Patt*, 2015

IC PROJECT

32 Bit MIPS Microprocessor Design & Verification
Area: Digital ASIC Design / Computer Architecture (Lund University, Sweden)
Designed and implemented a 32 Bit MIPS microprocessor architecture using 130nm process in standard ASIC flow. The processor has reduced instruction set architecture and capable of executing programs written in assembly language. The design process included Behavioral Specification, RTL design, Synthesis, Place & Route (Floor planning, Power Planning, Power Routing, Signal Routing) and verification.
Tools Used:VHDL, Model Sim, Design Vision, SocEncounter, Logic Analyzer

TRAINNING

- **Public Speaking**, 11 December 2018, at Barcelona Supercomputing Center, Spain.
- **Project Management for Researchers**, 16 - 22 October 2018 at Barcelona Supercomputing Center, Spain.
- **Oracle 9i: Database Administration Fundamentals-I**, 3 - 17 September 2007 at IBCS-PRIMAX, Dhaka, Bangladesh.
- **International Workshop on Environment and Disaster Management**, 19 - 23 August 2006 at Hotel Equatorial, Melaka, Malaysia. Organized by World Youth Foundation (WYF).