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**CRADA Final Report
for
CRADA Number 94-0263**

**PROXIMITY SENSOR
SYSTEM DEVELOPMENT**

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Abstract

Lockheed Martin Energy Research Corporation (LMERC) and Merritt Systems, Inc. (MSI) entered into a Cooperative Research and Development Agreement (CRADA) for the development and demonstration of a compact, modular proximity sensing system suitable for application to a wide class of manipulator systems operated in support of environmental restoration and waste management activities. In teleoperated modes, proximity sensing provides the manipulator operator continuous information regarding the proximity of the manipulator to objects in the workspace. In teleoperated and robotic modes, proximity sensing provides added safety through the implementation of active whole arm collision avoidance capabilities. Oak Ridge National Laboratory (ORNL), managed by LMERC for the United States Department of Energy (DOE), has developed an application specific integrated circuit (ASIC) design for the electronics required to support a modular whole arm proximity sensing system based on the use of capacitive sensors developed at Sandia National Laboratories. The use of ASIC technology greatly reduces the size of the electronics required to support the selected sensor types allowing deployment of many small sensor nodes over a large area of the manipulator surface to provide maximum sensor coverage. The ASIC design also provides a communication interface to support sensor commands from and sensor data transmission to a distributed processing system which allows modular implementation and operation of the sensor system. MSI is a commercial small business specializing in proximity sensing systems based upon infrared and acoustic sensors.

Objectives

The purpose of this CRADA was to combine a modified ORNL ASIC design and the MSI sensor hardware to provide a commercially available and supported compact modular proximity system marketed by MSI. To develop this system the following had to be achieved: (1) complete sensor design (MSI), (2) define communication interface (MSI/ORNL), (3) modify ASIC design

(ORNL), (4) component fabrication (MSI/ORNL), and (5) complete integration and testing (MSI/ORNL).

All of the above objectives were met to finalize this CRADA. Final status of the tasks is as follows:

Sensor Electronics Design: In July 1994 MSI engineers completed the electronics design of the infrared and ultrasonic proximity sensors. The schematics and other details of the design were delivered to ORNL.

Communication Interface Design: In February 1995 agreement between MSI and ORNL was reached on a communications interface between the ASIC and the MSI distributed processing system.

Modified ASIC Design: Documentation for the infrared sensor ASIC design was completed and delivered to MSI in July 1995. The documentation for the acoustic sensor ASIC design, as well as all data required to order the ASIC components, was delivered to MSI September 28, 1995.

Component Fabrication: MSI delivered to ORNL sufficient infrared and acoustic sensors to allow testing of sensor electronics. Prototype quantities of the infrared proximity sensor and the acoustic sensor ASICs were ordered and delivered to ORNL.

System Integration and Test: ORNL completed the preliminary evaluation of the fabricated ASICs. ORNL designed, fabricated and evaluated test cards which allow the ASICs and associated sensors to be used in the MSI sensor system. MSI completed modifications to their system to fit the communication standard agreed upon. The system test was conducted in mid-December, 1995. Both the infrared ASIC and acoustic ASIC sensor modules, developed as part of the CRADA, functioned well in the MSI sensor test system. The results were equal to or better than the non-ASIC sensor modules previously developed by MSI.

Benefits to DOE

This CRADA extended the capability of the proximity sensing systems initially developed under EM-50 funding for robotic systems to include additional sensor types. It is clear from previous sensor development and testing that multiple sensor types are necessary to provide adequate proximity data in the variety of environments in which manipulators are deployed in support of environmental restoration and waste management activities. This CRADA allowed the extension of the ORNL developed ASIC design to support infrared and acoustic proximity sensors in addition to the original capacitive sensors and provided the technology transfer of the ASIC design for the sensor electronics to a commercial supplier. The proximity sensing system resulting from this CRADA provides the needed multi-modal sensing capability.

Technical Discussion

Prior to this CRADA, researchers at ORNL developed a capacitive proximity sensing system for robotics applications. The system is based upon the sensornode application specific integrated circuit (ASIC). Each sensor uses a single ASIC to excite the sensor, amplify and process the signal returned by the sensor, digitize it and communicate that result to a microcontroller. Multiple sensors are arranged in "bracelets" consisting of the sensors, a communications bus and the microcontroller board. The system is formed from multiple bracelets that communicate via a token ring network to a VME-based host processor. The host processor maintains an array of sensor readings and reports any close objects to the processor controlling the robot the sensing system protects. This system, referred to as the Whole Arm Obstacle Avoidance (WAOA) system is described in detail in ORNL TM/12969.

During approximately the same time frame, Merritt Systems, Inc. (MSI) was developing an IR and acoustic proximity sensing system also for robotics applications. This system used commercially-available integrated circuits and also had a microcontroller-based communications network.

The goal of the CRADA was to combine the ORNL ASIC design and the MSI sensor types to provide a commercially available proximity sensor system capable of utilizing capacitive, infrared and/or acoustic sensors. Using the ORNL capacitive proximity sensor ASIC and the MSI infrared and acoustic sensors as the basis of new designs, two new ASICs were developed. One is an IR proximity sensor ASIC that uses a detection method much like that used in the capacitive proximity sensor (except for using an IR emitter and detector, instead of a capacitor), while the other is an Acoustic proximity sensor ASIC that works in conjunction with a microcontroller to make a time-of-flight measurement for a ultrasonic pulse and its reflection.

An IR proximity sensing unit contains an IR emitter, an IR detector, an IR Proximity Sensor ASIC and a microcontroller. The ASIC drives the emitter, the detector receives and converts reflected IR signals to electrical signals which are processed by the ASIC. The strength of the processed output is proportional to the target range. The output of the ASIC is converted to a digital format and made available to the overall sensing system by the microcontroller. The microcontroller is also responsible for setting up and controlling the ASIC's mode of operation via a serial interface.

An acoustic proximity sensing unit contains an acoustic emitter, an acoustic detector, an Acoustic Proximity Sensor ASIC and a microcontroller. The microcontroller emits a burst of pulses which are supplied to the ASIC. In turn, the ASIC buffers the burst to the emitter, the detector receives and converts reflected acoustic signals to electrical signals which are amplified and detected by the ASIC. The output of the ASIC is digital level indicating a reflected signal has been received, and that output is supplied to the microcontroller, which measures the time between emitted burst and the return. The microcontroller is also responsible for setting up and controlling the ASIC's mode of operation via the serial interface.

A series of tests were conducted to first to verify the correct operation of the two types of proximity sensing ASICs and then to demonstrate the capabilities of the sensing units. Prototype sensor units were made using the ASICs, incorporated into an MSI sensing system and successfully demonstrated. The IR proximity sensor unit

was capable of sensing objects at distances up to 30 inches while, the acoustic proximity sensor unit could sense objects up to 25 inches distant. In the case of the acoustic unit, the limit was due to maximum time of flight allowed by the microcontroller software. It appears that in both cases that greater ranges are possible with some adjustments, however, even the measured performance was as good or better than the non-ASIC sensors previously available.

An in-depth technical discussion is provided in Attachment 1.

Inventions

No inventions were made or reported.

Commercialization

MSI has licensed the ASIC design from ORNL. As of December, 1995, MSI has not found a volume application for proximity sensors that would make it economical to fabricate a run of ASIC chips (at a cost of \$100K for 20,000 chips). It is MSI's intention to use the ASIC design resulting from this CRADA within their commercial products when economically feasible.

Future Collaboration

MSI has indicated an interest in further collaboration with ORNL on other sensor types. MSI has entered into a separate CRADA with Sandia National Laboratories to explore joint development of capacitive proximity sensors.

Conclusion

All of the objectives of this CRADA were successfully met.

Attachment 1

**Merritt Systems, Inc. CRADA Project
Technical Discussion**

**A. L. Wintenberg, M. N. Ericson and J. W. Halliwell
Oak Ridge National Laboratory**

Merritt CRADA Project

Final Report. Rev. 0

April 20, 1996

A. L. Wintenberg, M. N. Ericson and J. W. Halliwell
Oak Ridge National Laboratory

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ASIC

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1.0 Introduction

Prior to this CRADA, researchers at ORNL developed a capacitive proximity sensing system for robotics applications. The system is based upon the sensor node application specific integrated circuit (ASIC). Each sensor uses a single ASIC to excite the sensor, amplify and process the signal returned by the sensor, digitize it and communicate that result to a microcontroller. Multiple sensors are arranged in "bracelets" consisting of the sensors, a communications bus and the microcontroller board. The system is formed from multiple bracelets that communicate via a token ring network to a VME-based host processor. The host processor maintains an array of sensor readings and reports any close objects to the processor controlling the robot the sensing system protects. This system, referred to as the Whole Arm Obstacle Avoidance (WAOA) system is described in detail in ORNL TM/12969.

During approximately the same time frame, Merritt Systems, Inc. (MSI) was developing an IR and acoustic proximity sensing system also for robotics applications. This system used commercially-available integrated circuits and also had a microcontroller-based communications network.

1.1 Goal of the CRADA

The goal of the CRADA was to combine the ORNL ASIC design and the MSI sensor types to provide a commercially available proximity sensor system capable of utilizing capacitive, infrared and/or acoustic sensors.

1.2 Summary of Achievements

Using the ORNL capacitive proximity sensor ASIC and the MSI infrared and acoustic sensors as the basis of new designs, two new ASICs were developed. One is an IR proximity sensor ASIC that uses a detection method much like that used in the capacitive proximity sensor (except for using an IR emitter and detector, instead of a capacitor), while the other is an Acoustic proximity sensor ASIC that works in conjunction with a microcontroller to make a time-of-flight measurement for a ultrasonic pulse and its reflection. Prototype sensor units were made using these ASICs, incorporated into an MSI sensing system and successfully demonstrated.

1.3 Report Contents

The remainder of this report contains a description of the agreed to serial interface, descriptions of IR and Acoustic proximity sensor ASICs, a summary of integration of the ASICs into the MSI proximity sensing system, and test results using the hybrid system.

2.0 Serial Interface Standard

Communications between the sensor ASIC and the microcontroller allows a number of functions to be performed. Transfers of data from the microcontroller to the ASIC deliver commands and setup parameters needed for ASIC operation. Transfers of data from a ASIC to the microcontroller allow the reading of data, sensor ID and sensor status.

The communications interface between the microcontroller and sensor ASIC is a bi-directional serial link with the microcontroller as the master and the ASIC as slave. Data are transferred in packets of 8 bits since this approach allows compatibility with the PIC microcontroller used by MSI as well as most other microcontrollers such as 80C51 variants. CMOS-compatible, 5 V logic levels are used in the interface.

The microcontroller and sensor ASIC communication interface is composed of a 5 signal serial interface (see Fig. 2.1). These signals are defined as follows:

- SDATA - Serial data line (bi-directional)
- SCLOCK - Serial data clock.
- WR/RDB - Data direction control (read or write)
- STROBE - Pulse used to latch data within sensor ASIC.
- RESETB - Control to reset registers within sensor ASIC.

Depending upon the ASIC configuration, the data direction control (WR/RDB) may not be needed. If the ASIC only supplies analog signals for range information or pulsed logic signals for time of flight information, then the ability to read digital data out of the ASIC may not be needed, and the WR/RDB signal and functions associated with reading data may be discarded.

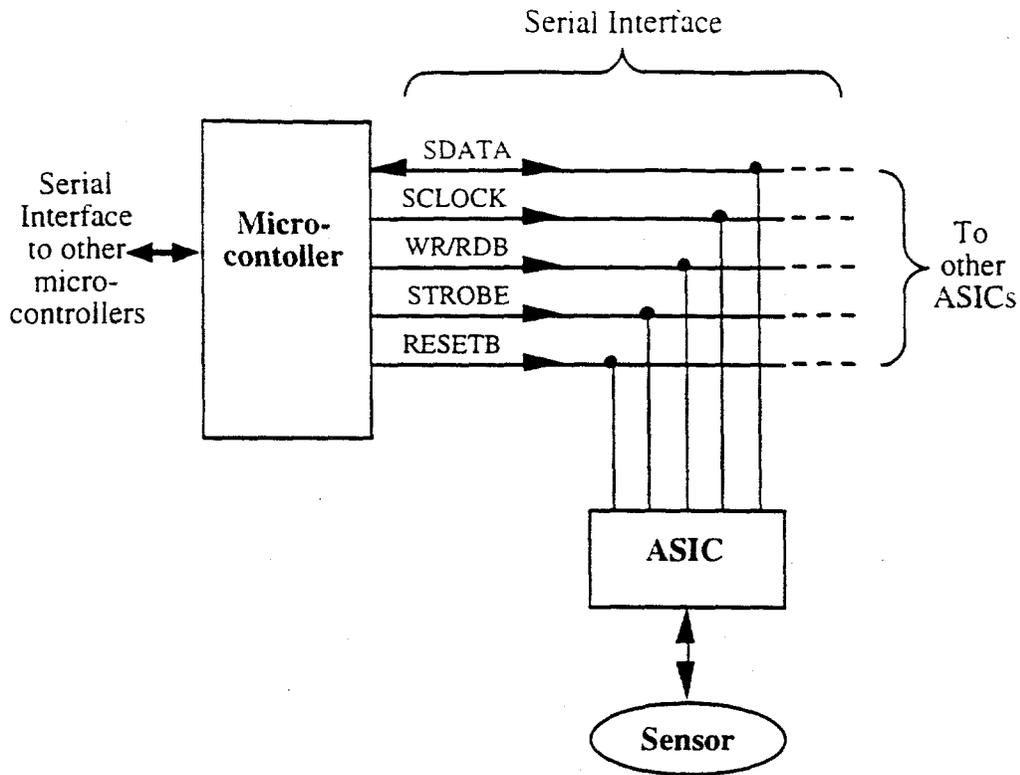


Fig. 2.1. Microcontroller and sensor ASIC communication interface.

This communication interface may be used in a network consisting of a microcontroller and a single ASIC or multiple ASICs connected in parallel. Certain details of the implementation may be simplified if only one ASIC is to be used per microcontroller. If multiple ASICs are used, they are connected in parallel and the serial interface can then be referred to as a serial bus.

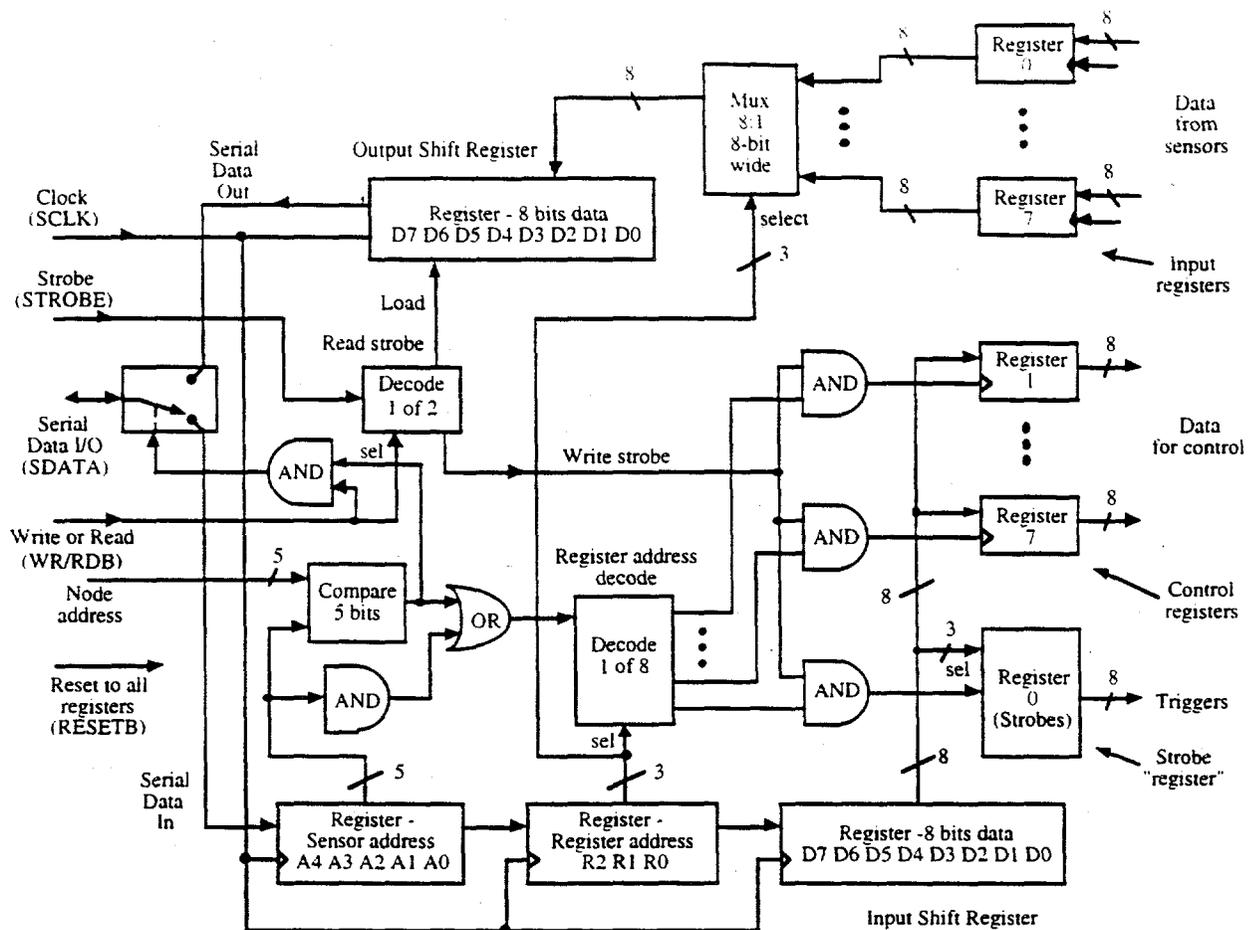


Fig. 2.2. Serial communication interface block diagram.

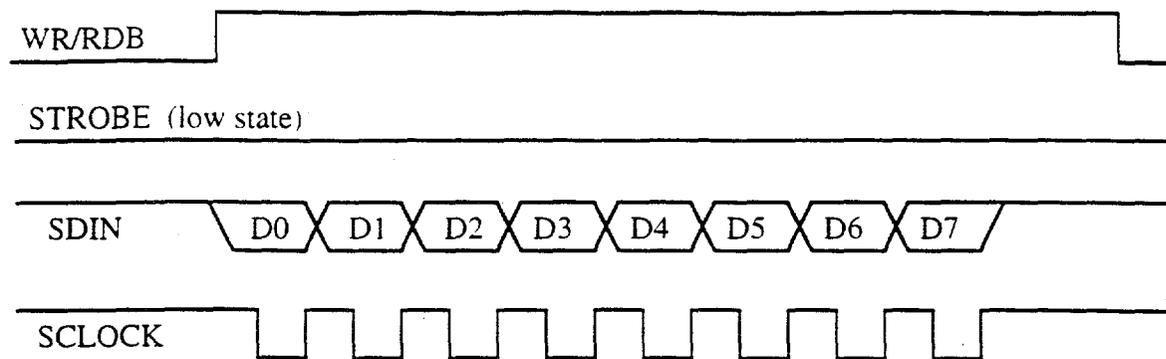
The block diagram shown in Fig. 2.2 is incorporated into the sensor ASICs as the serial interface. The architecture is based on switching the serial data line between two shift registers (one input and one output), using the WR/RDB line as a direction indicator, and shifting data (SDATA) using SCLOCK. STROBE is used to latch data to be transferred in or out of the appropriate shift register. RESETB is an active low signal and is used to clear all registers in the ASIC to provide a known initial condition at power up.

The input shift register is divided into three sections -- sensor address, register address, and data. The sensor address is used to identify which of the sensor ASICs is being addressed. This address is locally compared to a reference address (uniquely set for each sensor on the serial bus) and an address enable is asserted upon receipt of the proper address. Five register address bits are implemented allowing for as many as 32 sensor ASICs per serial bus

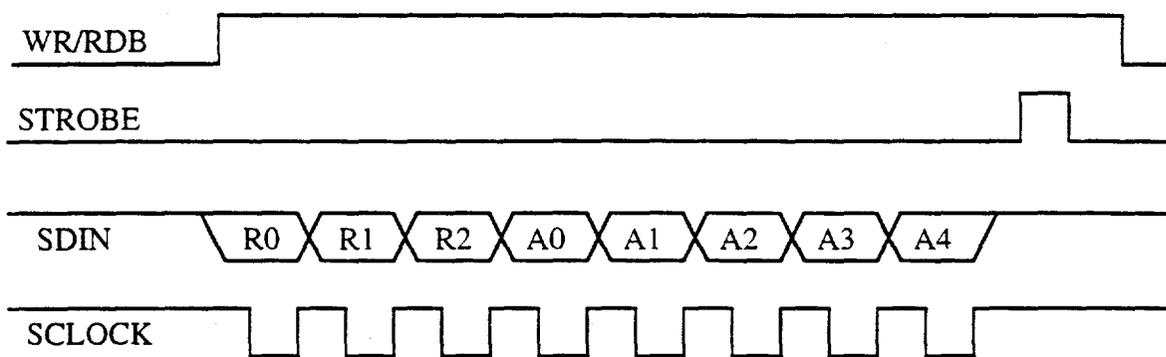
(microcontroller). In some instances improved speed can be obtained by writing some control commands to all ASICs on the serial bus simultaneously. To provide this capability, one address is reserved for a global write which reduces the maximum number of sensor ASICs to 31. The global write address is 31 (11111 in binary). The register address bits (3) are used for selection of on-chip registers to be used for sensor ASIC control and data acquisition. The registers are grouped into two types, input and control, and the type is selected by the write/read control signal (WR/RDB). Eight of each type are possible, but the actual implementation will likely require fewer input and control registers. The data byte of the input shift register contains data that can be loaded into one of the ASIC control registers.

A data write is accomplished by initiating the timing sequence detailed in Fig. 2.3a. Through the use of the shift clock, two 8-bit data bytes are shifted globally to the sensor ASIC(s) with the WR/RDB held in the high state. Within the ASIC, shifting takes place on the falling edge of SCLOCK, so the data (SDATA) must be settled in advance of the falling edge of SCLOCK. As previously mentioned, the first byte contains the data, the second the address bits for the sensor ASIC and selected control register. Within the addressed ASIC, assertion of the STROBE signal transfers data from the input shift register data byte into the selected sensor ASIC control register. The control register is loaded on the falling edge of STROBE for a write operation. All registers used in each of the ASICs can be configured using this procedure.

A data read is similarly accomplished using the timing sequence shown in Fig. 2.3b. A write operation is first performed to write only the address byte into the input shift register. This byte, as before, is used to select the sensor ASIC and associated data register to read. It is not necessary to write an additional data byte. After a byte write, the data is then read by setting the WR/RDB line to the low state (indicating a read operation), asserting the STROBE line which loads the selected input register data byte into the output shift register, and then serially shifting the data out using SCLOCK. Within the ASIC, shifting takes place on the falling edge of SCLOCK, so the microcontroller must allow the data (SDATA) to settle before considering it valid. For a read operation, STROBE is level sensitive and the high state is used to transfer data into the output shift register. After all data have been removed, the WR/RDB line is returned to the high state.

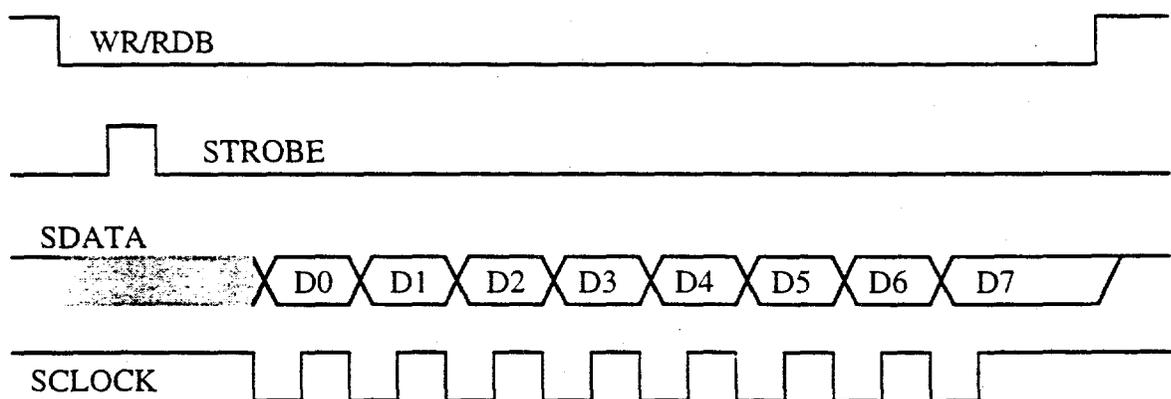


FIRST BYTE WRITE



SECOND BYTE WRITE

(A) Data Write



(B) Data Read (must be preceded by Data Write)

Fig. 2.3. Serial communication timing diagrams.

For some control purposes, it will be necessary to supply pulses to the sensor electronics. An addition to the data write process allows the generation of pulses with the same addressing capabilities. As in the data write, two 8-bit data bytes are shifted globally to the sensor ASIC. The address is decoded to produce an enable and the STROBE signal transfers the data into the addressed register. In addition, if the register address is 0, a decoder is enabled which allows passing the STROBE signal to one of 8 outputs which are selected with the lower 3 bits of the data. Thus writing a certain data byte to register 0 will also produce a pulse which can be used to start a process in the sensor ASIC. For example, the pulse could be used to start an analog-to-digital converter. The width of this pulse is application dependent.

It is possible to test many of the communication functions of the ASIC and the circuitry communicating with it by writing a data byte to the ASIC and reading it or part of it back. This requires that the control register have at least some of its bits connected to an input register (within the ASIC.) This exercise tests the ASIC addressing, the input shift register, (part of) the control register, the output data multiplexer and (part of) the output shift register. This feature can be implemented if space permits.

3.0 IR Proximity Sensor ASIC

This section describes the IR proximity sensor ASIC from a descriptive and operational viewpoint.

3.1 An Overview of the IR Proximity Sensor ASIC

An IR proximity sensing unit contains an IR emitter, an IR detector, an IR ASIC and a microcontroller as shown in Fig. 3.1. The ASIC drives the emitter, the detector receives and converts reflected IR signals to electrical signals which are processed by the ASIC. The output of the ASIC is converted to a digital format and made available to the overall sensing system by the microcontroller. The microcontroller is also responsible for setting up and controlling the ASIC's mode of operation.

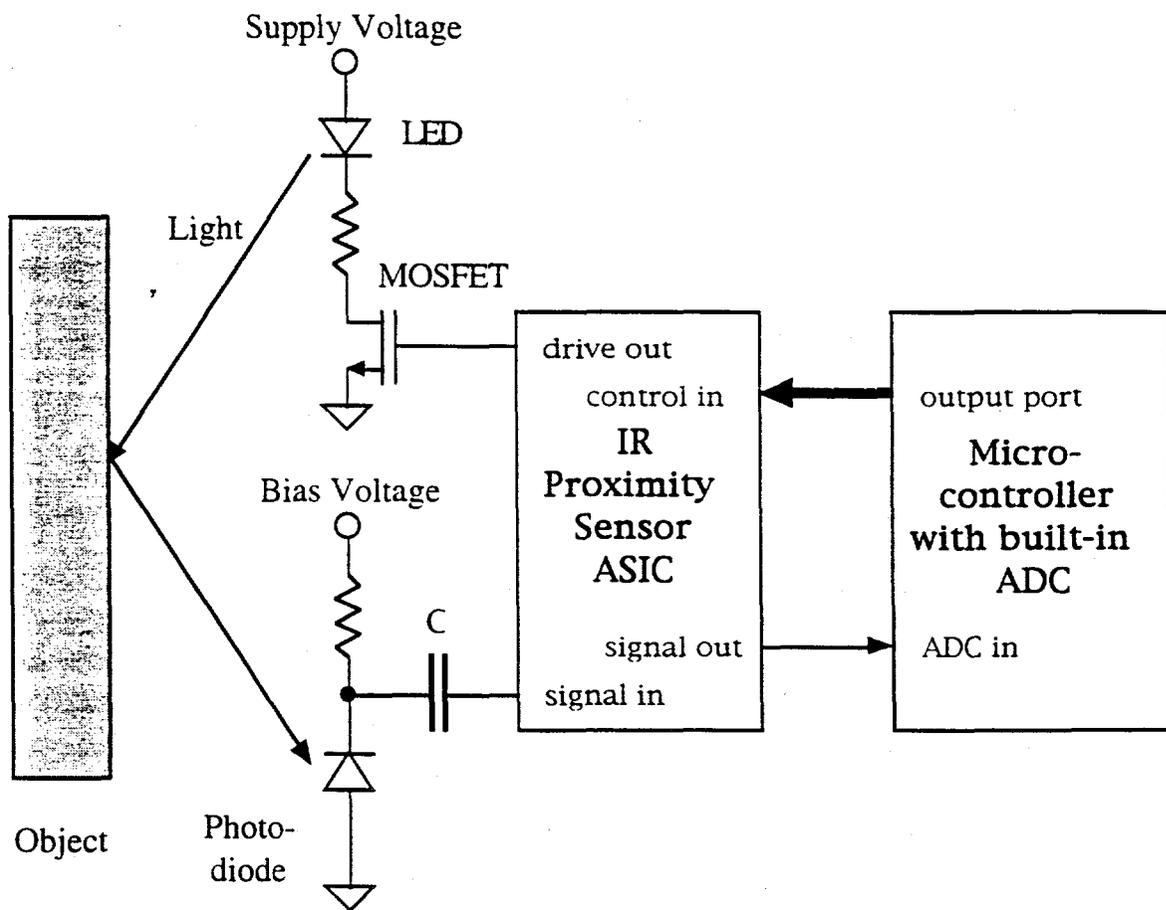


Fig 3.1. IR proximity sensor unit.

As shown in ASIC block diagram (Fig. 1.2), the IR proximity sensor ASIC is subdivided into three major blocks. The oscillator block provides sensor excitation. The analog signal processing block processes the signals received from the sensors and feeds the ADC. The communications and control block handles all communication from the microcontroller and controls the operation of the other blocks. The three blocks making up the ASIC are described in greater detail in the remainder of this document.

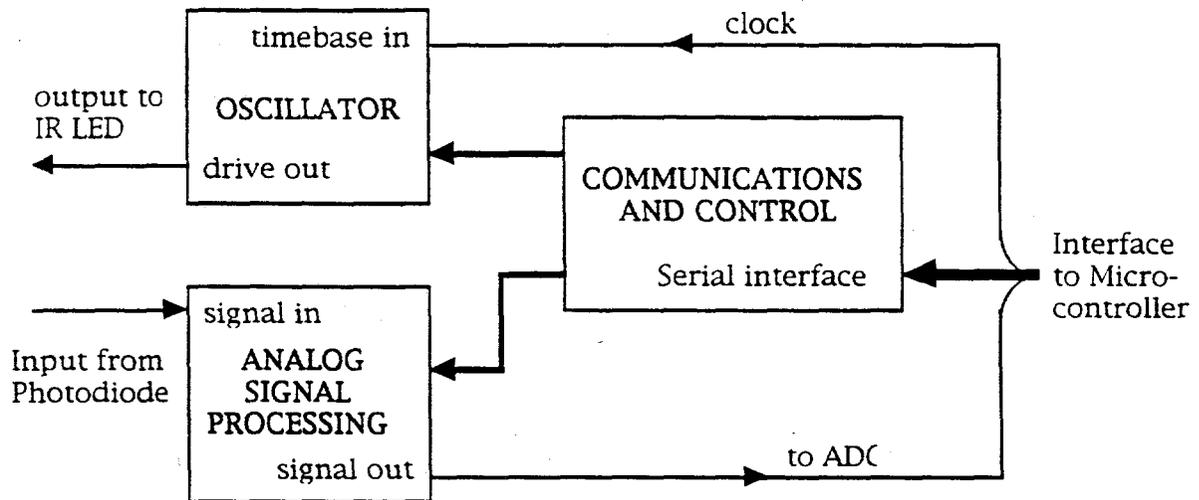


Fig. 3.2. IR proximity sensor ASIC functional block diagram.

3.2 ASIC Technology for the IR Proximity Sensor

The IR proximity sensor ASIC was designed using a 2-micron n-well CMOS process. This process was chosen for a number of reasons. First, this process is readily available from the MOSIS service and from ORBIT Semiconductor. This allows prototyping in a timely manner at reasonable expense. Second, a large number of useful analog cells (opamps, comparators, ADC, etc.) are available in that process. A full set of standard digital cells is also available. The use of previously designed cells greatly speeds the ASIC design and development process.

3.3 Oscillator

The IR proximity sensor is an active sensor and requires a periodic excitation signal. The oscillator provides this drive signal for the IR proximity sensor. The block diagram of the oscillator is shown in Fig.

3.3. The oscillator logic generates a frequency needed for sensor drive and the demodulation control needed by the analog signal processing module. There are complementary outputs for various configurations of IR emitter drivers.

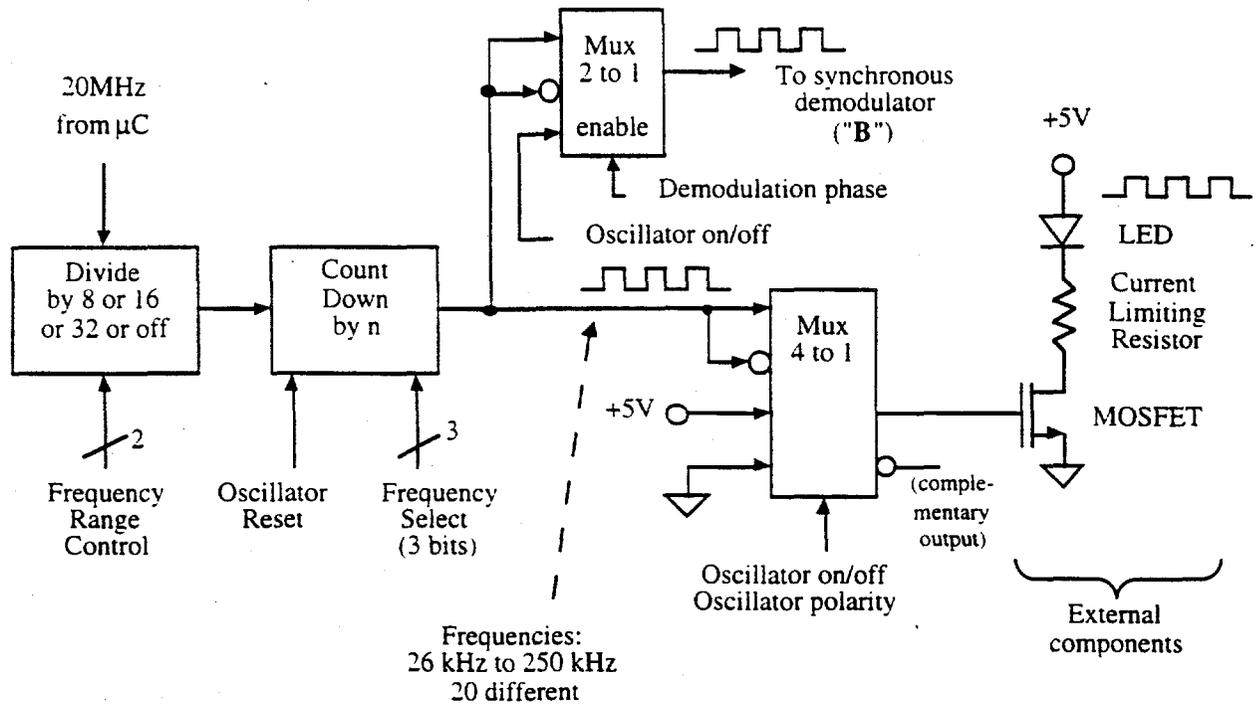


Fig. 3.3. , Oscillator block diagram.

The oscillator frequency is programmable to the extent that several frequencies in the range of 25 to 250 kHz are available. These choices of frequency may be needed to implement a system of many nodes with overlapping sensitive zones. Adjacent sensors need to operate at different frequencies to prevent interference. This feature may not be necessary if the oscillator in each sensor node needs only to be turned on briefly in order to make a proximity measurement.

The oscillator frequency is digitally generated from the microcontroller 20-MHz timebase. This timebase is distributed to the attached ASIC or ASICs. The oscillator divides this base frequency by a factor of 8 to yield a 2.5 MHz timebase which is further divided according to a 3-bit frequency select code (FS2-0). This produces a frequency in the range of 83 to 200 kHz. As an option, another control (OSC1-0) may be used to divide the 2.5 MHz base frequency by a factor of two or four. Thus any of the frequencies given in

Table 3.1 may be developed. The base oscillator output is designated by MOD_FREQ. This signal is buffered before being used to excite the sensors. The OSC1-0 control can also be used to disable the oscillator if both bits are set to 0.

Table 3.1. Oscillator frequency as a function of frequency select code.

Frequency Select Code (FS2-0)	Oscillator Frequency (kHz)	Oscillator Frequency (kHz)	Oscillator Frequency (kHz)
	(OSC1-0 = 11)	(OSC1-0 = 10)	(OSC1-0 = 01)
000	250.0	125.0	62.5
001	208.3	104.2	52.1
010	178.6	89.3	44.6
011	156.3	78.1	39.1
100	138.9	69.4	34.7
101	125.0	62.5	31.3
110	113.6	56.8	28.4
111	104.2	52.1	26.4

The oscillator is not designed to excite an IR emitter directly, unless currents less than 5 mA are anticipated. The oscillator basic output (MOD_FREQ) is buffered through some logic which produces the outputs OSC_OUT and OSC_OUT_BAR. An external positive voltage is needed for the IR emitter (can be the +5V supply), and a series resistor should be used to limit the current through the emitter and the external drive transistor.

The signals provided by the communications and control block that are required to operate the oscillator are given in Table 3.2.

Table 3.2 Oscillator Block Control Signals

Control	Number of bits	Function
FS2-0	3	output frequency control
OSC1-0	2	frequency range select and enable

OSC_POL	1	output polarity
RST_OSC	1 (pulse)	reset oscillator
D_PHASE	1	demodulation phase select

The effects of FS2-0 and OSC_1-0 have already been discussed. However it is worth repeating that if OSC_1 and OSC_0 are both zero, then the oscillator is off. OSC_POL controls the polarity of the main output (OSC_OUT). If OSC_POL is zero and the oscillator is off, then OSC_OUT will be low, while if OSC_POL is one and the oscillator is off, then OSC_OUT will be high. If the oscillator is on, then OSC_OUT will be the same as MOD_FREQ if OSC_POL is one, and OSC_OUT will be the complement of MOD_FREQ if OSC_POL is zero. OSC_OUT_BAR is always the complement of OSC_OUT.

The RST_OSC signal resets the oscillator. To insure proper oscillator operation, it is necessary to reset the oscillator after the frequency selection (FS2-0) is changed. The D_PHASE signal is used to control the demodulation operation and is described in the section on analog signal processing.

3.4 Analog Signal Processing

The analog signal processing block detects the signal from the sensor, amplifies, demodulates and filters it. This process produces a dc voltage that may be digitized by an ADC. The analog signal processing for the IR proximity ASIC incorporates the circuits shown in Fig. 3.4. The vast majority of these circuits are implemented as parts of the ASIC and only a limited external components are required.

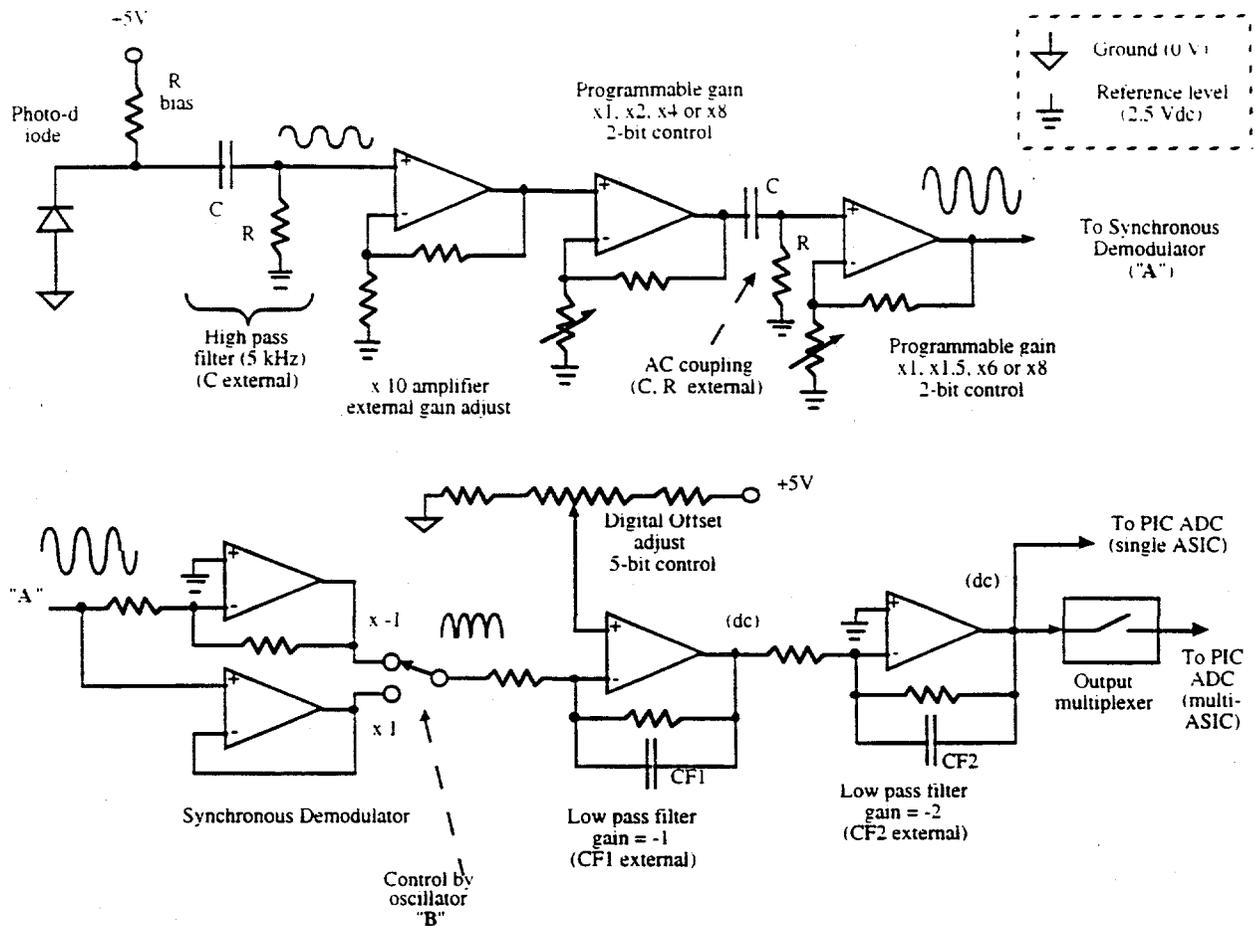


Fig. 3.4. Analog signal processing circuit block diagram.

The IR photodiode detector is biased through external resistor and ac-coupled to the ASIC input through an C-R network that also acts as a high pass filter. This blocks the detection of ambient light and 60- or 120-cycle light due to room lights, etc. The input to the ASIC is amplified by an amplifier with a nominal gain of three. This gain may be increased to 10 by connecting the TAP1 pin to the 2.5-V reference or by adding an external resistor between the TAP0 pin and the 2.5-V reference. In the latter case, the gain would be $1 + 28k/(14k || R_{\text{external}})$.

This first amplifier feeds two cascaded programmable gain amplifiers (PGA). The first allows gains of x1, x2, x4 or x8, while the second allows gains of x1, x1.5, x6 or x8. An external C-R network between the two amplifiers is used to provide additional high-pass filtering and to remove any shift in the dc level due to offset voltages in the

first two amplifiers. Table 3.3 gives the control codes for each possible gain of the two PGAs.

Table 3.3. Programmable gain amplifiers controls and gains.

PGA 1 Control (GC1-0)	Gain PGA 1	PGA 2 Control (GC4-3)	Gain PGA 2
00	1	00	1
01	2	01	1.5
10	4	10	6
11	8	11	8

The output of the second programmable gain amplifier is the input to the synchronous demodulation and low pass filter section. The output of the second PGA feeds two additional amplifiers, one with unity gain and the other with a gain of -1. The inverting amplifier uses carefully matched equal value resistors so its gain will be as close to -1 as possible. The outputs of these two amplifiers are connected to the inputs of a two-to-one analog multiplexer. The operation of the multiplexer is controlled by the D_CTRL signal provided by the oscillator block. When D_CTRL is high, the output of the unity gain amplifier is connected to the input of the first lowpass stage and when D_CTRL is low, the output of the inverting amp is connected. Since D_CTRL is either the same as or the complement of the square wave that is the output of the oscillator (MOD_FREQ), this switching is done in phase with the oscillator output. Since the signal driving the sensor is derived from MOD_FREQ, the signal at the output of the multiplexer is a rectified version of the demodulator input because one half wave has passed through the unity gain amp while the following half wave has passed through the inverting amp. The on resistance of the multiplexer (less than 500 ohms) is sufficiently small and relatively constant with the applied voltage level that its effect on the succeeding inverting amplifier is minimal.

The operation of the demodulator may be modified based upon the oscillator control code (OSC1-0) and the demodulation phase (D_PHASE) controls, as shown in Table 3.4. This allows the polarity of the signal developed by the demodulation circuit to be reversed, or for the demodulator to be used as a unity gain buffer or as an

inverting buffer. Normal operation with the IR proximity sensor requires the oscillator to be enabled and D_PHASE =1 or 0 depending upon how the IR emitter and detector are connected and driven.

Table 3.4. Demodulation controls and functions.

Oscillator Control (OSC1-0)	Demodulation Phase (D_PHASE)	Demodulation Control (D_CTRL)	Demodulation Operation
00	0	0	invert signal, no demodulation
00	1	1	buffer signal, no demodulation
01, 10, or 11	0	oscillator output inverted	demodulate with inversion
01, 10, or 11	1	same as oscillator output	demodulate

Once the signal has been rectified, it is necessary to low pass filter it in order to provide a dc level for the ADC. As shown in Fig. 3.4, two inverting one-pole filters are cascaded in order to provide the low pass function. The first stage has a dc gain of -1 while the gain of the second stage is -2. These gains may be modified through the addition of external resistors. The bandwidth of each stage is set using an external capacitor to approximately 1000 Hz for the prototype. This gives an overall bandwidth of approximately 700 Hz for the lowpass filter. This corresponds to a step response risetime of 0.5 ms which means that the response time of the analog section is sufficient to allow digitization at a 1 kHz (1 sample per ms) rate. If a lower update rate is to be used, the bandwidth can be lowered by changing the external capacitors. This bandwidth should be as low as possible while still allowing the circuit to respond in-between samples.

A 5-bit digitally programmable potentiometer is used to allow adjustment of the dc level at the output (which is the input to the ADC. This voltage is fed to the non-inverting input of the opamp used in the first lowpass filter. From that point to the output of the first lowpass filter the dc gain is 2. Since the demodulated signal is inverted by this stage, it is subtracted from twice the output of the digital potentiometer. Since the second lowpass filter is inverting as well, a positive voltage proportional to the demodulated signal minus

4 times offset voltage is developed and input to the ADC. The digital potentiometer has fixed resistors added to its end terminals to bring the adjustment range to approximately +/- 2V at the output of the second low-pass filter. The digital potentiometer control bits (S4-0) allow programming of this offset. A low code produces a negative output, while a high code produces a positive output. For a code of 10000 (binary), the output should be approximately 2.5 Vdc.

The digital pot comprises a resistor string, a set of CMOS switches, a 4-to-16 decoder and a 2 input analog mux. The resistor string consists of 32 equal valued resistors (420 ohm each, 13.5 kohm total). The four most significant bits (S4-1) are decoded and used to close two of the 32 CMOS switches. The inputs of these switches are connected to adjacent taps on the resistor string and their outputs are connected to the two inputs of the analog mux which is controlled by the least significant bit (S0). The output of the analog mux is the digital pot output.

For applications using multiple ASICs with one microcontroller or other ADC, an output multiplexer is included. This allows the analog outputs of multiple ASICs to be fed to one ADC. If OUT_EN is high, the output multiplexer is turned on, and the output of the second lowpass filter is passed through. Only one ASIC at a time should have its output multiplexer enabled.

The ASIC requires an off-chip reference voltage of +2.5 Vdc. This voltage is used as a mid-point reference between +5V and ground, buffered and distributed to several points in the ASIC.

The signals provided by the communications and control block that are required by the analog signal processing block are summarized in Table 3.5.

Table 3.5 Analog Signal Processing Block Control Signals

Control	Number of bits	Function
D_CTRL	clock	demodulation control
GC1-0	2	programmable amp 1 gain control
S4-0	5	digital pot control code

GC4-3	2	programmable amp 2 gain control
OUT_EN	1	output multiplexer control

3.5 Communications and Control

The communications interface between the microcontroller and sensor ASIC is a uni-directional serial link with the microcontroller as the master and the ASIC as slave. Transfers of data from the microcontroller to the ASIC deliver commands and setup parameters needed for ASIC operation. Data are transferred in packets of 8 bits since this approach allows compatibility with the PIC microcontroller used by MSI as well as most other microcontrollers such as 80C51 variants. CMOS-compatible, 5 V logic levels are used in the interface.

The microcontroller and sensor ASIC communication interface is composed of a 4 signal serial interface (see Fig. 3.5). These signals are defined as follows:

- SDIN - Serial data line
- SCLOCK - Serial data clock.
- STROBE - Pulse used to latch data within sensor ASIC.
- MRST - Control to reset registers within sensor ASIC.

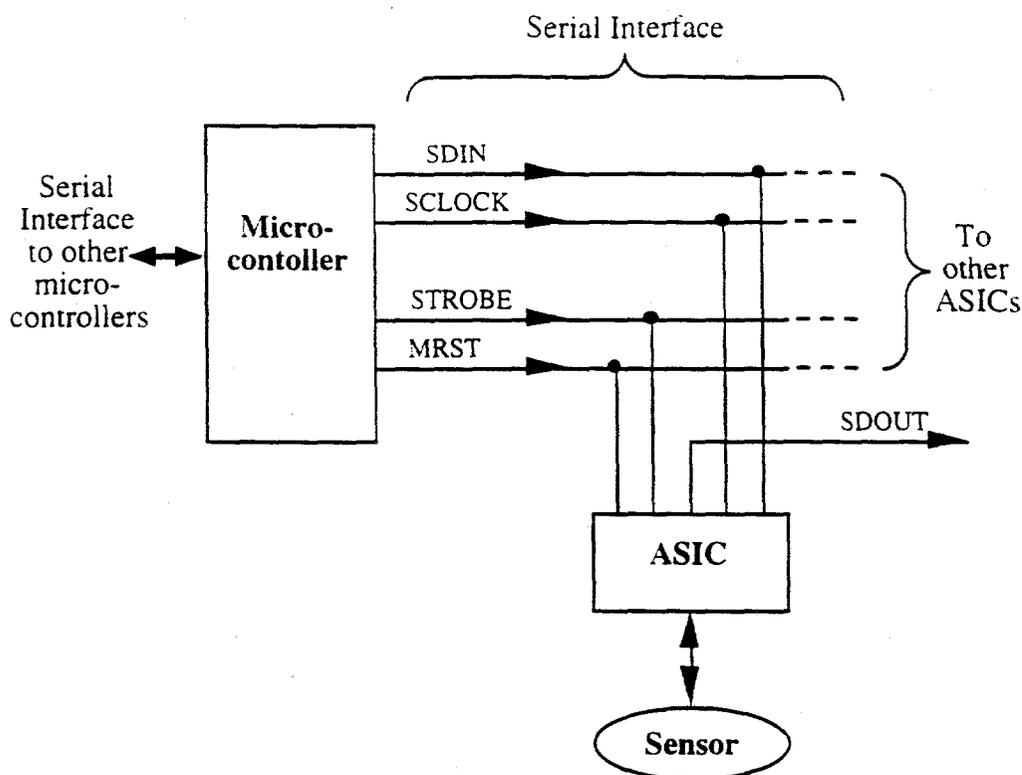


Fig. 3.5. Microcontroller and sensor ASIC communication interface.

This communication interface may be used in a network consisting of a microcontroller and a single ASIC or multiple ASICs connected in parallel. Certain details of the implementation may be simplified if only one ASIC is to be used per microcontroller. If multiple ASICs are used, they are connected in parallel and the serial interface can then be referred to as a serial bus.

The block diagram shown in Fig. 3.6 is incorporated into the sensor ASIC as the serial interface. The architecture is based on first shifting the serial data (SDIN) into an input shift register using SCLOCK, and then using the STROBE signal to latch data into the appropriate storage register. MRST is an active low signal and is used to clear all registers in the ASIC to provide a known initial condition at power up.

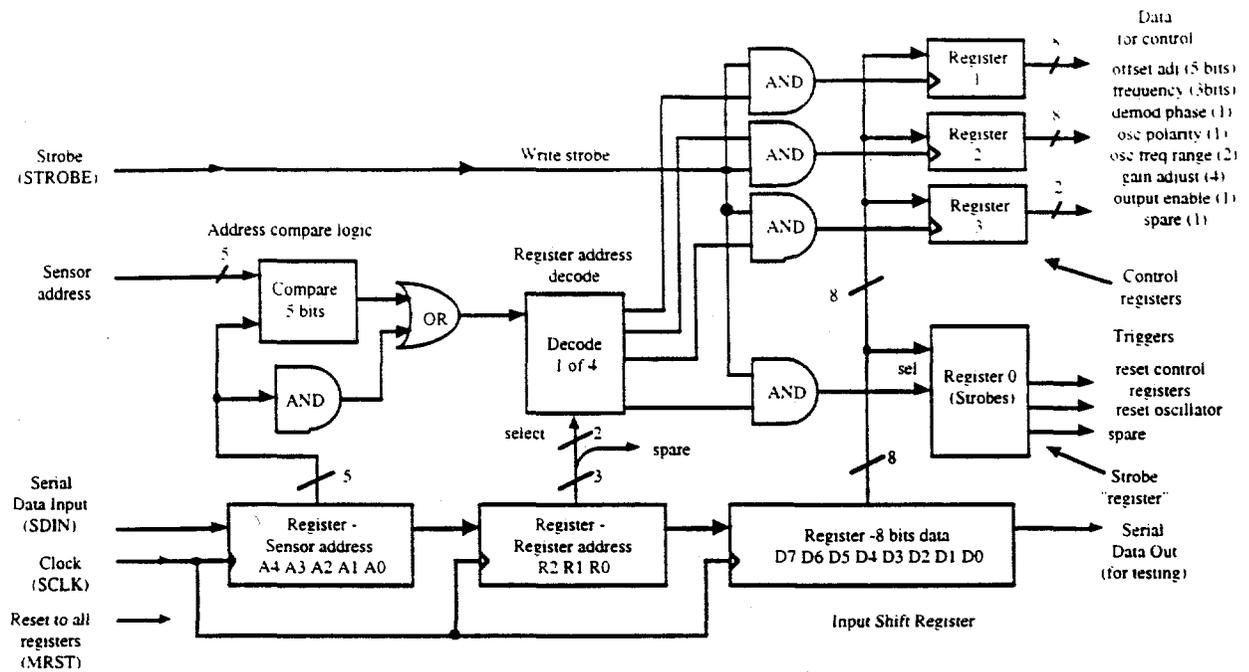


Fig. 3.6. Serial communication interface block diagram.

There is an additional output from the ASIC that is part of the serial interface; the serial data output (SDOUT). This output was included for diagnostic purposes, but it may be possible to use it to connect multiple ASICs in series as shown in Fig. 3.7. This may allow a greater data transfer rate to multiple sensors.

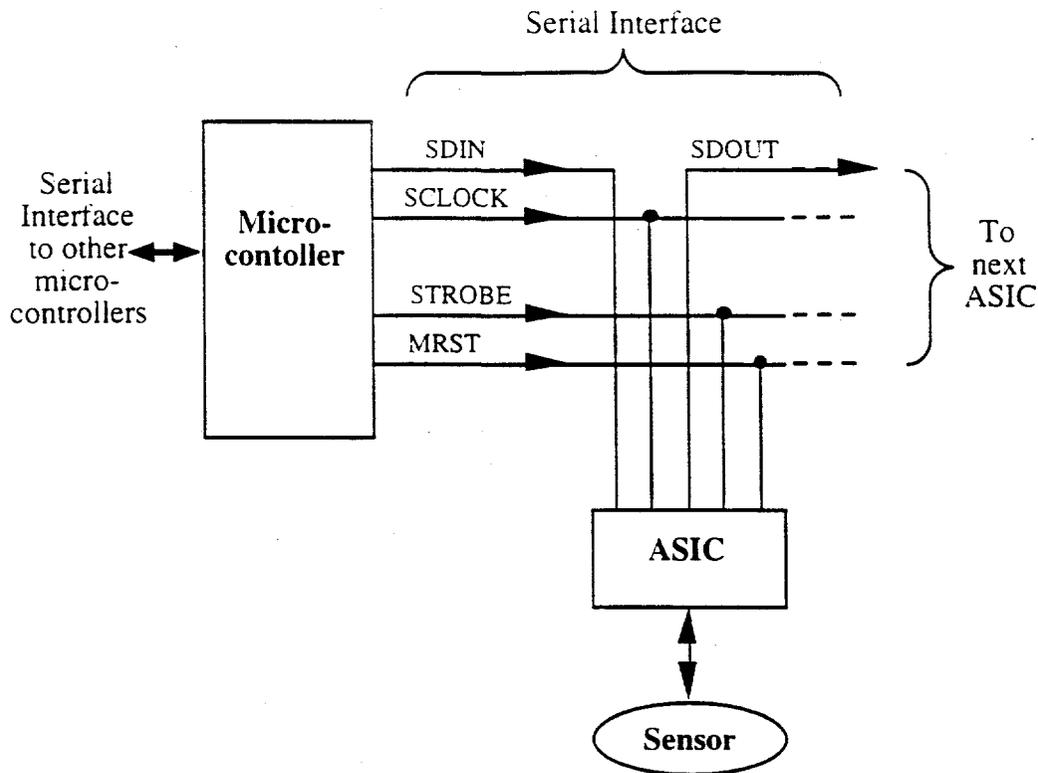


Fig. 3.7. Alternative microcontroller and sensor ASIC communication interface.

The input shift register is divided into three sections -- sensor address, register address, and data. The sensor address is used to identify which of the sensor ASICs is being addressed. This address is locally compared to a reference address (uniquely set for each sensor on the serial bus) and an address enable is asserted upon receipt of the proper address. Five register address bits are implemented allowing for as many as 32 sensor ASICs per serial bus (microcontroller). In some instances improved speed can be obtained by writing some control commands to all ASICs on the serial bus simultaneously. To provide this capability, one address is reserved for a global write which reduces the maximum number of sensor ASICs to 31. The global write address is 0 (0000 in binary). The register address bits (3) are used for selection of the on-chip registers used for sensor ASIC control. Eight registers are possible using 3 address bits, but the actual implementation requires fewer control registers. The data byte of the input shift register contains data that can be loaded into one of these control registers.

A data write is accomplished by initiating the timing sequence detailed in Fig. 3.8. Through the use of the shift clock, two 8-bit data

bytes are shifted globally to the sensor ASIC(s). Within the ASIC, shifting takes place on the falling edge of SCLOCK, so the data (SDIN) must be settled in advance of the falling edge of SCLOCK. As previously mentioned, the first byte contains the data, the second the address bits for the sensor ASIC and selected control register. Within the addressed ASIC, assertion of the STROBE signal transfers data from the input shift register data byte into the selected sensor ASIC control register. The control register is loaded on the falling edge of STROBE for a write operation. All registers used in each of the ASICs can be configured using this procedure.

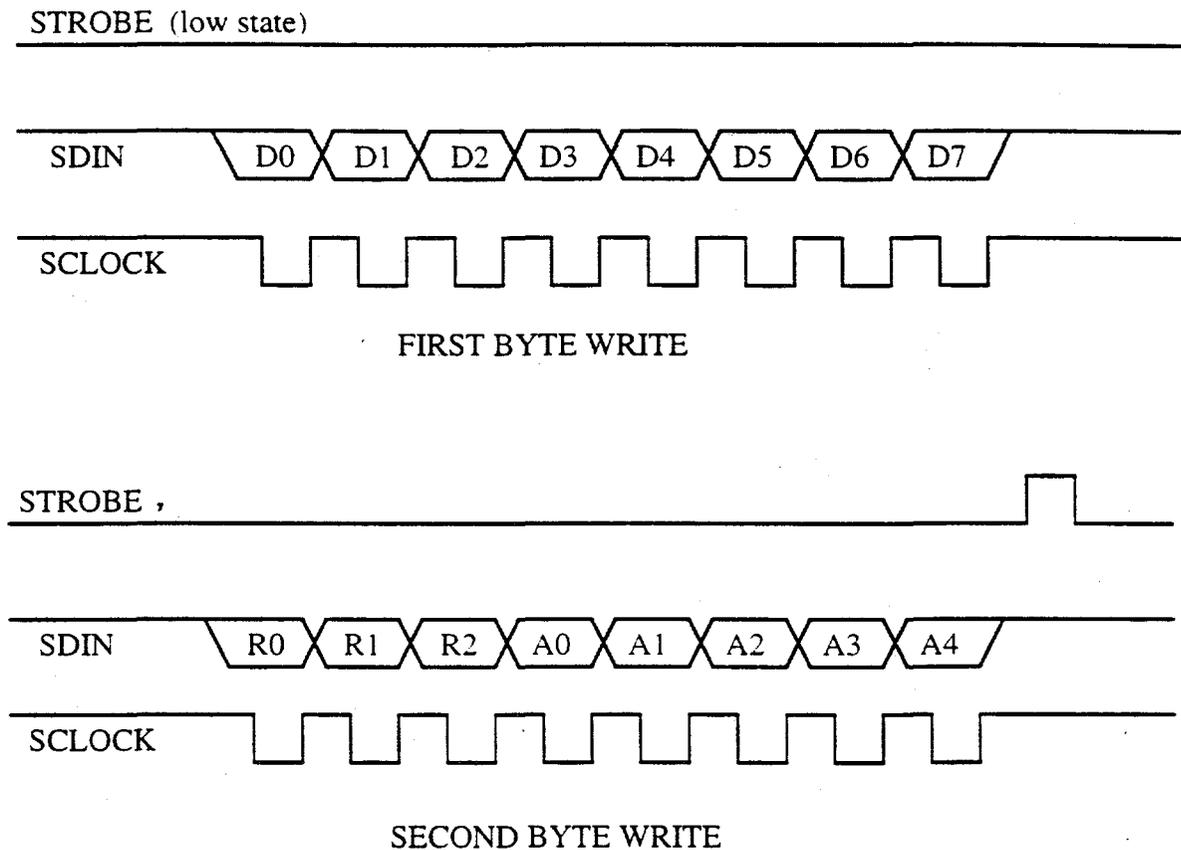


Fig. 3.8. Serial communications timing.

For some control purposes, it will be necessary to supply pulses to the sensor electronics. An addition to the data write process allows the generation of pulses with the same addressing capabilities. As in the data write, two 8-bit data bytes are shifted globally to the sensor ASIC. The address is decoded to produce an enable and the STROBE signal transfers the data into the addressed register. In addition, if

the register address is 0, a decoder is enabled which allows passing the STROBE signal to one of 8 possible outputs which are selected with the lower 3 bits of the data. Thus writing a certain data byte to register 0 will also produce a pulse which can be used to start a process in the sensor ASIC. For example, the pulse could be used to reset the oscillator. The width of this pulse is application dependent. Tables 3.6 and 3.7 shows the register assignments and the associated functions.

It is possible to test many of the communication functions of the ASIC and the circuitry communicating with it by writing data bytes to the ASIC and observing the serial data output (SDOUT). If the shift register is functioning properly, the output should be the same as the input, but with a 16 cycle (of SCLOCK) delay. Also, the reset function may be tested by clocking in a non-zero pattern (two bytes), asserting MRST and then clocking in two more bytes. The two bytes that are shifted out should contain all zeroes.

Register Address (binary)	Register Address (decimal)	Bit Assignment	Signal Name	Description
000	0	B7-2	(none)	not implemented
		B1	STRB1	strobe control bit 1
		B0	STRB0	strobe control bit 0
001	1	B7	OSC1	oscillator frequency control bit 1
		B6	OSC0	oscillator frequency control bit 0
		B5	GC4	programmable amp 2 gain control bit 1
		B4	GC3	programmable amp 2 gain control bit 0
		B3	DPHASE	demodulation phase control
		B2	FS2	frequency select bit 2
		B1	FS1	frequency select bit 1
		B0	FS0	frequency select bit 0
010	2	B7	OSC_POL	oscillator output polarity
		B6	GC1	programmable amp 1 gain control bit 1
		B5	GC0	programmable amp 1 gain control bit 0
		B4	S4	digital pot control bit 4
		B3	S3	digital pot control bit 3
		B2	S2	digital pot control bit 2
		B1	S1	digital pot control bit 1
		B0	S0	digital pot control bit 0
011	3	B7-2	(none)	not implemented
		B1	SDP1	spare bit (no external connection)
		B0	OUT_EN	multiplexed output enable

Table 3.6 Input and control register definitions.

STRB1-0 Code	Strobe Name	Description of Strobe
11	(none)	not used
10	RSTO	output register reset strobe
01	T1B	reset oscillator strobe
00	T0	spare

Table 3.7 Control strobe definitions.

4.0 Acoustic Proximity Sensor ASIC

This section describes the Acoustic proximity sensor ASIC from a descriptive and operational viewpoint.

4.1 An Overview of the Acoustic Proximity Sensor ASIC

An acoustic proximity sensing unit contains an acoustic emitter, an acoustic detector, an acoustic ASIC and a microcontroller as shown in Fig. 4.1. The ASIC buffers the drive to the emitter, the detector receives and converts reflected acoustic signals to electrical signals which are processed by the ASIC. The output of the ASIC is digital level indicating a reflected signal has been received which is then processed by the microcontroller. The microcontroller is also responsible for setting up and controlling the ASIC's mode of operation as well as generating the output pulse train for the emitter.

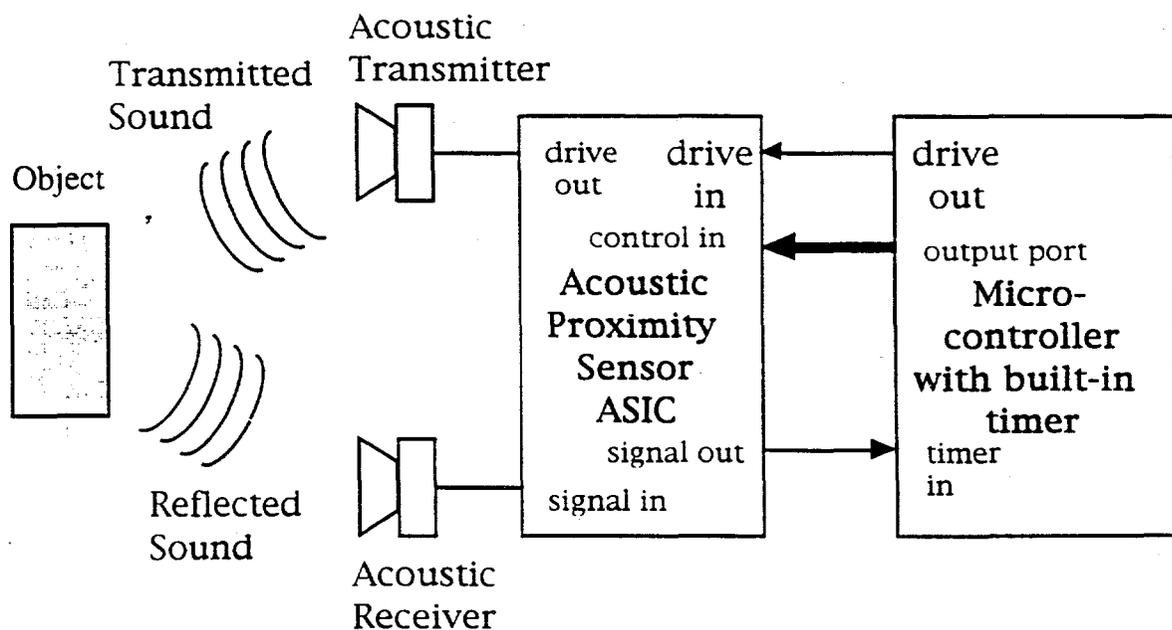


Fig 4.1. Acoustic proximity sensor unit.

As shown in the ASIC block diagram (Fig. 4.2), the acoustic proximity sensor ASIC is subdivided into three major blocks. The analog signal processing block processes the signals received from the sensors and converts this to a digital pulse which indicates

detected reflection. The communications and control block handles all communication from the microcontroller and controls the operation of the other blocks. The third block buffers the acoustic drive signal and provides complementary outputs for the acoustic emitter. The three blocks making up the ASIC are described in greater detail in the remainder of this document.

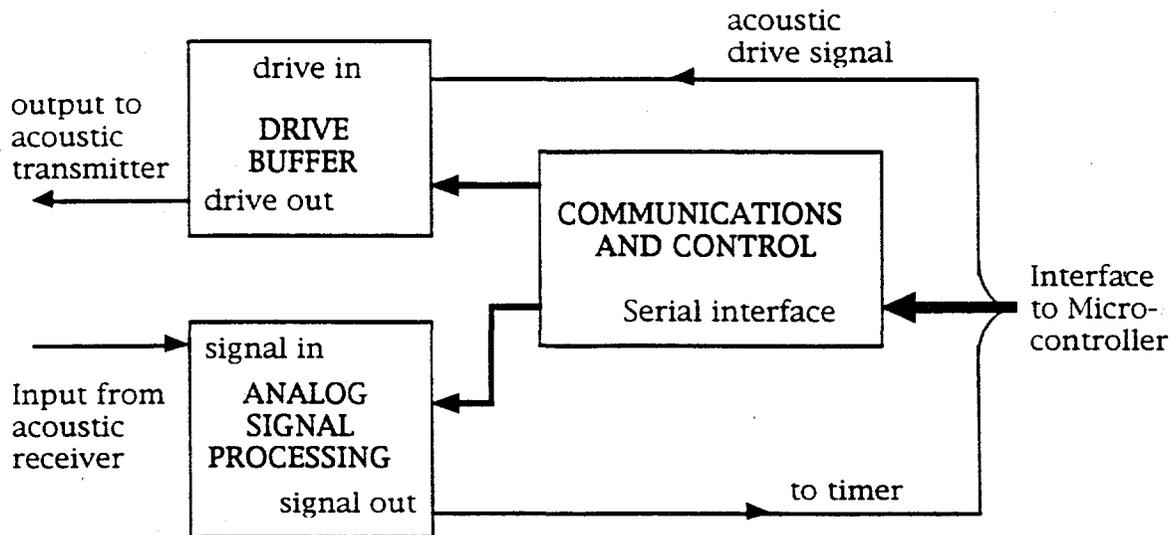


Fig. 4.2. Acoustic proximity sensor ASIC functional block diagram.

4.2 ASIC Technology for the Acoustic Proximity Sensor

The Acoustic proximity sensor ASIC was designed using a 2-micron n-well CMOS process. This process was chosen for a number of reasons. First, this process is readily available from the MOSIS service and from ORBIT Semiconductor. This allows prototyping in a timely manner at reasonable expense. Second, a large number of useful analog cells (opamps, comparators, ADC, etc.) are available in that process. A full set of standard digital cells is also available. The use of previously designed cells greatly speeds the ASIC design and development process.

4.3 Acoustic Emitter Drive Buffer

The acoustic proximity sensor is an active sensor and requires a periodic excitation signal. The drive signal timing is generated by the microcontroller and is then buffered by the ASIC. There are

complementary outputs for various configurations of acoustic emitter drivers, as illustrated in Fig. 4.3.

The acoustic emitter is a resonant device and therefore requires a fixed frequency drive pulse train. The emitter currently being used requires a 40 kHz drive signal. The number of cycles of drive can be varied in order to accommodate different ranging situations. A single cycle of drive is sufficient to provide proximity detection for distances in the 1 to 2 foot range. Typically, 5 to 10 cycles of drive would be used in order to provide a larger signal to noise ratio for the detector.

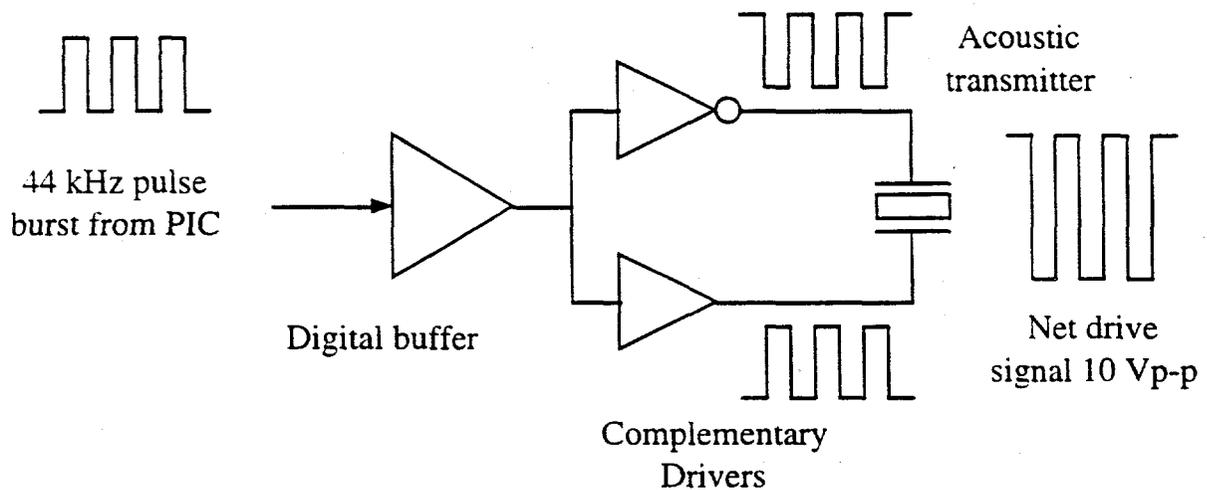


Fig. 4.3. Acoustic emitter drive block diagram.

4.4 Analog Signal Processing

The analog signal processing block (Fig. 4.4) of the ASIC is designed to detect a pulse burst signal from the acoustic sensor. The signal from the sensor is amplified, bandpass filtered, and then passes through a two-step pulse train detector. The pulse train detector consists of a pulse thresholding circuit followed by a low pass filter and then an envelope detecting circuit. The output from the envelope detector is passed to the microcontroller to indicate a signal has been received. Since the microprocessor generates the initial pulse train, the reflection signal time of flight, and thus distance, can be calculated. The vast majority of these circuits are implemented as parts of the ASIC and only a limited quantity of external components are required.

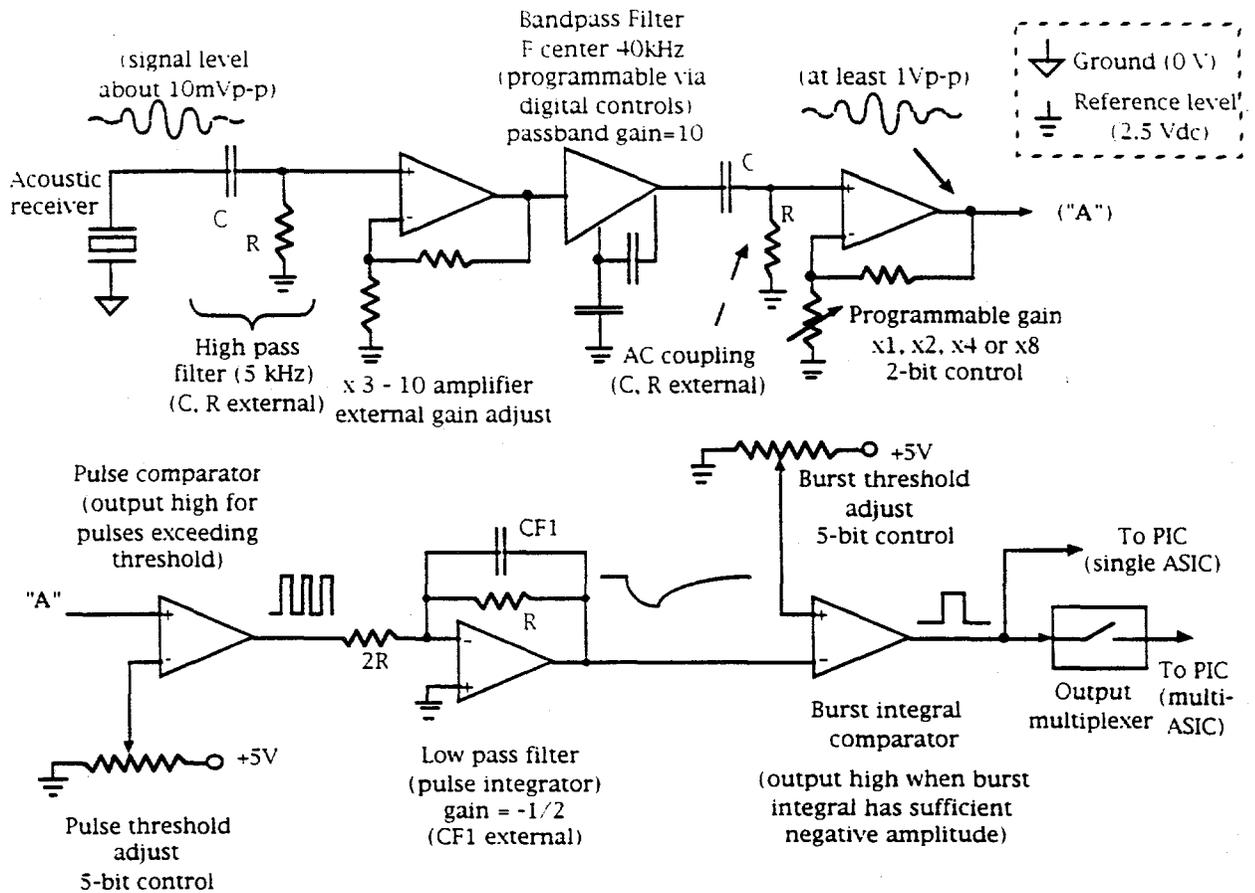


Fig. 4.4. Analog signal processing circuit block diagram.

The acoustic detector is used unbiased and is ac-coupled to reduce possible low frequency audio interference. A charge bleeding resistor is required at the input amplifier to prevent input offset drift due to leakage current. The ASIC amplifies the input signal with an amplifier with a nominal gain of three. This gain may be increased to 10 by grounding the TAP1 pin or by adding an external resistor between the TAP0 pin and the 2.5-V reference. In the latter case, the gain would be $1 + 28k / (14k \parallel R_{\text{external}})$.

This first amplifier feeds a bandpass filter which has a pin programmable center frequency. Inputs S1_con and S2_con allow the bandpass center frequency to be varied to four different values. External capacitors are used to tune the bandpass filter. The nominal center frequency of the filter is 40kHz which corresponds to the center frequency response of the acoustic transmitter and receiver.

The output of the band pass filter amplifier is the input to a single stage of programmable gain amplifier (PGA). Table 4.1 gives the gains of the PGA as a function of the control code GC1-0. The output of the PGA feeds the input of a pulse detection comparator. The comparator level is set to detect the individual pulses received from the acoustic detector, providing a fixed pulse train independent of the pulse reflection amplitude. The threshold level of this comparator is programmed by the microcontroller. Thirty-two comparator levels are available.

PGA 1 Control (GC1-0)	Gain PGA 1
00	1
01	2
10	4
11	8

Table 4.1. Programmable gain amplifier control and gains.

Once the individual pulses are level detected, it is necessary to low pass filter the waveform to acquire the pulse train envelope. As shown in Fig, 4.4, one inverting one-pole filter is used to provide the low pass function. The bandwidth of this stage is set using an external capacitor to approximately 3 kHz for the prototype. This corresponds to a step response risetime of 0.12 ms which is sufficient to detect the pulse train envelope. The output of the lowpass filter goes to a final level detector which is used to detect a particular level of the pulse train envelope. The comparator reference level in this detector is also programmed through the microcontroller.

Two separate 5-bit digitally programmable potentiometers are used to allow adjustment of the dc level at each of the level detectors. Each digital potentiometer has four control bits allowing programming of this level. A low code produces a zero output, while a high code produces a positive output. For a code of 10000 (binary), the output should be approximately 3.75 Vdc. The pulse detection threshold is set by S4-0, while the envelope detection level is set by TH4-0.

Each digital pot comprises a resistor string, a set of CMOS switches, a 4-to-16 decoder and a 2 input analog mux. The resistor string consists of 32 equal valued resistors (420 ohm each, 13.5 kohm total). The four most significant bits (S4-1 or TH4-1) are decoded and used to close two of the 32 CMOS switches. The inputs of these switches are connected to adjacent taps on the resistor string and their outputs are connected to the two inputs of the analog mux which is controlled by the least significant bit (S0 or TH0). The output of the analog mux is the digital pot output.

For applications using multiple ASICs with one microcontroller, an output multiplexer is included. This allows the envelope detected signal of multiple ASICs to be fed to one microprocessor input. If COMP_OE is high, the output multiplexer is turned on, and the output of envelope detector passed through. Only one ASIC at a time should have its output multiplexer enabled.

The ASIC requires an off-chip reference voltage of +2.5 Vdc. This voltage is used as a mid-point reference between +5V and ground, buffered and distributed to several points in the ASIC.

The signals provided by the communications and control block that are required by the analog signal processing block are summarized in Table 4.2.

Table 4.2. Analog Signal Processing Block Control Signals.

Control	Number of bits	Function
GC1-0	2	programmable amp 1 gain control
S4-0	5	pulse detect digital pot control code
TH4-0	5	envelope detect digital pot control code
COMP_OE	1	output multiplexer control

4.5 Communications and Control

The communications interface between the microcontroller and sensor ASIC is a uni-directional serial link with the microcontroller

as the master and the ASIC as slave. Transfers of data from the microcontroller to the ASIC deliver commands and setup parameters needed for ASIC operation. Data are transferred in packets of 8 bits since this approach allows compatibility with the PIC microcontroller used by MSI as well as most other microcontrollers such as 80C51 variants. CMOS-compatible, 5 V logic levels are used in the interface.

The microcontroller and sensor ASIC communication interface is composed of a 4 signal serial interface (see Fig. 4.5). These signals are defined as follows:

- SDIN - Serial data line
- SCLOCK - Serial data clock.
- STROBE - Pulse used to latch data within sensor ASIC.
- MRST - Control to reset registers within sensor ASIC.

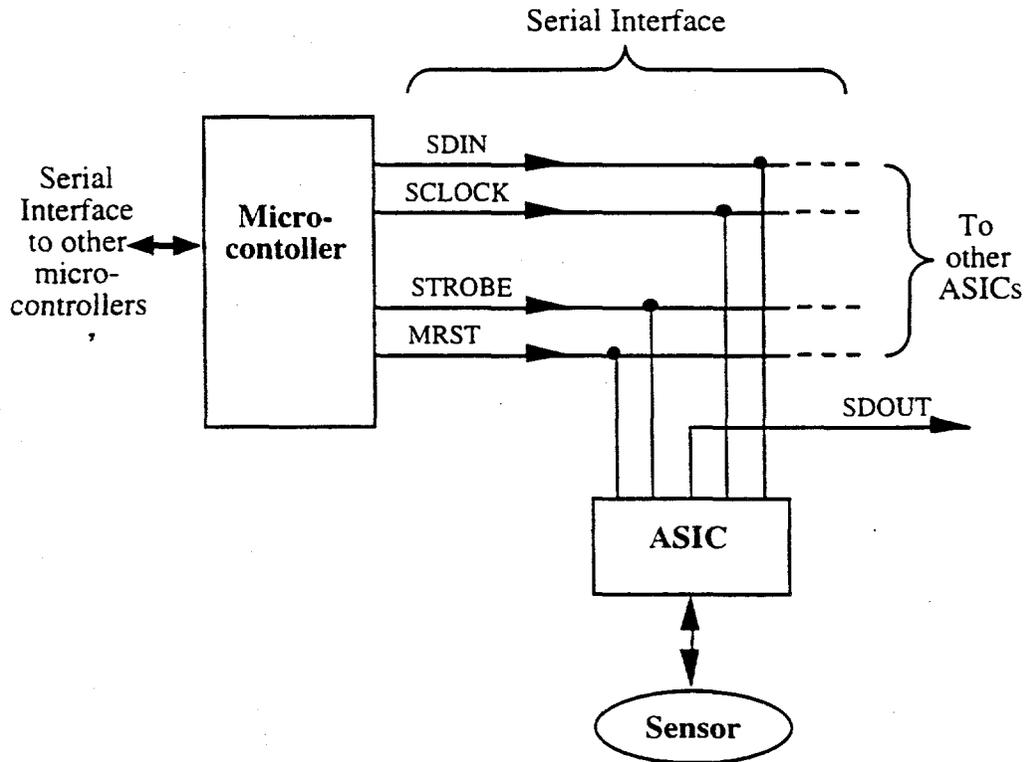


Fig. 4.5. Microcontroller and sensor ASIC communication interface.

This communication interface may be used in a network consisting of a microcontroller and a single ASIC or multiple ASICs connected in parallel. Certain details of the implementation may be simplified if only one ASIC is to be used per microcontroller. If multiple ASICs

are used, they are connected in parallel and the serial interface can then be referred to as a serial bus.

The block diagram shown in Fig. 4.6 is incorporated into the sensor ASIC as the serial interface. The architecture is based on first shifting the serial data (SDIN) into an input shift register using SCLOCK, and then using the STROBE signal to latch data into the appropriate storage register. MRST is an active low signal and is used to clear all registers in the ASIC to provide a known initial condition at power up.

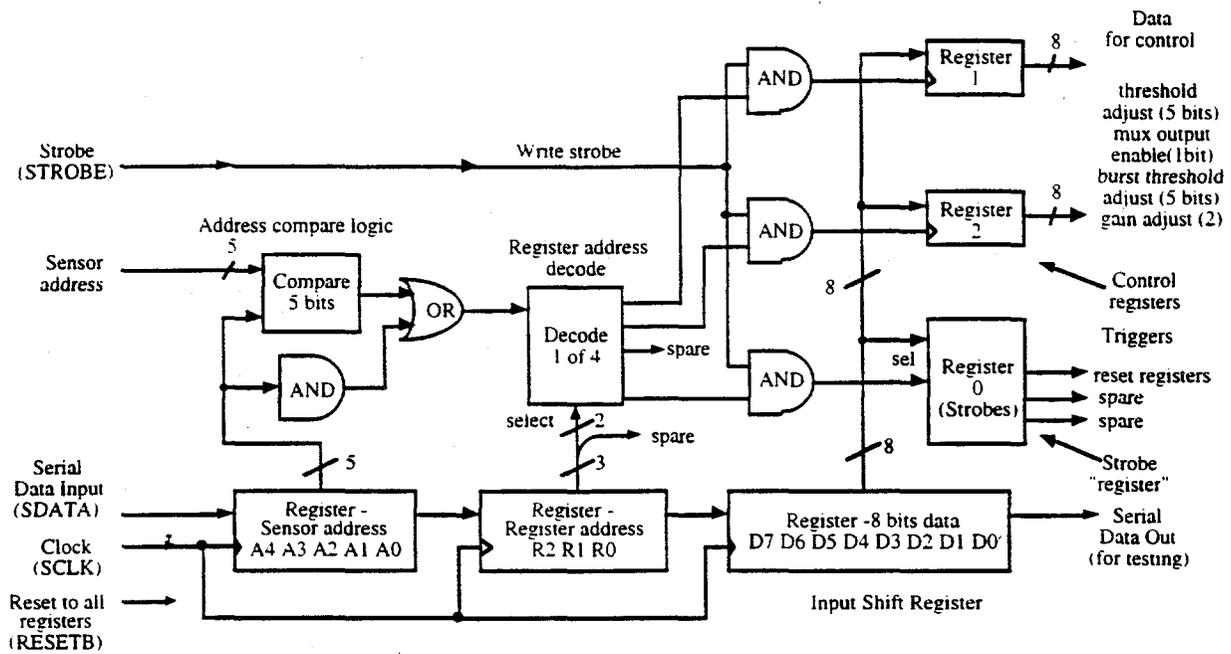


Fig. 4.6. Serial communication interface block diagram.

There is an additional output from the ASIC that is part of the serial interface; the serial data output (SDOUT). This output was included for diagnostic purposes, but it may be possible to use it to connect multiple ASICs in series as shown in Fig. 4.7. This may allow a greater data transfer rate to multiple sensors.

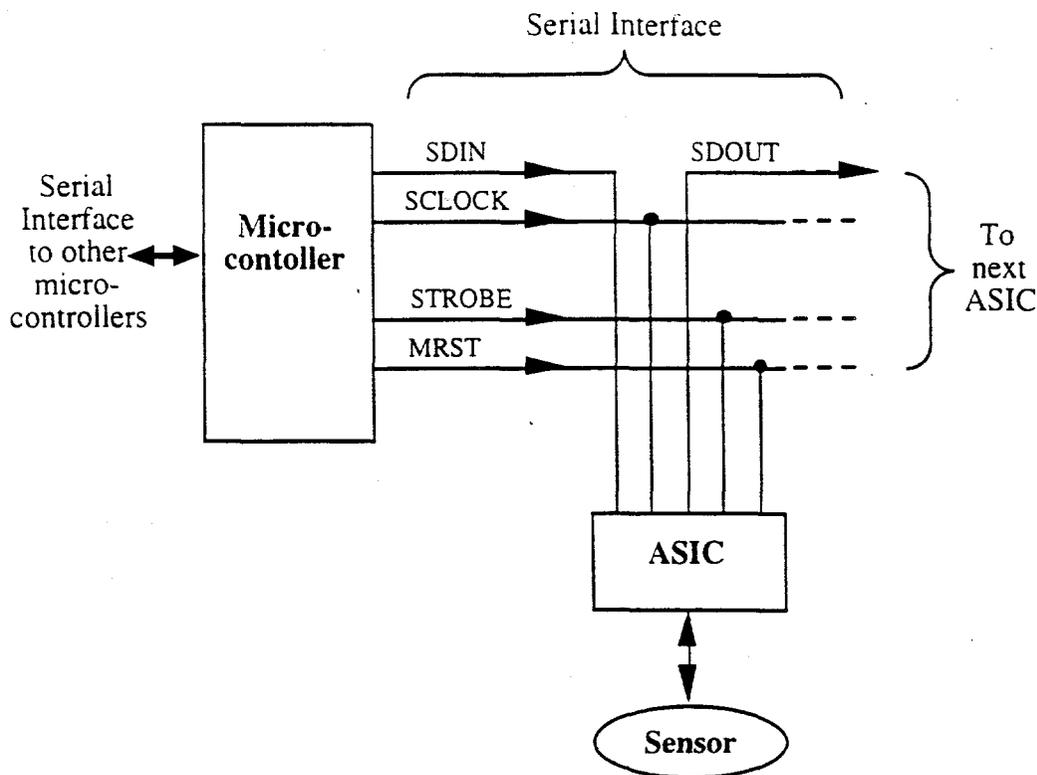


Fig. 4.7. Alternative microcontroller and sensor ASIC communication interface.

The input shift register is divided into three sections -- sensor address, register address, and data. The sensor address is used to identify which of the sensor ASICs is being addressed. This address is locally compared to a reference address (uniquely set for each sensor on the serial bus) and an address enable is asserted upon receipt of the proper address. Five register address bits are implemented allowing for as many as 32 sensor ASICs per serial bus (microcontroller). In some instances improved speed can be obtained by writing some control commands to all ASICs on the serial bus simultaneously. To provide this capability, one address is reserved for a global write which reduces the maximum number of sensor ASICs to 31. The global write address is 0 (0000 in binary). The register address bits (3) are used for selection of the on-chip registers used for sensor ASIC control. Eight registers are possible using 3 address bits, but the actual implementation requires fewer control registers. The data byte of the input shift register contains data that can be loaded into one of these control registers.

A data write is accomplished by initiating the timing sequence detailed in Fig. 4.8. Through the use of the shift clock, two 8-bit data

bytes are shifted globally to the sensor ASIC(s). Within the ASIC, shifting takes place on the falling edge of SCLOCK, so the data (SDIN) must be settled in advance of the falling edge of SCLOCK. As previously mentioned, the first byte contains the data, the second the address bits for the sensor ASIC and selected control register. Within the addressed ASIC, assertion of the STROBE signal transfers data from the input shift register data byte into the selected sensor ASIC control register. The control register is loaded on the falling edge of STROBE for a write operation. All registers used in each of the ASICs can be configured using this procedure.

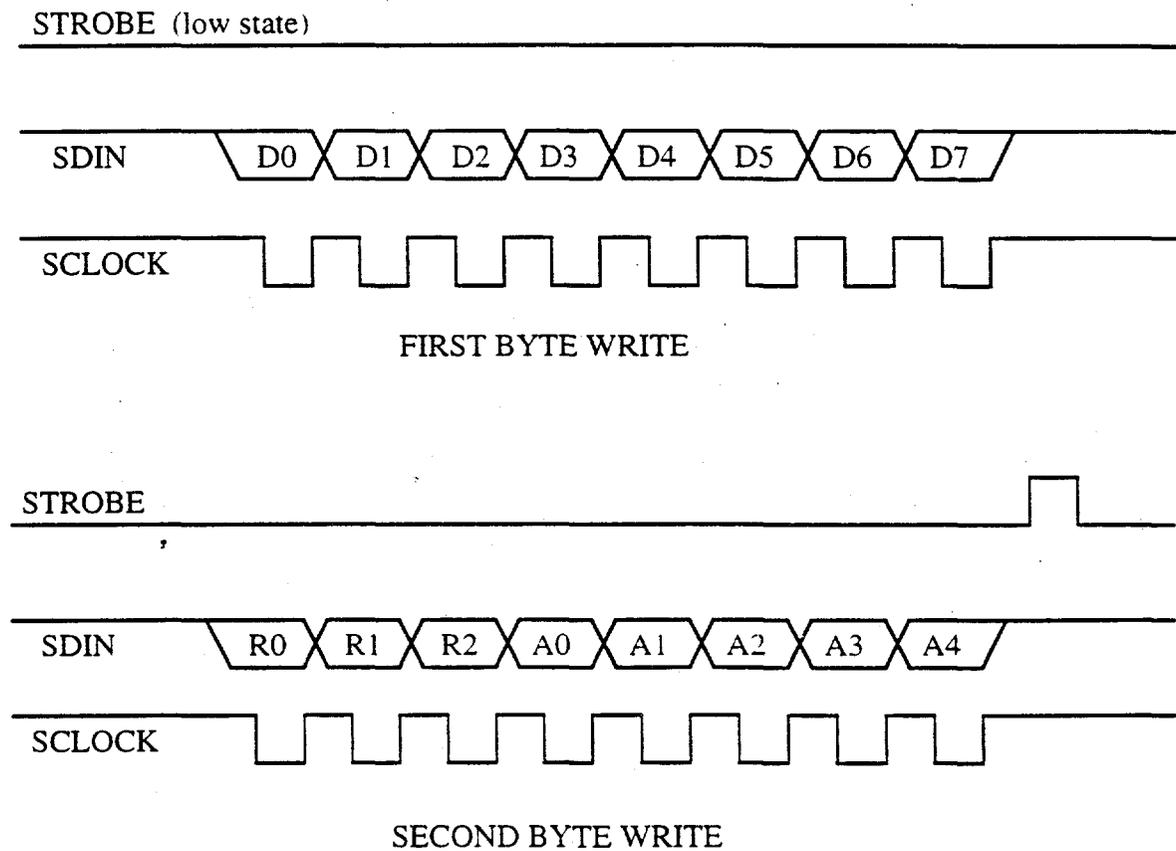


Fig. 4.8. Serial communications timing.

For some control purposes, it will be necessary to supply pulses to the sensor electronics. An addition to the data write process allows the generation of pulses with the same addressing capabilities. As in the data write, two 8-bit data bytes are shifted globally to the sensor ASIC. The address is decoded to produce an enable and the STROBE signal transfers the data into the addressed register. In addition, if the register address is 0, a decoder is enabled which allows passing

the STROBE signal to one of 8 possible outputs which are selected with the lower 3 bits of the data. Thus writing a certain data byte to register 0 will also produce a pulse which can be used to start a process in the ASIC. For example, the pulse could be used to reset a register. The width of this pulse is application dependent. Tables 4.3 and 4.4 show the register assignments and the associated functions.

It is possible to test many of the communication functions of the ASIC and the circuitry communicating with it by writing data bytes to the ASIC and observing the serial data output (SDOUT). If the shift register is functioning properly, the output should be the same as the input, but with a 16 cycle (of SCLOCK) delay. Also, the reset function may be tested by clocking in a non-zero pattern (two bytes), asserting MRST and then clocking in two more bytes. The two bytes that are shifted out should contain all zeroes.

Register	Register	Bit	Signal	Description
000	0	B7-2		not implemented
		B1	STRB1	strobe control bit 1
		B0	STRB0	strobe control bit 0
001	1	B7	FC2	spare (no external connection)
		B6	FC1	spare (no external connection)
		B5	FC0	spare (no external connection)
		B4	S4	envelope thresh digital pot control bit 4
		B3	S3	envelope thresh digital pot control bit 3
		B2	S2	envelope thresh digital pot control bit 2
		B1	S1	envelope thresh digital pot control bit 1
		B0	S0	envelope thresh digital pot control bit 0
010	2	B7	COMP_OE	comparator mux output enable
		B6	GC1	programmable amp gain control bit 1
		B5	GC0	programmable amp gain control bit 0
		B4	S4	pulse thresh digital pot control bit 4
		B3	S3	pulse thresh digital pot control bit 3
		B2	S2	pulse thresh digital pot control bit 2
		B1	S1	pulse thresh digital pot control bit 1
		B0	S0	pulse thresh digital pot control bit 0

Table 4.3 Input and control register definitions.

STRB1-0 Code	Strobe Name	Description of Strobe
11	(none)	not used
10	RSTO	output register reset strobe
01	T1B	spare (no external connection)
00	T0	spare (no external connection)

Table 4.4 Control strobe definitions.

Appendix A

Summary of LED/Detector Testing

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April 4, 1995
John Halliwell
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Summary of LED/Detector Testing for Merrit CRADA

A number of LED's and PIN photodiode detectors were tested to evaluate their performance in a simple position detection scheme. A test set up as shown in Figure 1 was used to maintain constant test conditions. Each LED emitter was evaluated with each PIN photodiode detector and a matrix of performance data was obtained for a fixed distance test target. The best pair was then tested to look at performance versus distance to a 6" x 9" target using a setup as shown in Figure 2. The LED/Detector pair used by Merrit on their evaluation board was also tested for reference. A final test involved swinging the 6" x 9" target angle to look at beam width of the light source.

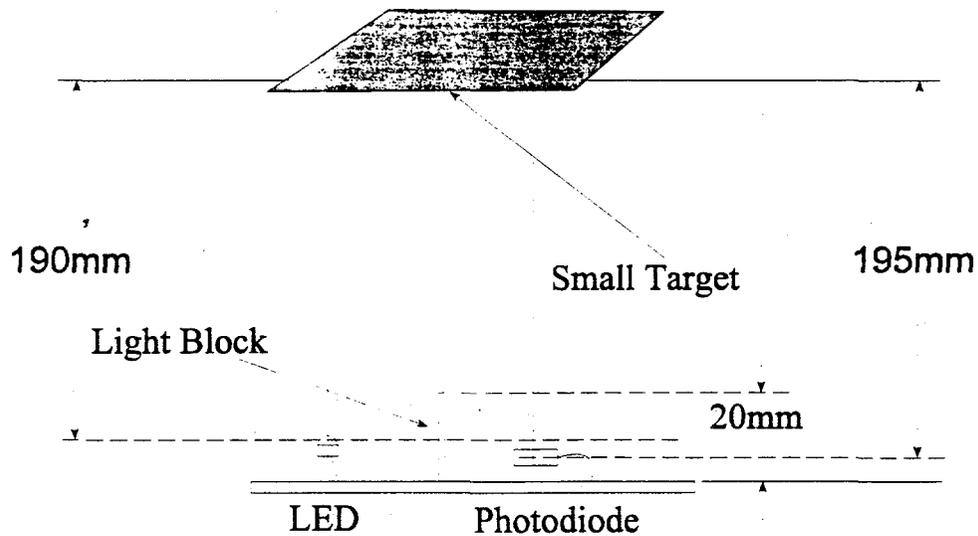


Figure 1 LED/ Photodiode Test Configuration.

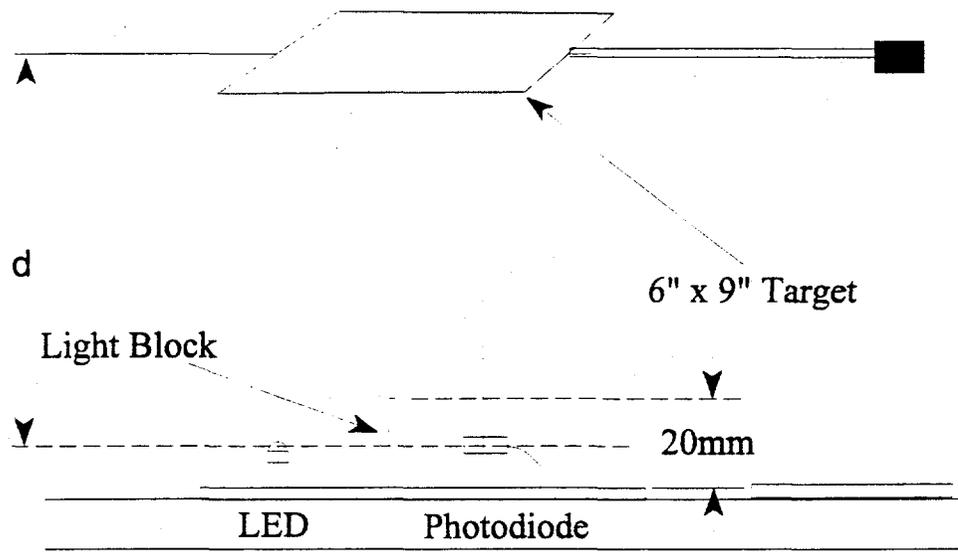


Figure 2 LED/ Photodiode Test Configuration with Variable Height (d) 6" x 9" Target.

Table 1 lists the devices tested and their respective manufacturers. Note that the table also lists the emission peak for the LEDs and the detection peak for the photodiodes. All of the devices tested (except the components provided by Merrit) are available from Digikey Electronics.

Table 1. LED/Detector Devices Tested.

Device Number	Manufacturer	Description
LN66R	Panasonic	IR LED, 950nm peak
LN175	Panasonic	IR LED, 900nm peak
PN323B	Panasonic	PIN Photodiode, 960nm peak
PN334	Panasonic	PIN Photodiode, 900nm peak
LTR-516AD	Lite-On	PIN Photodiode, 940nm peak
LTE-5228A	Lite-On	IR LED, 940nm peak
LTE-4228U	Lite-On	IR LED, 940nm peak
1N6266	Quality Tech. Semi	IR LED, 940nm peak
OD-100	Opto Diode Corp.	IR LED, 880nm peak
SFH-205	Siemens	PIN Photodiode, 950 nm peak

Table 2 lists the data matrix for the evaluated LED/Photodiodes. Data sheets for the components (where available) are attached at the end of this document. The LTE-5228/LTR-516AD pair outperformed all other LED/Detector pairs. The SFH-205 provided by Merrit performed nearly as well as the LTR-516AD. The slight difference in response may be due to the difference in peak sensitivity wavelengths. The OD-100 emission peak is lower in wavelength than any of the other emitters tested and was not well matched to the LTR-516AD or the SFH-205. The PN334 which was the best spectral match to the OD-100 was the poorest performing detector. Note that these tests were performed using a limited number of devices and so do not represent a statistical sampling of devices. Several LTR-516ADs were tested. Each performed at nearly the same level for the same test conditions.

Table 2. LED/Detector Device Performance Matrix.

Data taken with Tektronix scope, 64 averages, Rms signal values shown in millivolts, 50% duty cycle @ 50kHz, 100 mA LED drive, all data at same distance to target (approximately 8 inches). No signal voltage at detector = 0.4 mV.

LED \ Detector >	PN323	SFH-205	LTR-516	PN334
OD-100	2.0	3.9	2.9	1.6
LN175	1.8	2.4	2.3	1.5
LN66	5.8	8.3	9.0	2.0
LTE-5228	5.9	9.5	10.2	2.0
LTE-4228	5.9	7.6	8.1	1.9
1N6266	3.7	4.4	4.7	1.7

Figure 3 shows a plot of the signal versus distance for the test set up shown in Figure 1. Data for the Merrit OD-100 LED and the LTE-5228 are compared using the LTR-516AD detector.

Figure 4 shows the data for signal strength versus target angle. Note that this measurement is heavily influenced by the target size.

A schematic of the circuits used is shown in Figure 5. The signal from the LED detector was amplified by a simple op-amp pre-amp circuit. The LED drive was set to 100 mA for each LED under test. Note that the OD-100 can be operated at much higher current than any of the other LEDs tested. In applications where the higher current is not a problem, the OD-100 may perform better than the LTE-5228 (which is limited to 100 mA of drive current). All of the LEDs and detectors purchased cost around \$1 each in small quantities (except the 1N6266 which was \$4). Pricing for the Merrit provided LED/Detector was not investigated.

Input to the LED driver was controlled with a Hewlett-Packard pulse generator producing a 50kHz, 50% duty cycle pulse train. The pre-amp output was monitored on a digitizing scope set to compute the RMS signal value after 256 averages.

Response to 6 X 9 Inch Target

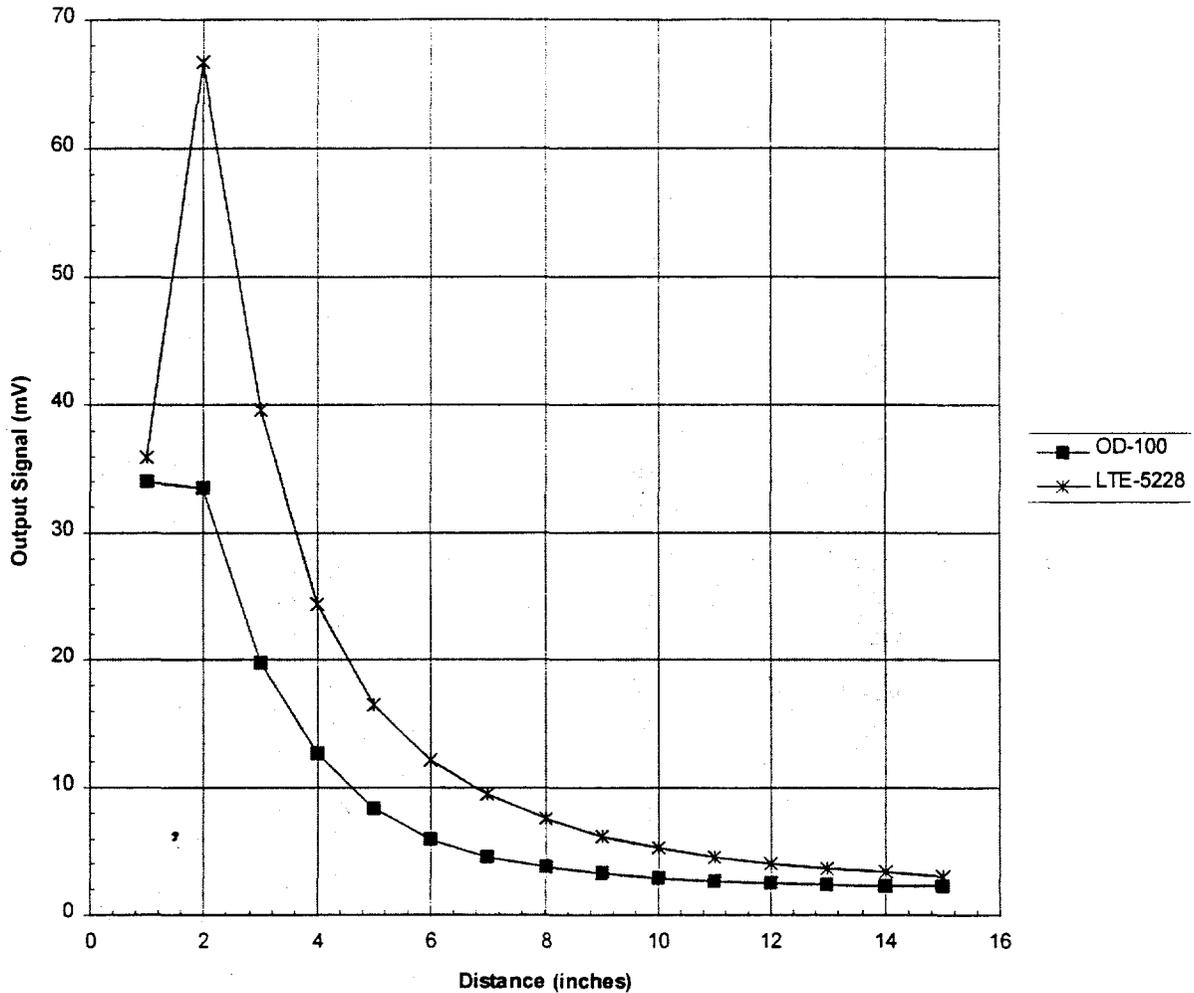


Figure 3. Signal Strength vs. Distance for the OD-100 and the LTR-5228 using an LTR-516 PIN Photodiode detector.

In addition, an infrared sensitive video camera was used to qualitatively evaluate the Merrit LED and the LTE-5228 LED (found to be the best performer of the tested devices) for comparison. The Merrit LED (OD-100) produced a less intense direct beam of light, but emitted light over a much broader area. The LTE-5228 produced a narrow beam which illuminated a several inch diameter area at a distance of 12 inches. At this same distance the OD-100 produced a less intense but more uniform illumination over a much wider area. For the 6 X 9 inch target the LTE-5228 produced a noticeable bright spot on the target, while the OD-100 uniformly illuminated the target

Response to 6 X 9 Inch Target versus Angle

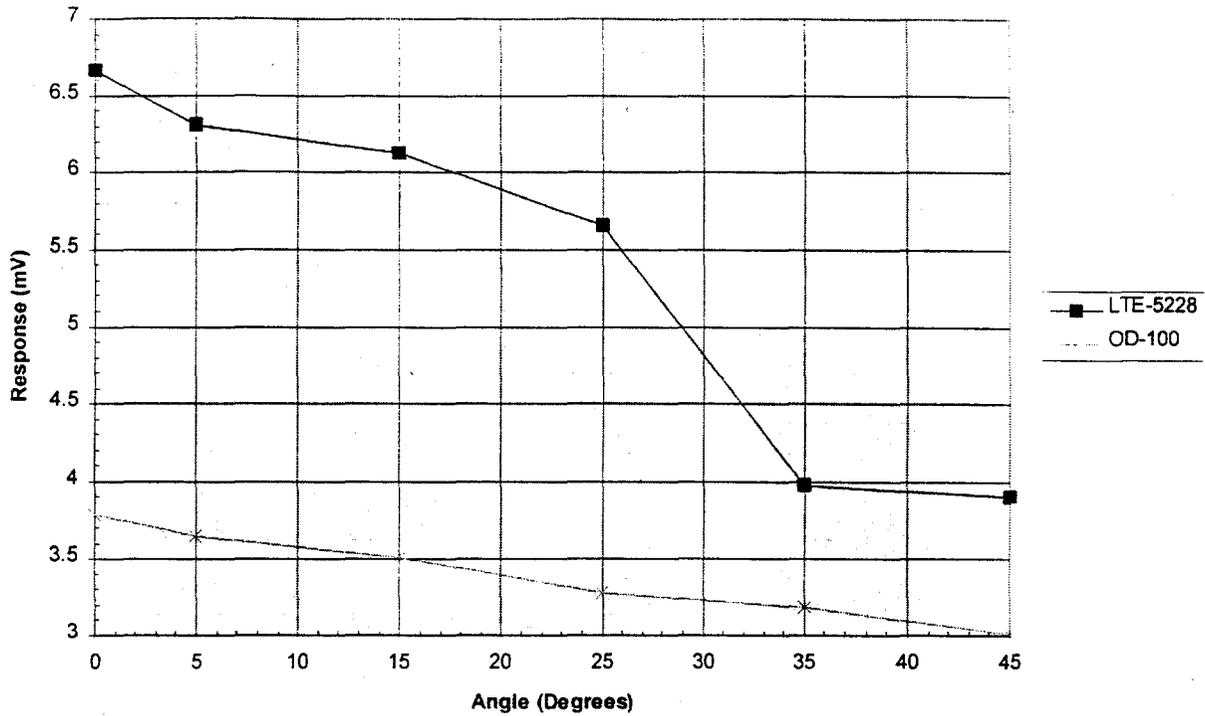


Figure 4 Signal Strength vs. Target Angle for the OD-100 and the LTR-5228 using an LTR-516 PIN Photodiode detector.

at a range of roughly 2 feet. Given the power rating and construction of the OD-100 it is likely much more expensive than the LTE-5228. Multiple LTE-5228 LEDs could be used to illuminate a broad area.

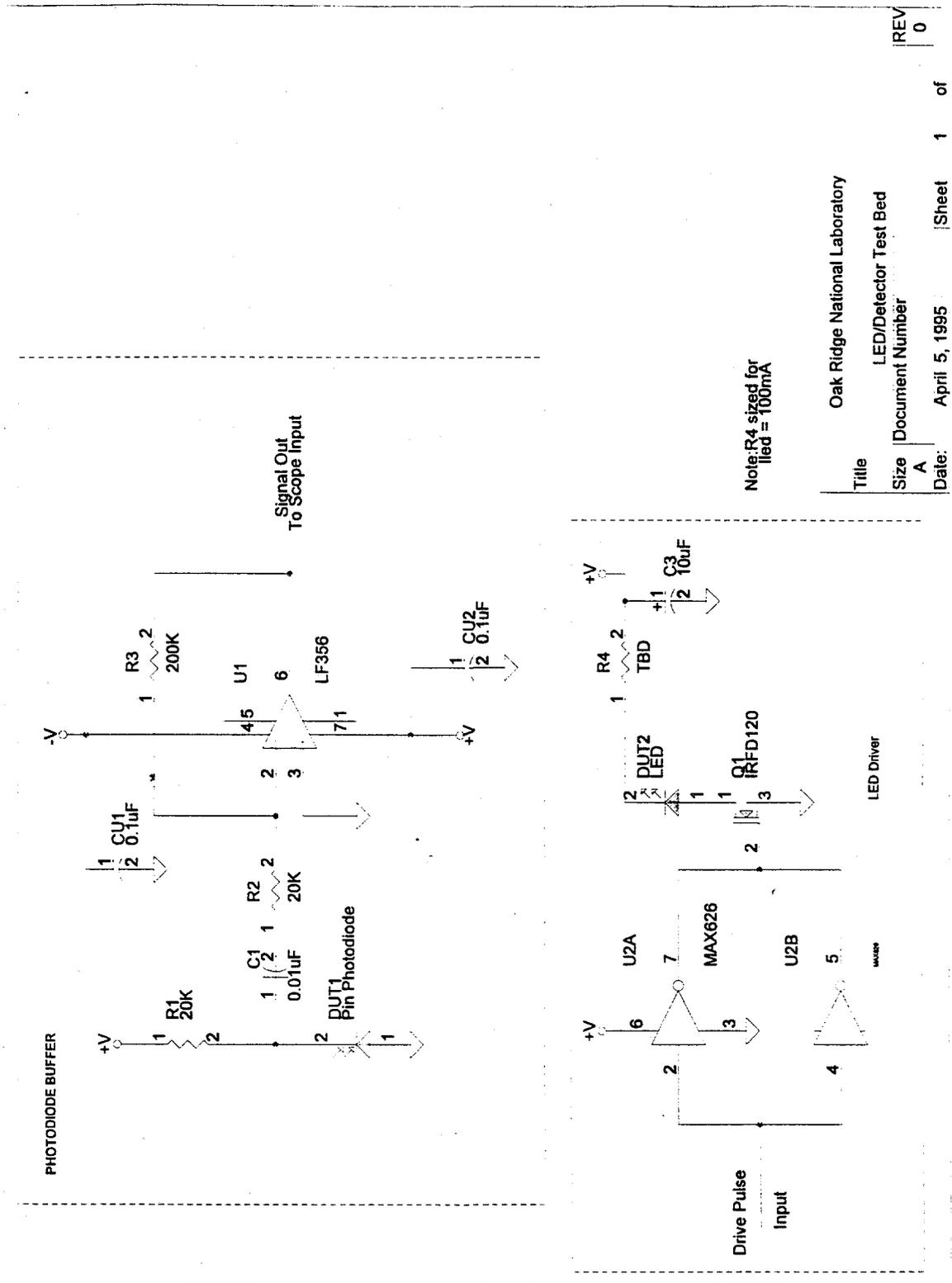


Figure 5. Test Circuit Schematic.

5.0 System Integration and Testing

System integration and testing proceeded in two phases. The IR and acoustic proximity sensor ASICs were first tested for functionality at ORNL. After passing these preliminary test, they were integrated into an MSI sensing system and further tests were conducted at MSI.

5.1 Preliminary tests at ORNL

Upon receipt of the IR and Acoustic proximity sensor ASICs, test fixtures resembling Figs. 5.3 and 5.6 were constructed to allow functional testing of the ASIC designs. Since the serial interface used by these ASICs is very similar to that used by the capacitive sensor ASIC (Sensornode4c), it was relatively simple to modify the cables originally intended to connect a bracelet processor to a capacitive sensor node so that either the IR or Acoustic sensor test fixture could be connected to a bracelet processor of the type described in ORNL TM/12969. The needed connections are shown in Table 5.1.

Bracelet Processor Pin No.	Signal Name	Signal Description	Connect through	Test board signal name	Test board Pin No.
1	SDIN	serial data	yes	SD_IN	1
2	SCLK	shift clock	yes	SCLK_IN	2
3	WR/RDB	read/write control	yes (not needed)	NC	3
4	STROBE	strobe	yes	STROBE_IN	4
5	MRST	reset	yes	MRST_IN	5
6	CLOCK	timebase	no	20MHz_IN (IR) or DRV (acoustic)	6
7	+5V	+5V supply	yes	+5V	7
8	-5V	-5V supply	yes (not needed)	NC	8
9	GND	ground	yes	GROUND	9
10	NC	no connect	no	ADC (IR) uPORT (acoustic)	10

Table 5.1. Connections between bracelet processor and proximity sensor ASICs used for functional tests.

For the IR proximity sensor ASIC, the 20-MHz timebase was supplied by the oscillator on the test fixtures, and the other control signals and power were supplied by the bracelet processor which was in turn connected to a pc running the "host" program. The direct communications option of the "host" program was used to set the appropriate bits in the registers of the ASIC. This option allows control of the individual bits in any register and, unlike many of the other functions of the "host" program, is not specifically tailored to the needs of the Sensornode4c ASIC. Since the IR proximity sensor ASIC produces an analog output that is converted to digital by the ADC built into the PIC microcontroller, the output was viewed using an oscilloscope for the functional tests. This also allowed examination of intermediate outputs and test points. Fig. 5.1 shows a block diagram of the functional test setup.

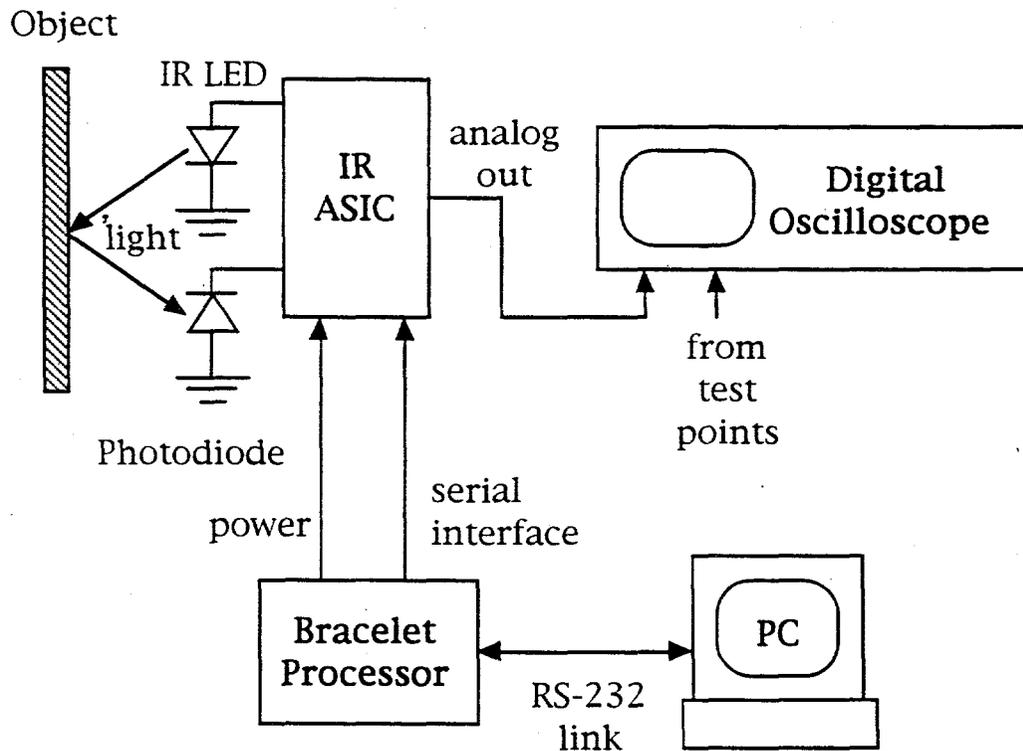


Fig. 5.1. Functional test setup for IR proximity sensor ASIC.

The test setup was used to verify that the IR proximity sensor A worked as designed. For example, the oscillator was programme

operate at different frequencies and those frequencies were verified to be correct. Also the various gains were measured, and the function of the demodulator, the offset DAC and the output multiplexer were checked and found to be operational. Finally, a set of conditions was determined by trial and error to give reasonable proximity sensing capability. This setup required writing 7F(hex) to register 1, 3F(hex) to register 2 and 01(hex) to register 3 followed by writing 01(hex) to register 0. The register 1 values set the oscillator to 26.4 kHz and the second programmable gain amplifier (PGA) to x8, while the register 2 values set the first PGA to x2 and the digital offset potentiometer to one extreme. The register 3 value turns on the output multiplexer and the value written to register 0 resets the oscillator (assuring it oscillates at the desired frequency.)

For the acoustic proximity sensor ASIC, a similar setup (Fig. 5.2) was used. The bracelet processor and the "host" program were used to set up the ASIC, while the burst of pulses (for driving the acoustic transducer) that the PIC microcontroller would normally supply, were supplied by a pulse generator. The output of the PGA or the pulse comparator were observed on the oscilloscope along with the output of the burst envelope comparator. The oscilloscope was triggered by the pulse generator. When the circuit is adjusted properly, the time between the trigger signal and the change of the output state of the burst envelope comparator is the delay between the emitted burst of ultrasound and the return of the reflection or, in other words, the time-of-flight of the sound traveling approximately twice the distance from the sensor to the target.

The test setup was used to verify that the acoustic proximity sensor ASIC worked as designed. Many parts of the circuit are very similar to those used in the IR ASIC, so the testing followed similar lines. Gains, offsets and other functions were measured. The drive buffer and bandpass filter were found to work as designed.

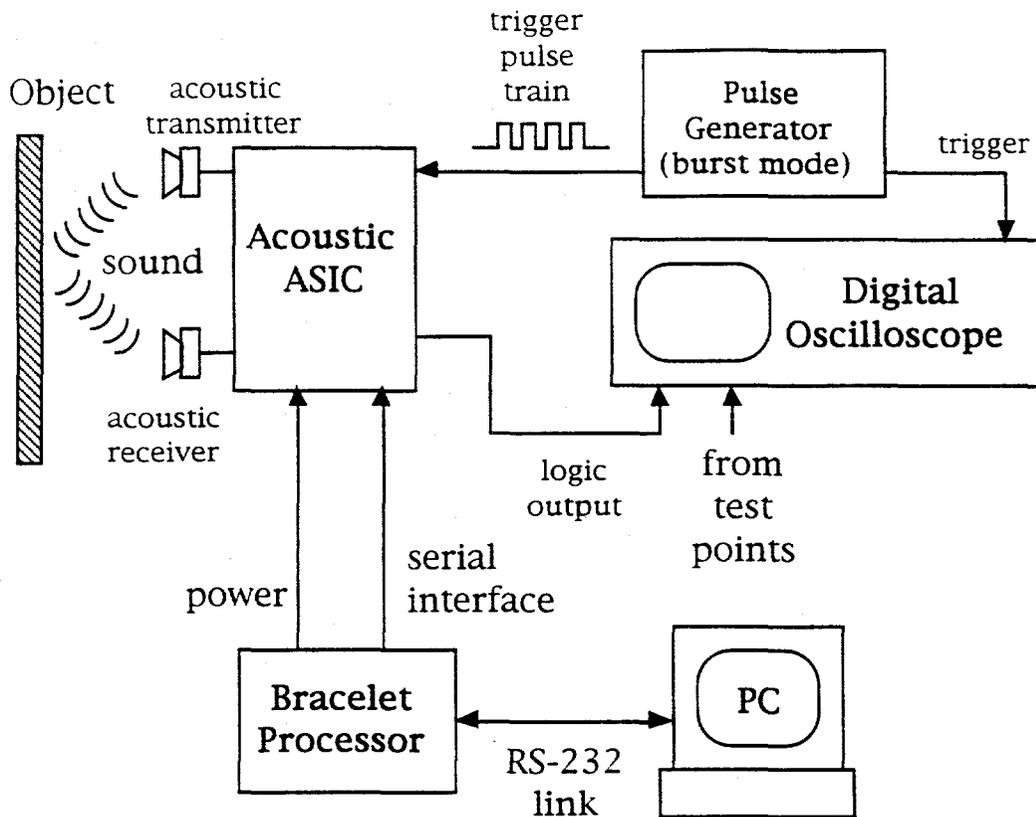


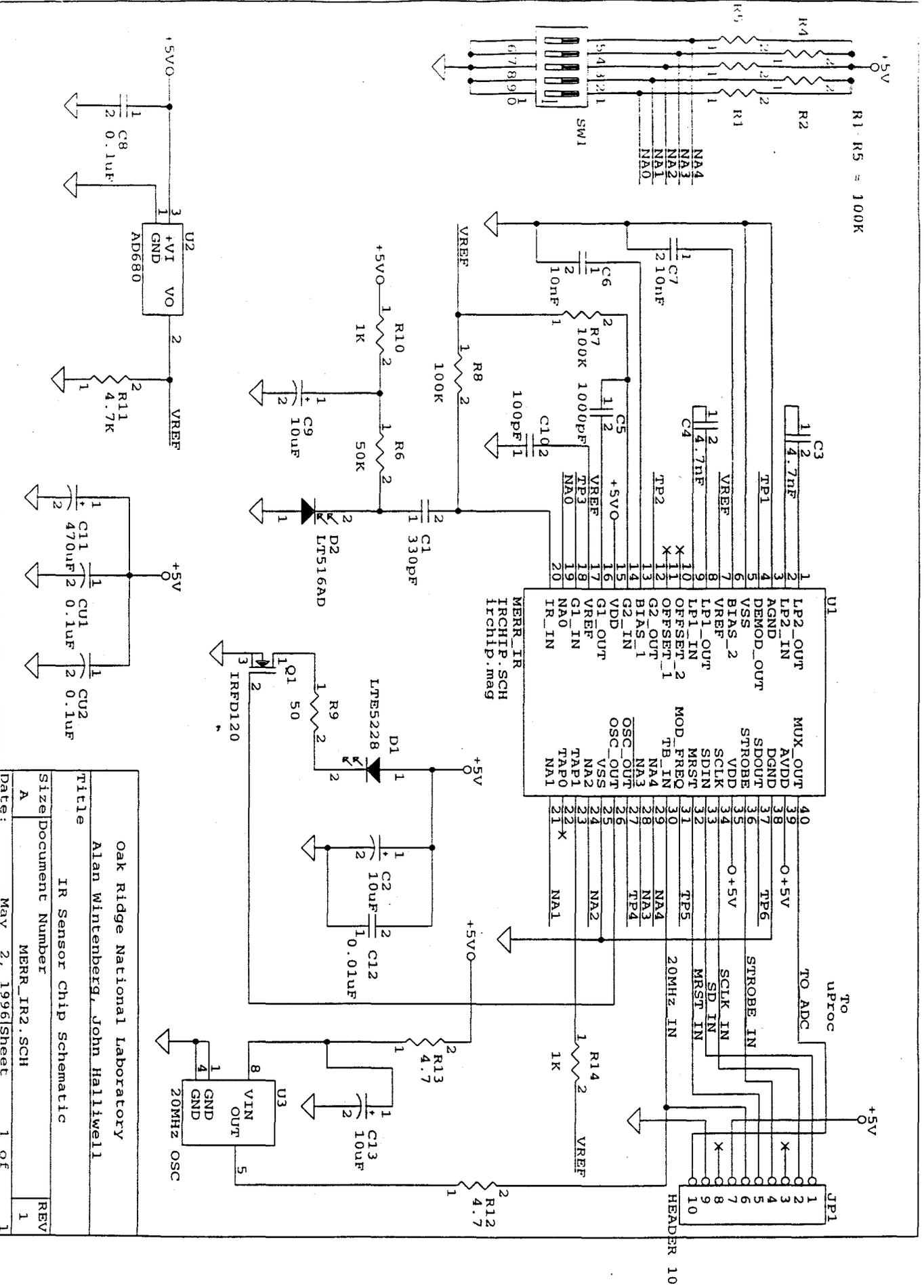
Fig. 5.2. Functional test setup for acoustic proximity sensor ASIC.

5.2 IR Proximity Sensor ASIC Integration and Testing

An IR sensor unit based upon the functional test fixture design was developed and several copies were fabricated. A schematic of the unit is shown in Fig. 5.3. Such a sensor unit was incorporated into an MSI sensor system as shown in Fig. 5.4. As in the functional tests at ORNL, the IR proximity sensor ASIC excited the IR LED and processed the signal detected by the IR photodiode. Setup was accomplished by using the serial interface previously agreed. The actual implementation was a serial download board developed by MSI. (Eventually this function should be incorporated into the microcontroller.) The analog output of the IR ASIC was processed by an MSI IR module modified to allow access to the ADC built into the microcontroller. This module was plugged into an MSI sensing network (Sensor Skin copyright) that also included un-modified IR modules. This network was controlled and the proximity data monitored by a MSI software running on a PC.

IR sensor unit schematic

Figure 5.3



Oak Ridge National Laboratory	
Alan Wintenberg, John Halliwell	
Title IR Sensor Chip Schematic	
Size	Document Number
A	MERR_IR2.SCH
Date:	MAY 2, 1996 Sheet 1 of 1
REV	1

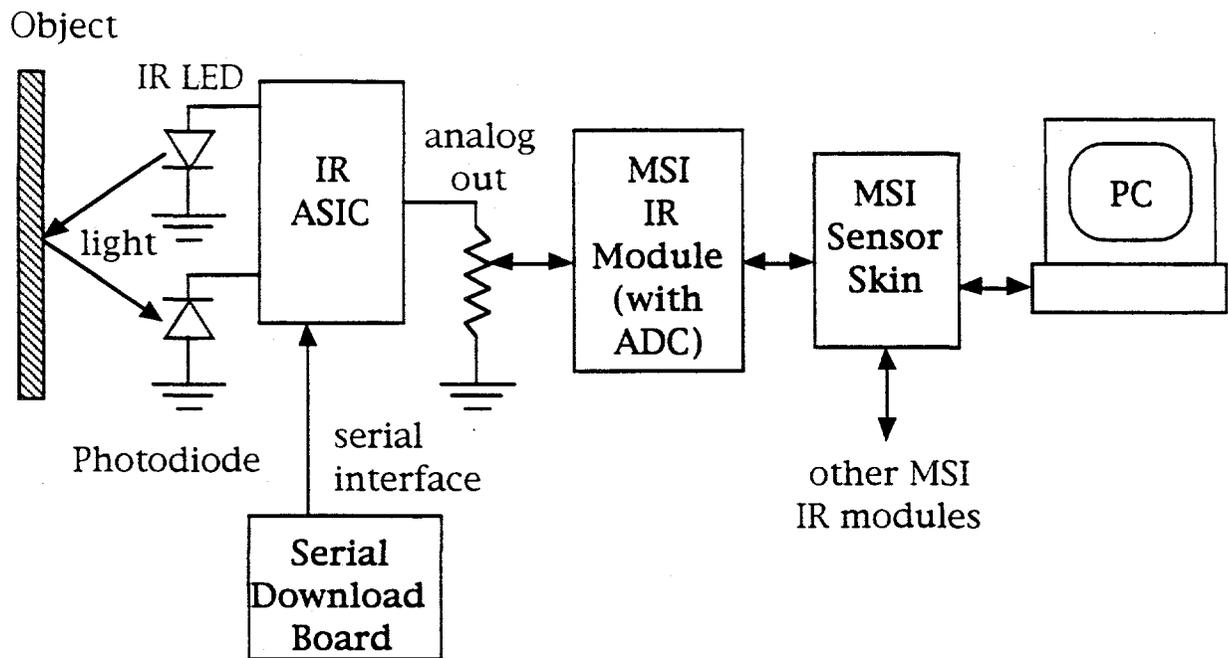


Fig. 5.4. Final test setup for IR proximity sensor ASIC.

The sensor using the IR proximity sensor ASIC performed very well. Using control settings of 7F(hex) for register 1, 5F(hex) for register 2 and 01(hex) for register 3, an 8 inch by 10 inch white poster board target could be detected at distances up to 30 inches. (These register values set the oscillator to 26.4 kHz, the first PGA to x4, the second PGA to x8, and the digital offset potentiometer to one extreme.) A plot of the sensor response is shown in Fig. 5.5.

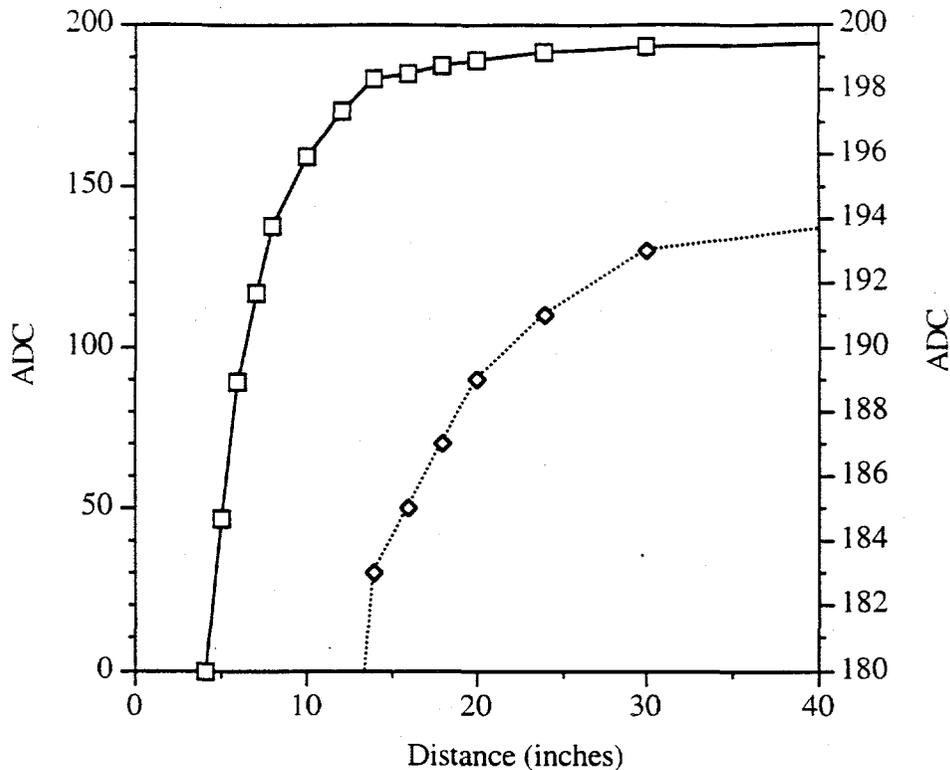


Fig. 5.5. IR sensor response for poster board target.

5.3 Acoustic Proximity Sensor ASIC Integration and Testing

An acoustic sensor unit based upon the functional test fixture design was developed and several copies were fabricated. A schematic of the unit is shown in Fig. 5.6. Such a sensor unit was incorporated into an MSI sensor system as shown in Fig. 5.7. A modified MSI acoustic module was used to produce a logic-level pulse train which was amplified by the acoustic proximity sensor ASIC and used to drive the acoustic transmitter. The ASIC processed the signal detected by the acoustic receiver and upon detecting an echo, produced a pulse which was used by the MSI acoustic module as the stop for the time-of-flight measurement. As for the IR sensor tests, the setup was accomplished by using the serial download board developed by MSI. This modified acoustic module was also plugged into an MSI sensing network (Sensor Skin copyright) that also included un-modified acoustic and IR modules. This network was controlled and the proximity data monitored by a MSI software running on a PC.

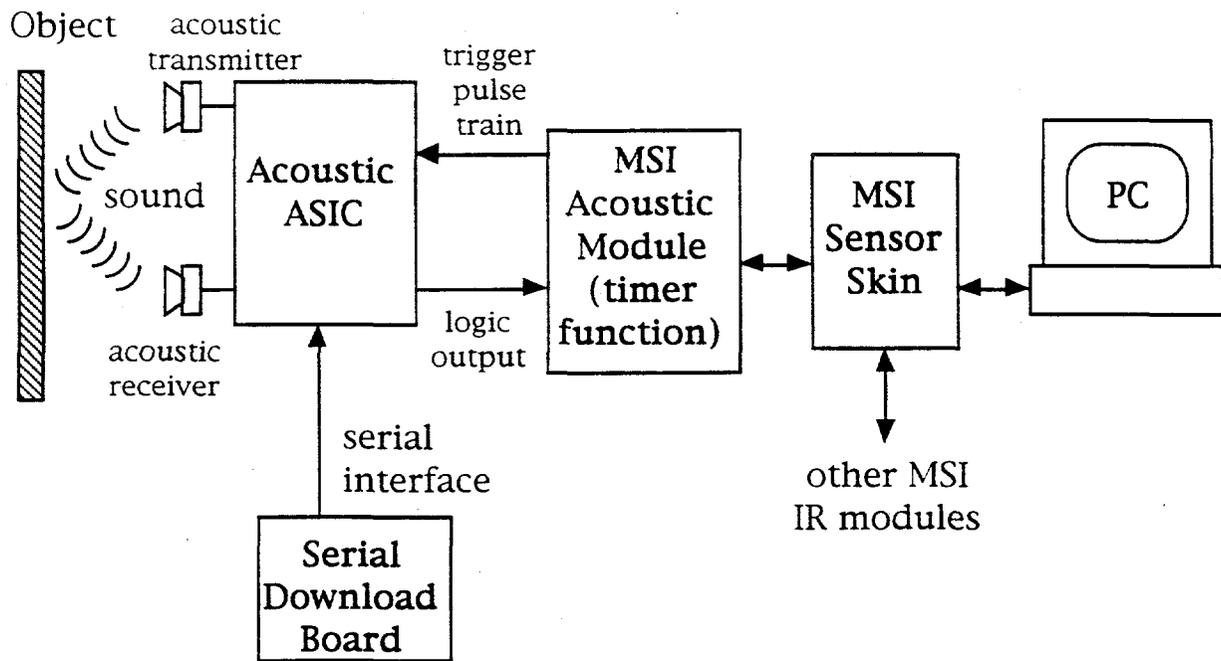


Fig. 5.7. Final test setup for acoustic proximity sensor ASIC.

The sensor using the acoustic proximity sensor ASIC performed even better than the IR proximity sensor. Using control settings of 0F(hex) for register 1, and 83(hex) for register 2, the same 8 inch by 10 inch white poster board target previously used could be detected at distances greater than 48 inches. (These register values set the burst threshold to approximately half scale, the PGA to x1, and the pulse threshold to a moderately low value.) A plot of the sensor response is shown in Fig. 5.8. The timebase used for the timer was adjusted so that 100 counts corresponds to a target 10 inches from the sensor. Thus each count corresponds to 0.1 inch. Since the timer maximum value is 255, the modified acoustic module could only report distances up to 25.5 inches, but observation of the output of the acoustic proximity sensor ASIC using an oscilloscope revealed correct sensing at distances greater than 48 inches.

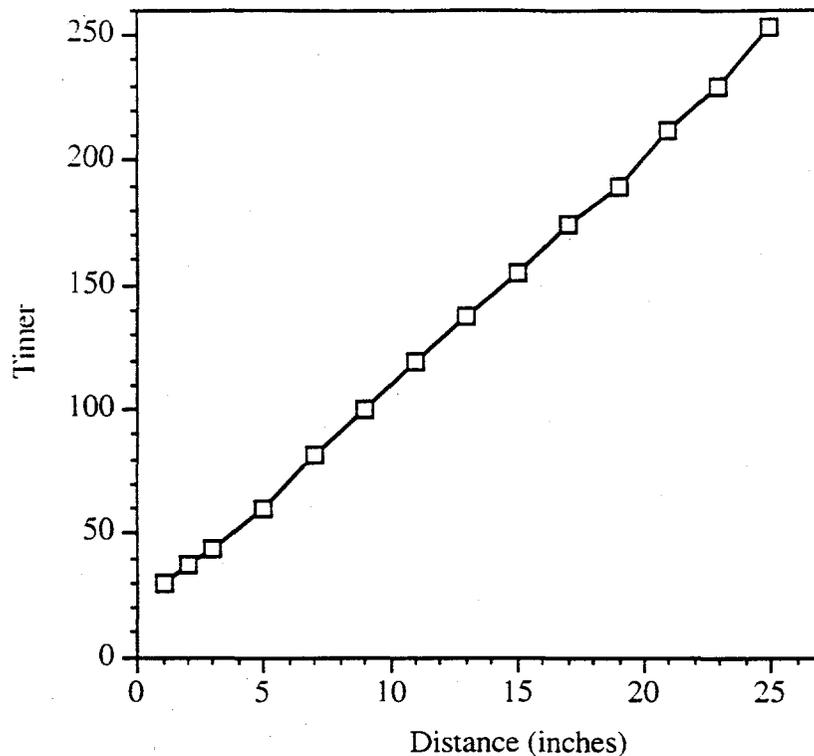


Fig. 5.8. Acoustic sensor response for poster board target.

Close examination of Fig. 5.8 reveals that the response is not linear at small distances. Since the timer actually measures flight time from the acoustic transmitter to the receiver, a correction is needed due to the distance between the transmitter and the receiver. As shown in Fig. 5.9, the distance the sound travels is actually slightly more than the distance to the target. By taking the timer reading and making a trigonometric correction, a more accurate estimate of the target distance is obtained. This result is shown in Fig. 5.10. Obviously, the correction becomes negligible as the target distance becomes large, and the path length approaches twice the normal distance.

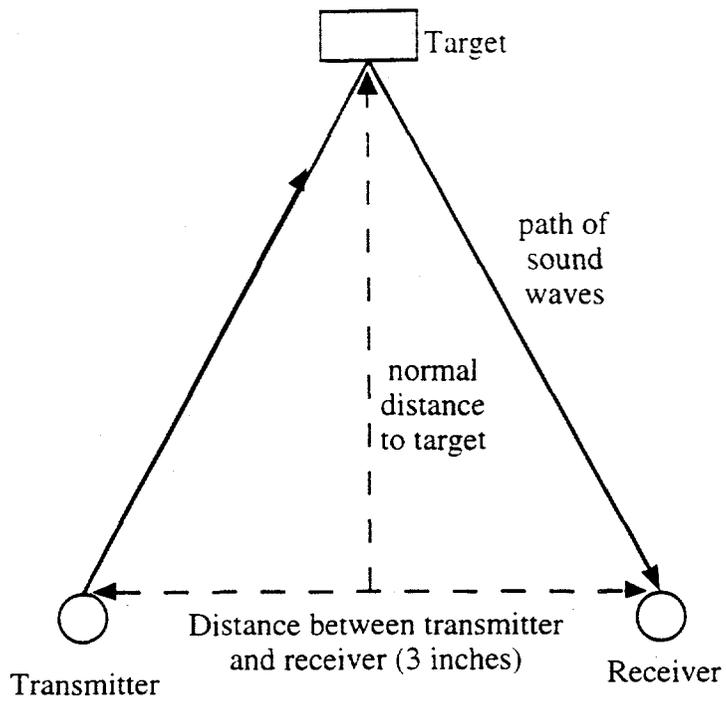


Fig. 5.9. Acoustic sensor transmitter, target and receiver geometry.

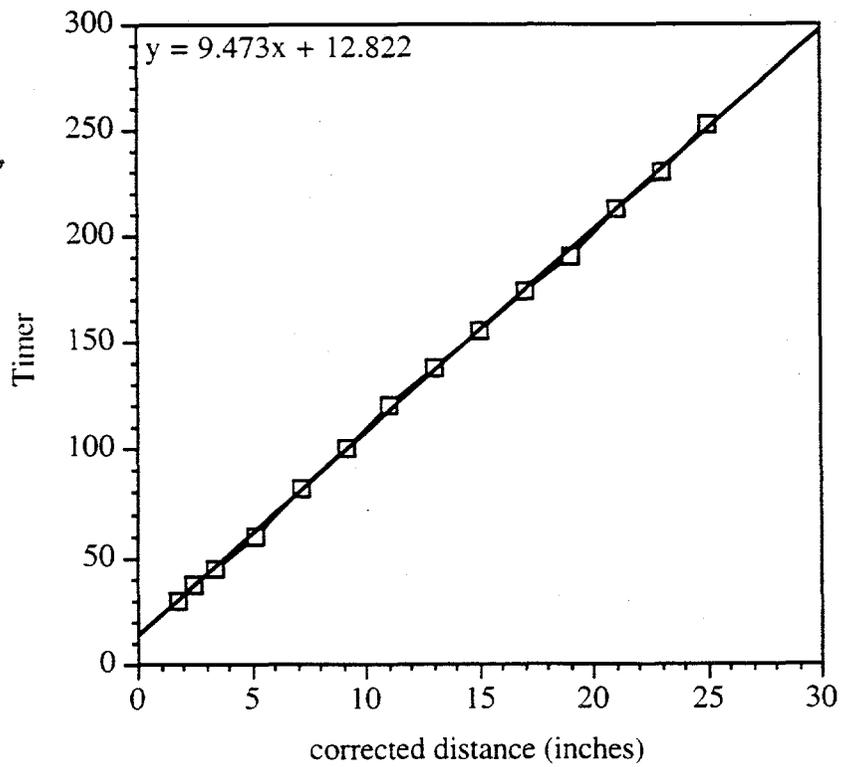


Fig. 5.10. Corrected acoustic sensor response.

Appendix B

Summary of LED/Detector with the Sensornode ASIC

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April 10, 1995
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Integration of LED/Detector with the Sensornode ASIC (for Merrit CRADA)

In order to integrate an IR LED/Detector pair with the Sensornode ASIC some basic testing was done. First, the photodiode sensitivity was studied, and second, tests were run with the Sensornode ASIC using the best LED/Detector pair from previous testing (LTE-5228A LED/ LT-516AD photodiode).

It is expected that any given LED/Detector pair will have a fixed basic sensitivity curve (which represents photodiode current as a function of IR illumination) as shown in Figure 1. This curve represents a case where the front end electronics of the Sensornode ASIC and the A/D that follows add no noise to the system. Range of the detection system will actually be limited by three factors. First, as shown in Figure 1 the basic noise of the detector limits signal sensing (minimum signal conditions). Second, background noise (ambient IR sources) may limit range. Third, system dynamic range (wether at the photodiode or in the signal processing electronics) will limit the sensor's use to a predetermined set of distances.

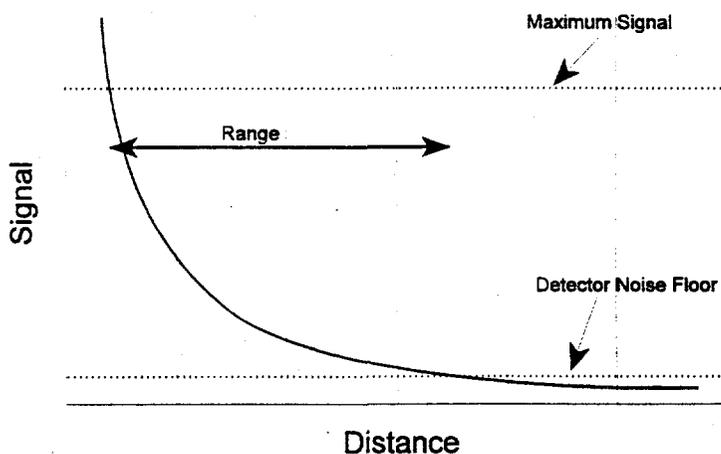


Figure 1. Photodiode response vesus distance.

The detector noise floor is determined by the photodiode noise and the system

impedance at the photodiode. A number of things can be done to minimize the impact of the noise including lowering the system impedances, choosing the quietest photodiode available, and bandlimiting the signal processing path to lower the noise contribution. Bandlimiting is very effective in this application since the IR light source of interest is operated in a pulsed mode at a specific frequency.

Background IR will be emitted by a number of light sources including solar, incandescent (lamps, flashlights, etc...), and fluorescent lamps. Proper optical filtering to limit the photodiode response to a narrow bandwidth of light in the IR spectrum will help but does not eliminate the background problem. Bench testing showed that even overhead fluorescent lighting emitted some IR.

Dynamic range comes into play in two ways. First, it limits the range over which the detector can be used if system gains are fixed. Second, background light sources can saturate the photodiode or amplifiers which follow the photodiode. Many light sources contain IR energy that is either steady state (DC) or very low in frequency (60, 120, 180 Hz, ...). This will be discussed further in the following paragraphs.

Figure 2 shows the basic bias scheme for a photodiode operated in a current source mode. Light impinging on the detector causes a current, I_{led} , to flow through the reverse biased photodiode. This in turn increases the voltage drop across R_b . This voltage change is then coupled to the signal processing circuitry. For the circuit of Figure 2, the diode has a dynamic range of $+V$ volts. Table 1 shows the maximum photodiode current for several values of R_b with $+V = 10$ volts. Even though the photodiode can be AC coupled to the signal processing circuitry, this does not prevent an IR light source from saturating the photodiode. If sufficient IR energy is directed at the photodiode not only will the voltage across the photodiode

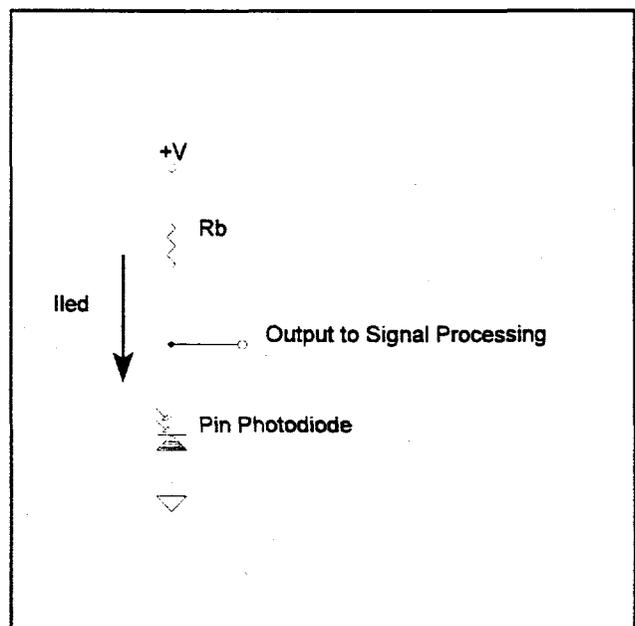


Figure 2. Typical Photodiode bias circuit.

approach zero volts but it will operate in the photovoltaic mode and produce a voltage opposite that of the reverse bias. Table 2 shows the currents measured in an LT516AD photodiode for several conditions with R_b equal to 499Kohms. Table 3 shows the response for R_b equal to 10Kohms. Note that the photodiode was saturated by a flashlight at 2 feet or an incandescent bulb at 3 feet for R_b equal to 499Kohms.

Table 1. Maximum photodiode current for various values of Rb.

Rb (ohms)	Iled max (uA)
10K	1000
49.9K	200
200K	50
499K	20

Table 2. Photodiode current for different light sources, Rb = 499K (using LT516AD photodiode).

Conditions	Vin (volts)	Vled (volts)	LED Current (uA)
No light	10.07	9.58	0.97
Room light	10.04	9.51	1.06
Flashlight @ 2ft	10.03	-0.37	20.9 (photovoltaic)
100W incandescent bulb @ 3ft	10.03	0.00	20.1 (saturated)

Table 3. Photodiode current for different light sources, Rb = 10K (using LT516AD photodiode).

Conditions	Vin	Vled	LED Current (uA)
Room light	10.03	10.02	1.10
Flashlight @ 2ft	10.03	8.88	115

In order for the photodiode bias to remain unsaturated for large amounts of IR energy, Rb must be made progressively smaller. While this does lower the noise floor of the photodiode bias circuit and improve its time response (faster rise and fall times) it reduces the amount of voltage swing seen by the signal processing electronics. The tradeoff is to make Rb large enough to provide sufficient signal to the ASIC while making Rb small enough to prevent bias saturation for high level IR sources.

The LED drive circuit and photodiode bias circuit used to interface the IR pair to the Sensornode ASIC are shown in Figure 3. The LED drive was set at roughly 100mA. It was found that even at the 100mA drive level, effort must be made to prevent capacitive coupling of signal directly from the LED to the photodiode. Careful grounding and shielding of both the LED and the photodiode are needed to allow detection of the small signals present for distant objects. The photodiode is AC coupled to the sensornode ASIC with a high pass cutoff of roughly 4kHz. This was done to remove any low frequency noise from the photodiode's output. The bias

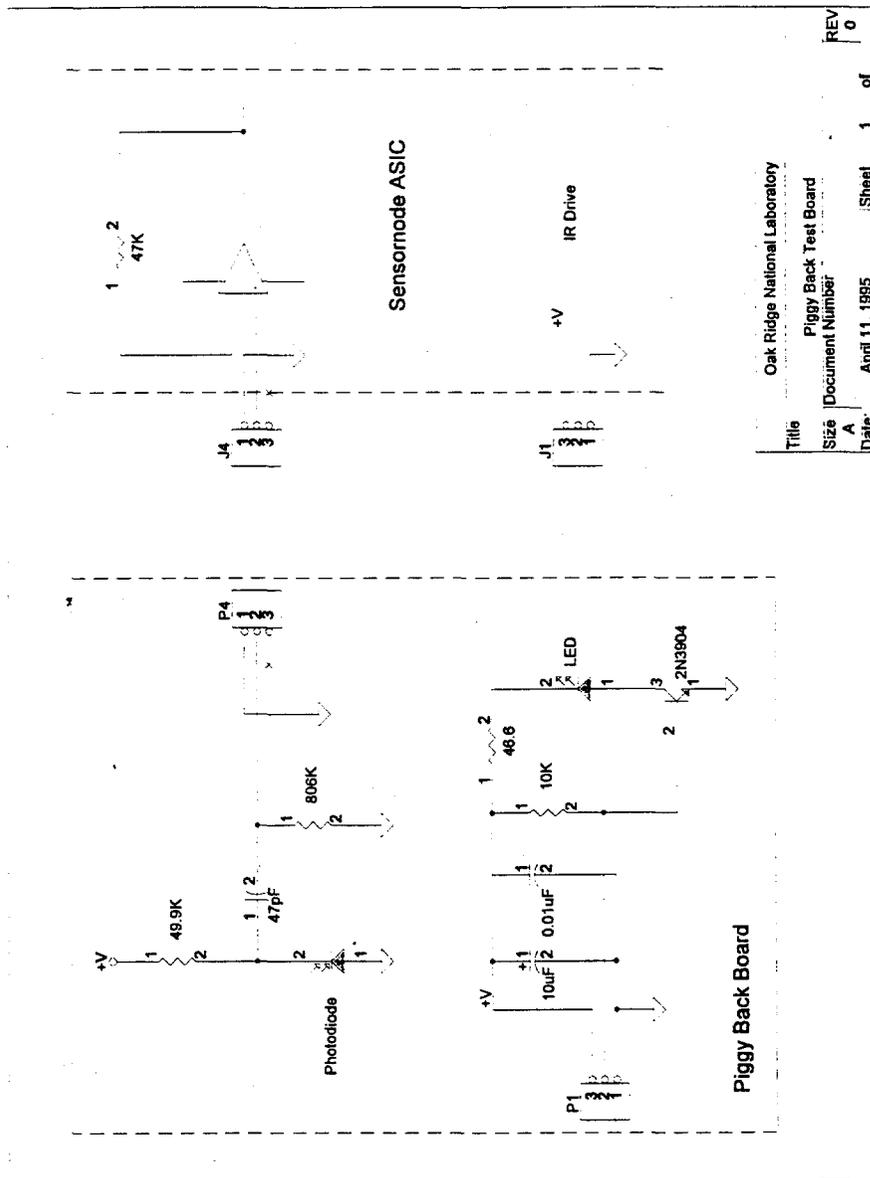


Figure 3. Schematic of Piggy Back Interface Board.

resistor for the photodiode was set at 49.9K. This will allow operation at a current of up

to 100uA without saturation (for a 5 volt bias supply). If operation is required in close proximity to incandescent lighting then the bias resistor would have to be made smaller (reducing sensing distance).

Response curves were measured using the sensornode ASIC for three sets of setup parameters. All tests were run with the LED being driven at 50kHz.