

# A Generalized Multilevel Inverter Topology with Self Voltage Balancing

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**Abstract**—Multilevel power converters that provide more than two levels of voltage to achieve smoother and less distorted ac-to-dc, dc-to-ac, and dc-to-dc power conversion, have attracted many contributors. This paper presents a generalized multilevel inverter (converter) topology with self voltage balancing. The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from the generalized inverter topology. Moreover, the generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically without any assistance from other circuits, thus in principle providing a complete and true multilevel topology that embraces the existing multilevel inverters. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived. Some application examples of the generalized multilevel converter will be given.

## I. INTRODUCTION

Multilevel converters (or inverters) have been used for ac-to-dc, ac-to-dc-to-ac, dc-to-ac, and dc-to-dc power conversion in high power applications such as utility and large motor drive applications. Multilevel inverters provide more than two voltage levels. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency, higher efficiency, and lower voltage devices. There are three major multilevel topologies: cascaded, diode-clamped, and capacitor-clamped [1-11]. For the number of levels ( $M$ ) no greater than 3 (i.e.,  $M \leq 3$ ), or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Instead, each voltage level can be supported by a capacitor and proper control [6-7, 11]. However, for  $M > 3$  and applications involved in active power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control to support and maintain each voltage level [7, 10]. In this aspect, the three existing multilevel converters are neither operable nor complete for real (active) power conversion because they all depend on outside circuits for voltage balancing.

This paper presents a generalized multilevel inverter topology. The generalized multilevel inverter topology can balance each voltage level by itself regardless of inverter control and load characteristics. The existing multilevel inverters such as diode-clamped and capacitor-clamped multilevel inverters can be derived from this generalized inverter topology. Moreover, the generalized multilevel inverter topology provides a true multilevel structure that can balance each DC voltage level automatically at any number of levels regardless of active or reactive power conversion without any assistance from other circuits, thus in principle providing a complete multilevel topology that embraces the existing multilevel inverters. From this generalized multilevel inverter topology, several new multilevel inverter structures can be derived. In this paper, the detailed structures and operating principle of the generalized multilevel converter topology are presented. Analysis, discussion, and some application examples are briefed.

## II. GENERALIZED MULTILEVEL INVERTER AND OPERATING PRINCIPLE

Fig. 1 shows the generalized multilevel inverter topology per phase leg, where each switching device, diode, or capacitor's voltage is  $IV_{dc}$ , i.e.,  $1/(M-1)$  of the dc link voltage. Any inverter with any number of levels including the conventional two- (2-) level inverter, can be obtained from this generalized topology as shown in the figure. For example, the two level inverter phase leg can be obtained by cutting off at the "2-level line", three level inverter leg by cutting off at the "3-level line", and so on as shown in Fig. 1. It is evident that an  $M$ -level inverter can be constructed by the basic cell as shown in Fig. 2. The generalized  $M$ -level phase leg (Fig. 1) is a horizontal Pyramid of the basic cells. Since the basic cell is a two-level phase leg, this generalized multilevel inverter (Fig.1) is called P2 multilevel inverter. To explain the operating principle and analyze the circuit, the 5-level circuit is used hereafter. Fig. 3 shows the generalized 5-level inverter phase leg (or 5-level P2 inverter phase leg).

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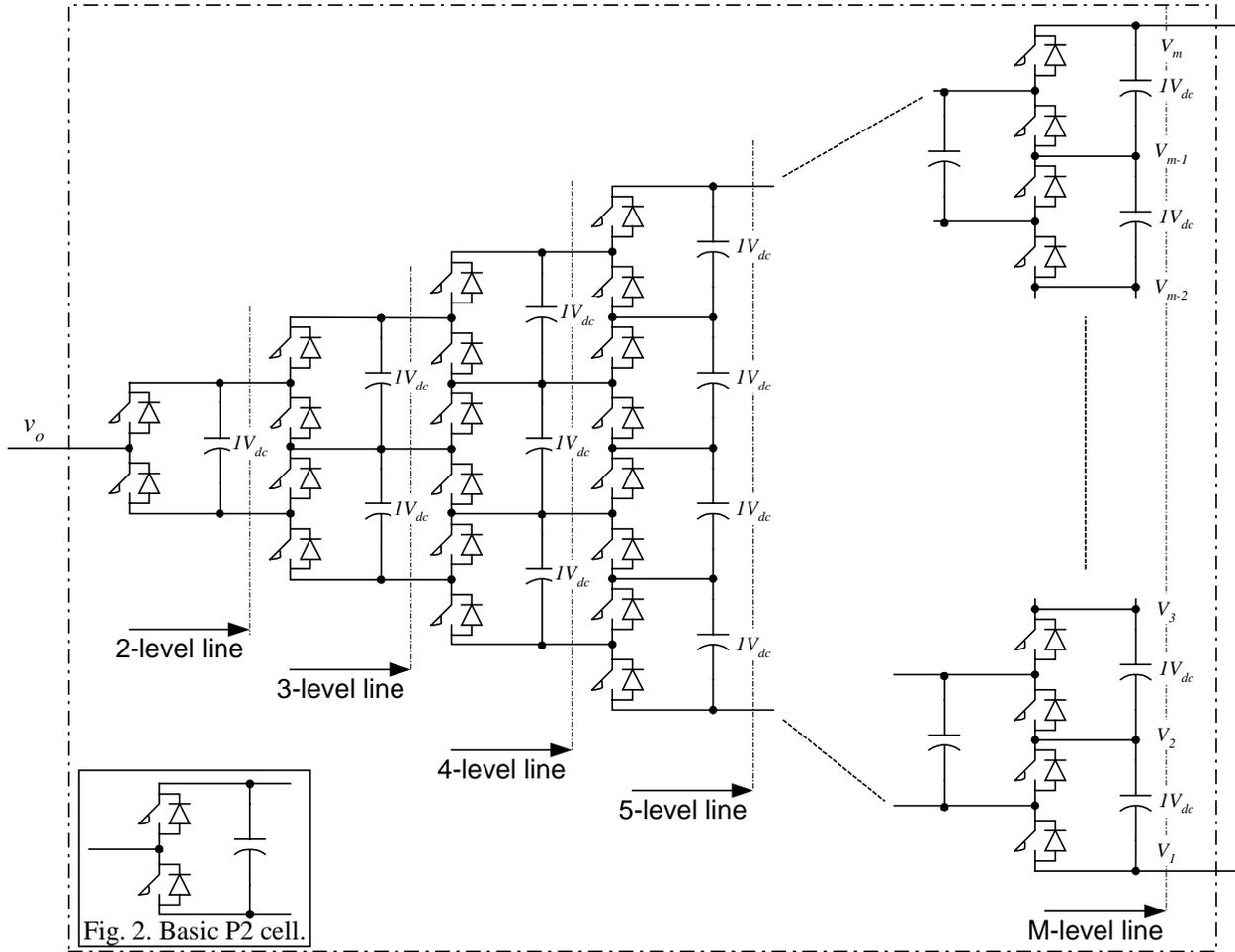


Fig. 1. Generalized multilevel inverter topology. ( $M$ -level, one phase leg).

In Fig. 3, switches  $Sp_1$ - $Sp_4$  and  $Sn_1$ - $Sn_4$  and diodes  $Dp_1$ - $Dp_4$  and  $Dn_1$ - $Dn_4$  shown in bold-line are the main devices to produce desired voltage waveforms. The rest of the switches and diodes are for clamping and balancing the capacitors' voltages, i.e., voltage levels. Each component's voltage stress is  $IV_{dc}$ . All voltage levels are self-balanced through clamping switches and clamping diodes. The operation can be explained as in Figs. 4-6. The circled (both solid line and dash line) devices indicate on-state devices and current path. The un-circled devices are off-state devices. In addition, the solid-line circled devices are the on-state devices necessary to produce the desired voltage level, whereas the dash-line circled ones are the on-state devices to keep their capacitors' voltages balanced, i.e., for balancing and clamping purpose. For example, in Fig. 4, switches  $Sn_1$ - $Sn_4$  are gated on to produce zero (0) voltage (i.e.,  $v_o=0$ , the zero potential is referenced to the negative rail of the dc bus). The dash-line-circled devices are gated

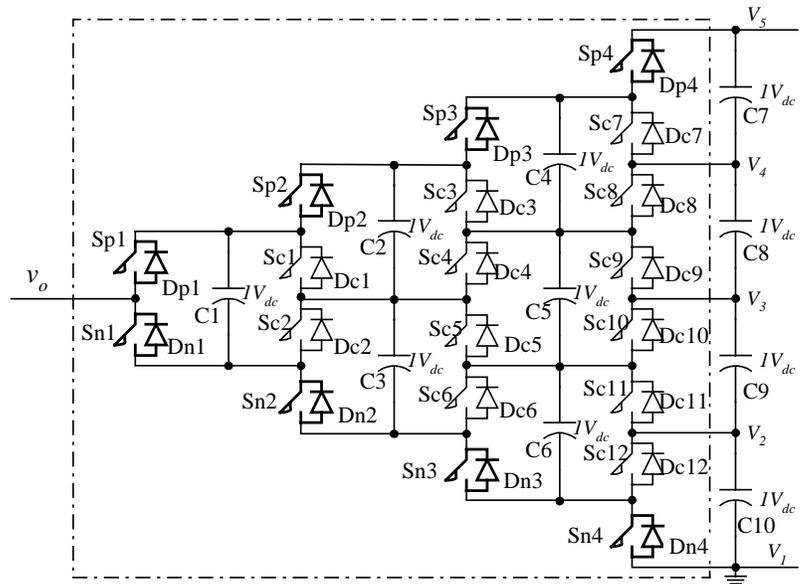


Fig. 3. Five-level P2 inverter phase leg.

on to clamp and balance voltages. The switches Sc1, Sc5, and Sc11 are gated on so that the capacitors C1, C3, C6, and C10 are connected in parallel to balance their charges (i.e.,  $V_{c1}=V_{c3}=V_{c6}=V_{c10}$ ). Similarly, the switches Sc3 and Sc9 are gated on so that the capacitors C2, C5, and C9 are charge-balanced (i.e.,  $V_{c2}=V_{c5}=V_{c9}$ ). And Sc7 is gated on letting C4 and C8 be charge-balanced (i.e.,  $V_{c4}=V_{c8}$ ). Fig. 5 shows one set of switching states for producing  $v_o=1V_{dc}$ . There are three other alternative switching states as shown in Table 1 to produce  $v_o=1V_{dc}$  and balance capacitors' charges. Fig. 6 shows one example of the alternatives. In Fig. 5,  $V_{c1}=V_{c3}=V_{c6}=V_{c10}$ ,  $V_{c2}=V_{c5}=V_{c9}$ , and  $V_{c4}=V_{c8}$ . In Fig. 6,  $V_{c3}=V_{c6}=V_{c10}$ ,  $V_{c1}=V_{c2}=V_{c5}=V_{c9}$ , and  $V_{c4}=V_{c8}$ . In this way, all capacitors' voltage can be balanced.

From the above explanation and with reference to Fig. 6, one can infer the following switching rules: (1) each switch pole is an independent switching unit; (2) any adjacent two switches of each switch pole are complementary, (i.e., if one is on the other is off and vice versa); (3) if any switch's state is determined or known then the rest switches of the pole are automatically determined because of the complementary rule. Table 1 summarizes the switching states to generate 0,  $1V_{dc}$ ,  $2V_{dc}$ ,  $3V_{dc}$ , and  $4V_{dc}$  voltage levels. Only Sp1-Sp4's states are shown because the complementary rule uniquely determines all remaining switches' states.

Fig. 7 shows simulation results of a three phase 5-level P2 inverter (three Fig. 3 phase legs connected together with a shared dc bus) driving an induction motor.  $I(\text{Load}_a)$ ,  $I(\text{Load}_b)$ , and  $I(\text{Load}_c)$  are the motor currents,  $V_{ab}$  is the inverter output phase "a" to phase "b" voltage, and V1 thru V5 are the five voltage levels, respectively. The waveforms clearly demonstrated that all the voltage levels are well balanced. As a well-known fact, the existing diode-clamped and capacitor-clamped multilevel inverters with more than 3 levels have no ability to balance each voltage level themselves for active power conversion.

Figs. 8-11 show some examples of existing multilevel inverters that can be deduced from the generalized multilevel inverter. Fig. 8 shows the diode-&-capacitor-clamped multilevel inverter that is derived from Fig. 3 by eliminating all clamping switches. Further eliminating the clamping switches and diodes of Fig. 3 yields the capacitor-clamped (or flying capacitor) multilevel inverter of Fig. 9.

Similarly, a diode-clamped multilevel inverter, Fig. 10, can be derived from Fig. 3 by eliminating the clamping switches and capacitors. Further, another diode-clamped multilevel inverter as shown in Fig. 11 can be obtained by swapping diode clamping paths.

Using the same pyramid structure of the P2 inverter, several other new configurations can be derived from the generalized multilevel inverter topology. For example, Fig. 12 shows a generalized multilevel inverter that is based on a 3-level diode-clamped phase leg, thus being called P3D multilevel inverter (or converter). Similarly, Fig. 13 shows the generalized P3C multilevel converter, which is based on a 3-level capacitor-clamped phase leg. Again in Figs. 12 and 13, each device's voltage stress is one voltage level. Compared with the P2 multilevel inverter, however, the P3D and P3C multilevel inverters require fewer clamping switches, diodes, and capacitors for the same number of levels. Some analysis and comparison are given in the following section.

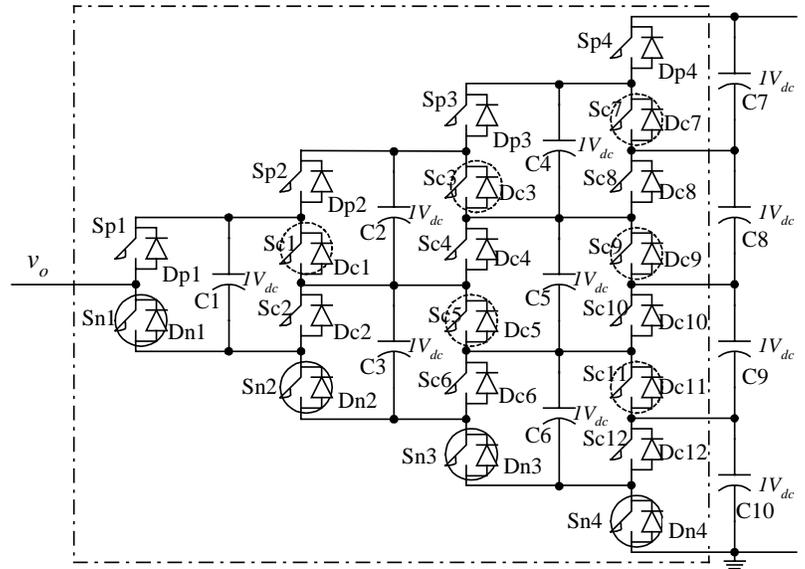


Fig. 4. Switching states to produce  $v_o=0$  and to clamp and balance capacitors' voltages.

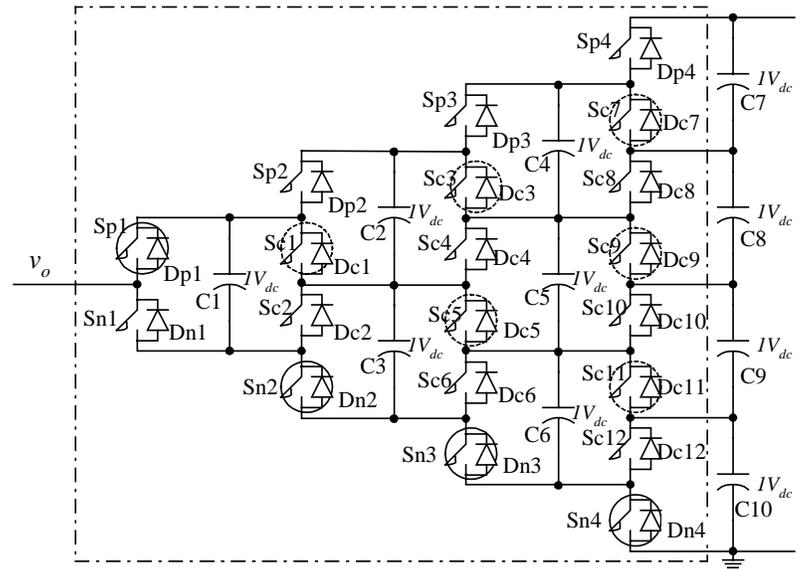


Fig. 5. Switching states to produce  $v_o=1V_{dc}$  and to clamp and balance capacitors' voltages.

### III. ANALYSIS, DISCUSSION, AND APPLICATION EXAMPLES

As described in the previous section, all capacitors' voltage is clamped (equalized) as the multilevel converter switches from one state to another. At each state change, the multilevel converter connects two different groups of capacitors together through switches and /or diodes. Fig. 14(a) shows a circuit illustrating this transition. If the two capacitors have a voltage difference,  $\Delta V$ , power loss will occur at each transition when the switch closes. To investigate such power loss, a MOSFET based multilevel converter is used as an example. For a MOSFET switch, it can be equivalently expressed as a resistance when turned on (Fig. 14(b)). The energy loss can be expressed as following at each transition:

$$E_{loss} = \frac{1}{4} C \cdot (\Delta V)^2, \quad (1)$$

which is proportional to the voltage difference and capacitance but independent of the resistance. The resistance only affects the initial charging/ discharging current and duration (Fig. 14(c)), but has no effect on the loss. The voltage difference is caused by charging or discharging current during each switching state, which can be expressed as

$$\Delta V = \frac{I_{avg}}{C \cdot f_{sw}}, \quad (2)$$

where  $I_{avg}$  is the average charging or discharging current during one switching cycle and  $f_{sw}$  is the switching frequency. From (1) and (2), the energy loss at each switching-over instant can be rewritten as (3) and the power loss is thus expressed as (4)

$$E_{loss} = \frac{I_{avg}^2}{4C \cdot f_{sw}^2}, \quad (3)$$

$$P_{loss} = \frac{I_{avg}^2}{4C \cdot f_{sw}}. \quad (4)$$

Therefore, the power loss is inversely proportional to the capacitance and switching frequency. In the simulation of Fig. 7 it was confirmed that the power loss generated is less than 1% of the load power at fundamental frequency switching. Using higher switching frequency and redundant switching states can reduce this power loss dramatically.

In the P2 M-level converter, the number of the required switching devices/diodes is  $M \cdot (M - 1)$  and the number of the required capacitors is  $M \cdot (M - 1) / 2$ . These numbers

can be easily obtained from the pyramid structure. Similarly, in the P3D M-level converter the required switching devices/diodes is  $(M^2 - 1) / 2$  and the number of the required capacitors or clamping diodes is  $(M^2 - 1) / 4$ . In the P3C M-level converter the required switching devices/diodes is again  $(M^2 - 1) / 2$  and the number of the required capacitors is  $3 \cdot (M^2 - 1) / 8$ . Compared with the P2 multi-level converter, the P3D and P3C multilevel converters advantageously use less switching devices, diodes, and capacitors. For example, the P2 5-level inverter needs 20 switching devices/diodes and 10 capacitors per phase leg, whereas the P3D 5-level inverter only uses 12 switching devices/diodes and 6 capacitors. It is possible to construct a multilevel inverter using basic cells with more than 3 levels. However, voltage balancing becomes an issue again.

The immediate use of the generalized multilevel converter topology may include switched-capacitor dc-dc converters and voltage multipliers [12-16]. For these applications, the component count is actually minimal and less than traditional ones. In addition, device stresses are minimized because of the auto-voltage balancing ability. Fig. 15 shows one example for bi-directional dc/dc conversion, the input inductor can be minimized or even eliminated for voltage multipliers. Another interesting and promising application is shown in Fig. 16 for bi-directional dc-dc conversion for the dual battery system of automobiles [17, 18]. In this application, low-voltage (30V) low-cost MOSFETs can be used to achieve high-efficiency (>99%), compact, and magnetic-less power conversion. Therefore, in these niched applications, the generalized multilevel converter can: (1) use low-voltage MOSFETs, (2) minimized or eliminate bulky magnetics, and (3) produce less distortion and virtually-zero EMI at output. Due to page limitation, detailed experimental set-up and results cannot be included in this paper. In a follow-up paper, some application examples will be investigated and experimental results will be reported.

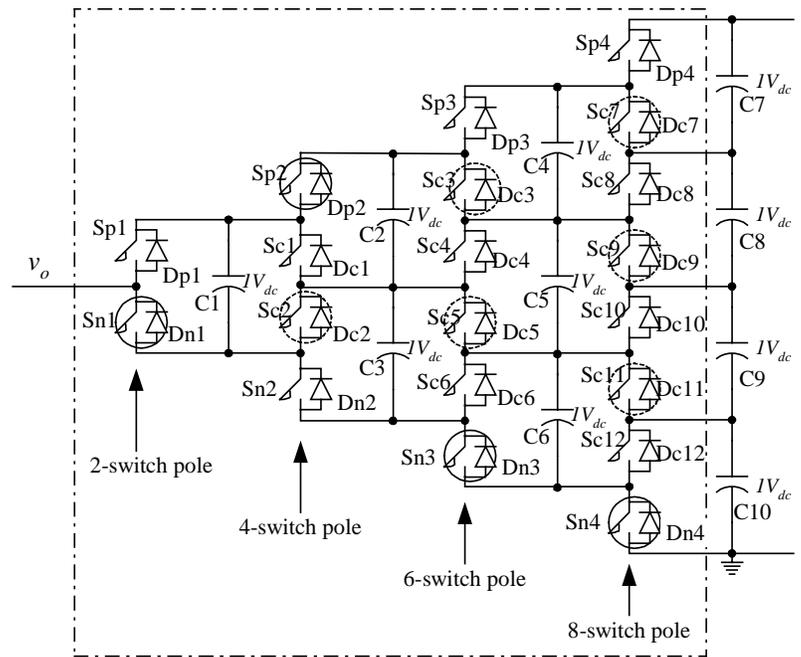


Fig. 6. Alternative switching states to produce  $v_o = 1V_{dc}$  and to clamp/balance capacitors' voltages.

Table 1. Switching states to produce  $v_o=0, 1Vdc, 2Vdc, 3Vdc,$  and  $4Vdc$  voltage levels.

Output Voltage	Capacitor* Path	Switch States**			
		Sp1	Sp2	Sp3	Sp4
0Vdc	None	0	0	0	0
1Vdc	+C1	1	0	0	0
	-C1 + C2+C3	0	1	0	0
	-C3-C2 + C4+C5+C6	0	0	1	0
	-C6-C5-C4 + C7+C8+C9+C10	0	0	0	1
2Vdc	+C2+C3	1	1	0	0
	-C1 + C4+C5+C6	0	1	1	0
	-C3-C2 + C7+C8+C9+C10	0	0	1	1
	+C1 -C3-C2 + C4+C5+C6	1	0	1	0
	+C1 - C6-C5-C4 + C7+C8+C9+C10	1	0	0	1
	-C1+C2+C3-C6-C5-C4+C7+C8+C9+C10	0	1	0	1
3Vdc	+C4+C5+C6	1	1	1	0
	-C1 +C7+C8+C9	0	1	1	1
	+C2+C3-C6-C5-C4+C7+C8+C9+C10	1	1	0	1
	+C1 -C3-C2 +C7+C8+C9+C10	1	0	1	1
4Vdc	+C7+C8+C9+C10	1	1	1	1

\* The capacitor path shows those capacitors that are connected to the output for each correspondent switching state. "+" shows that the capacitor is connected positively to the output and "-" shows that the capacitor is connected negatively.  
 \*\* "1" indicates on and "0" indicates off-state.

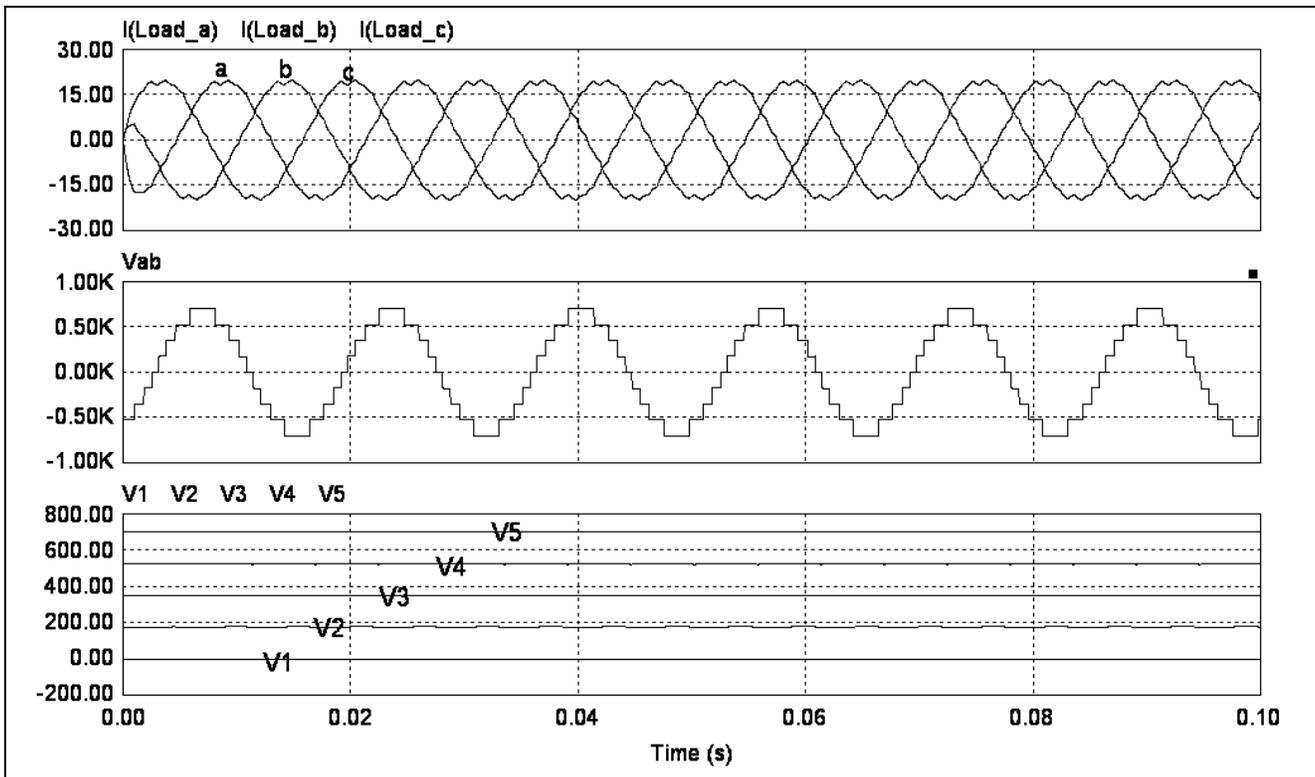


Fig. 7. Simulation results showing balanced voltage levels.

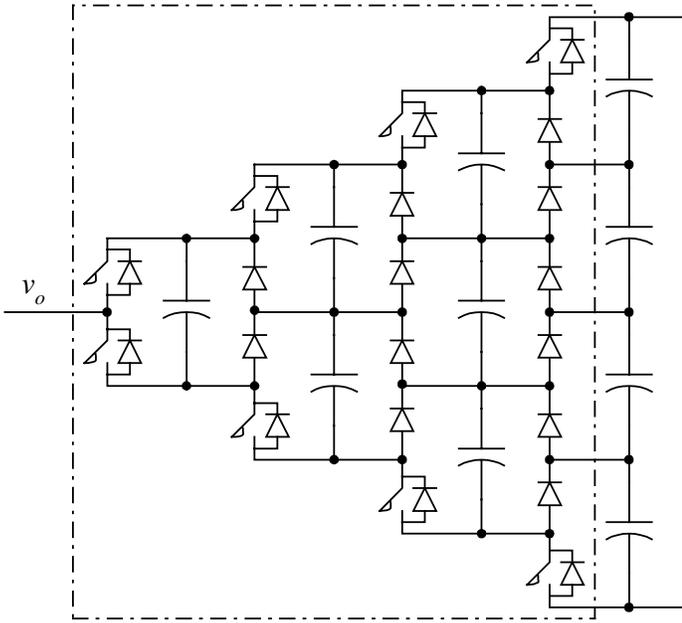


Fig. 8. Diode-&-capacitor-clamped multilevel inverter deduced from the Fig. 3 generalized topology sans clamping switches.

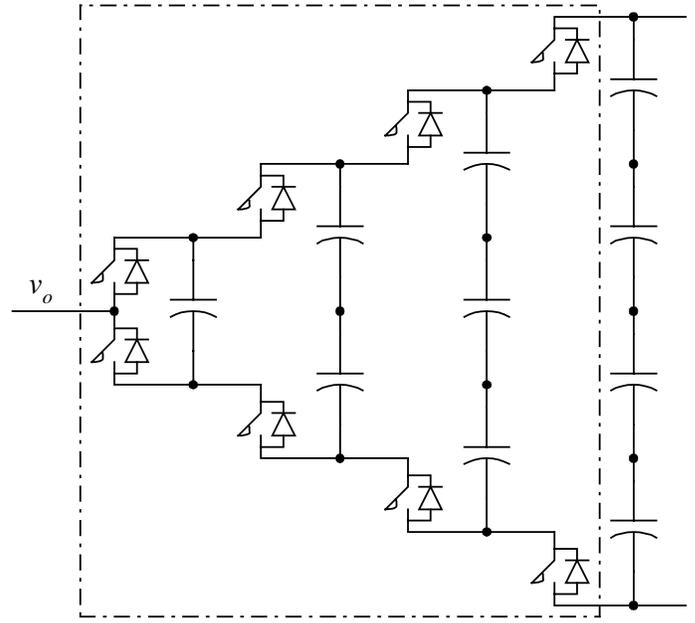


Fig. 9. Capacitor-clamped (or flying capacitor) multilevel inverter further deduced from the Fig. 3 generalized topology sans clamping switches and diodes.

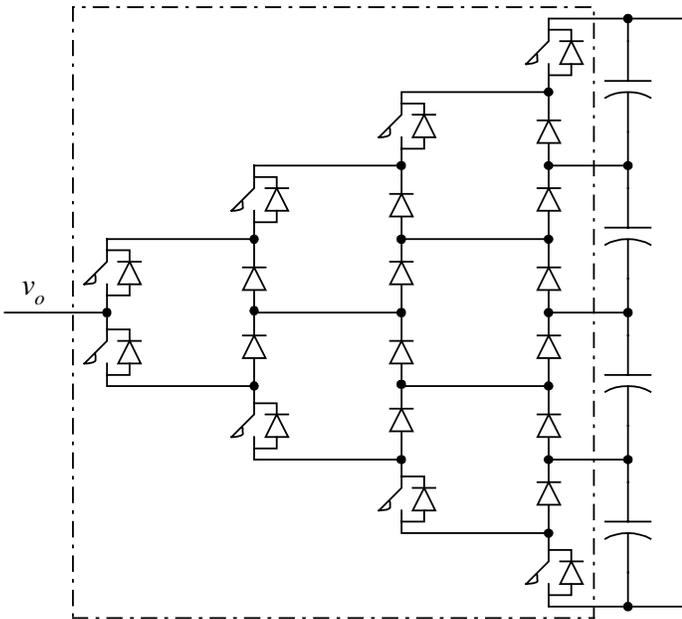


Fig. 10. Diode-clamped multilevel inverter I further deduced from the Fig. 3 generalized topology sans clamping switches and capacitors.

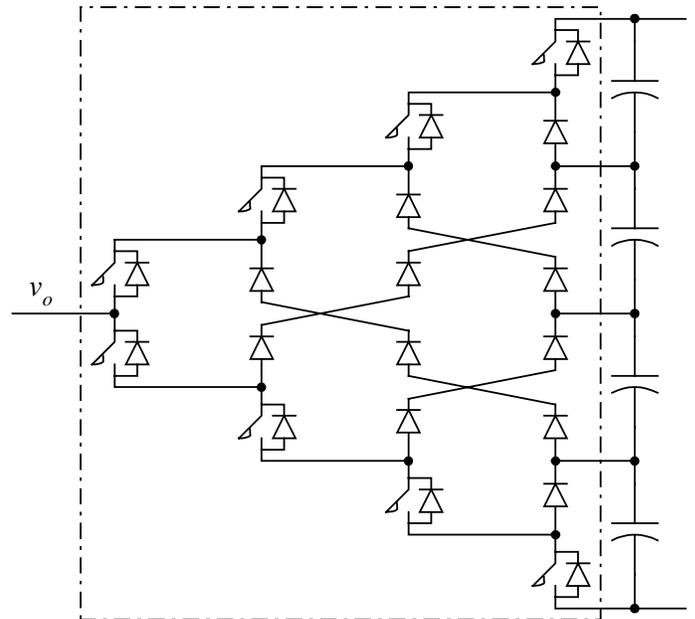


Fig. 11. Diode-clamped multilevel inverter II further deduced from the Fig. 3 generalized topology sans clamping switches and capacitors and with swapped diode clamping paths.

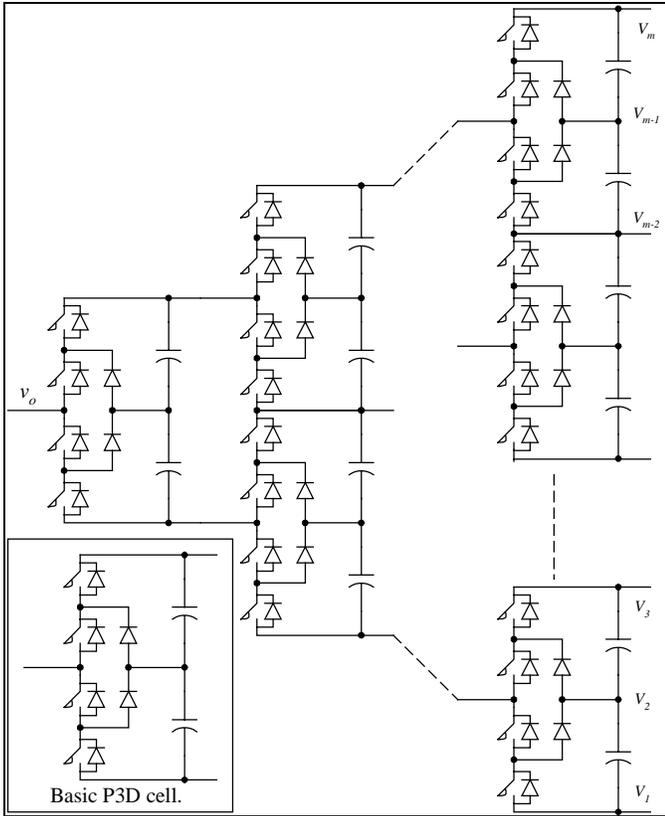


Fig. 12. Generalized P3D multilevel inverter.

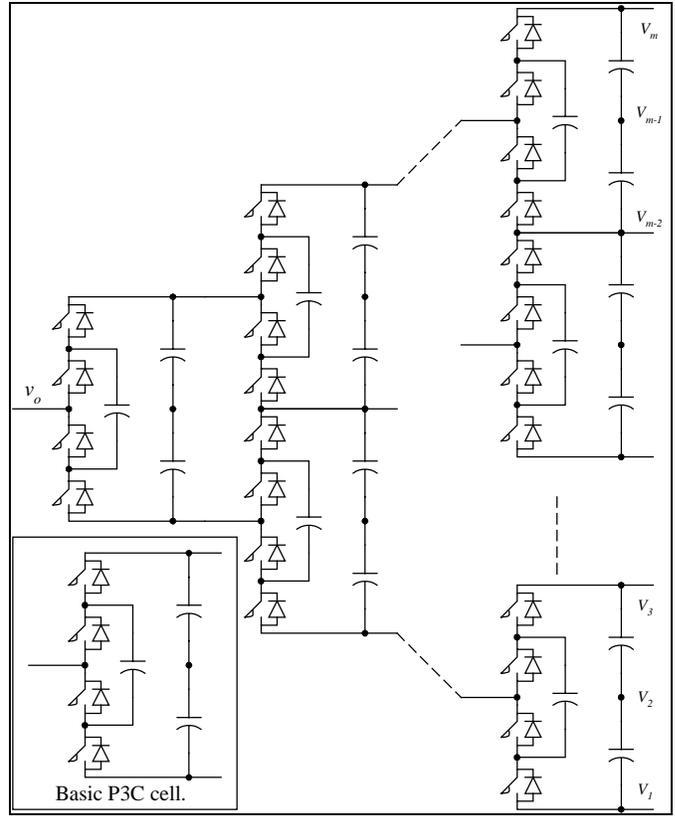


Fig. 13. Generalized P3C multilevel inverter.

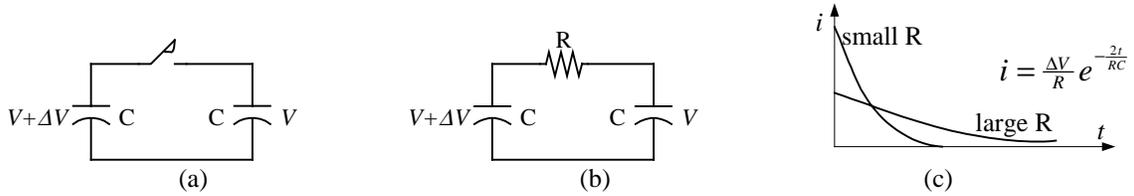


Fig. 14. Equivalent circuits and charging/discharging current waveforms during voltage equalization.

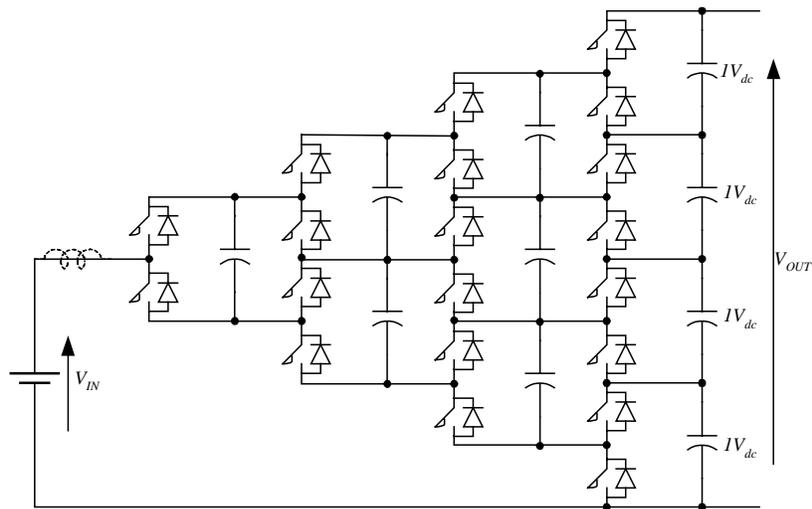


Fig. 15. Generalized P2 5-level converter for switched-capacitor dc-dc converter and voltage multiplier applications with bi-directional power flow.

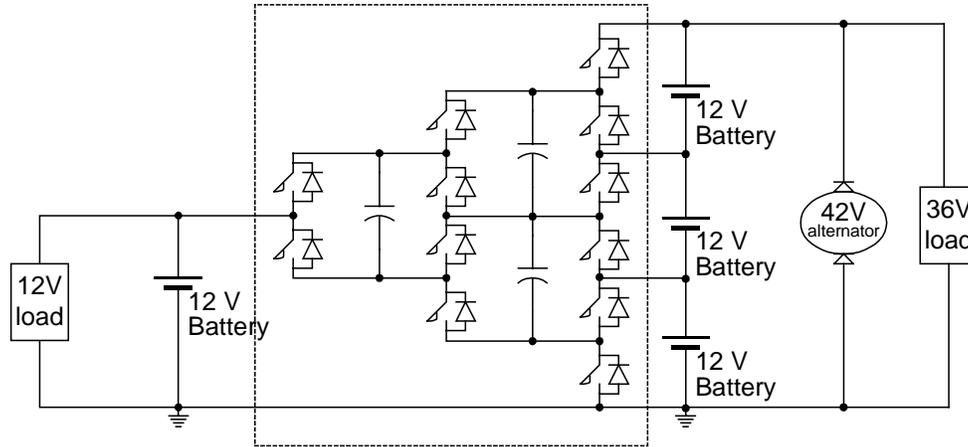


Fig. 16. 4-level P2 converter for dual battery system of automobiles.

#### IV. CONCLUSIONS

This paper has presented a generalized multilevel inverter topology. The existing multilevel inverters can be derived from this generalized structure. It has been demonstrated that the generalized multilevel inverter has self-voltage-balancing ability that the existing multilevel inverters do not have for the number of levels greater than three (i.e.,  $M > 3$ ) and for real power conversion. Although the generalized multilevel inverter needs a lot of clamping switches, diodes, and capacitors, in principle it is a true and complete multilevel inverter (or converter). In addition, the generalized topology has led to some new multilevel structures such as P3D and P3C. In some applications such as capacitor-switched power conversion, voltage multiplier, and bi-directional dc/dc conversion, the generalized multilevel converter topology has a niche for implementing magnetics-less, compact, high-efficiency, zero-EMI, and low-cost power conversion. In a follow-up paper, some application examples will be investigated and experimental results of a P2 4-level dc/dc converter for the dual battery system of automobiles will be reported.

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