MINIMUM CURRENT MAGNITUDE CONTROL OF SURFACE PM SYNCHRONOUS MACHINES DURING CONSTANT POWER OPERATION

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Abstract—The dual mode inverter control (DMIC) was developed to provide broad constant power speed range (CPSR) operation for surface mounted permanent magnet machines (PMSMs) having low inductance [1,2]. The DMIC interfaces the output of a common voltage source inverter (VSI) to the PMSM through an ac voltage controller. The ac voltage controller consists of three pairs of antiparallel SCRs, one antiparallel pair in series with each winding of the motor. In a recent paper [3] the performance of DMIC type controllers was analyzed using a fundamental frequency model and the authors concluded that the function of the SCRs was "equivalent to" extra inductance placed in series with the motor. The objective this is to show that the conclusion of [3] is misleading in two main respects. First, it ignores the fact that the SCRs enable maximum watts per rms amp control during constant power operation. It is shown that the rms motor current can be minimized for any given power level with the DMIC. Such control is not possible with a fixed inductance machine no matter how large the inductance when driven by a VSI. Second, the conclusion of [3] implies that a winding design strategy leading to a sufficiently large motor inductance would not benefit from the SCRs. It is shown that for PMSMs with inductance sufficiently large to achieve an infinite CPSR using only the VSI, losses can be substantially reduced by employing the SCRs. In

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particular, the SCRs can reduce motor current by a factor of 0.7071 at high speed and rated power. This reduces motor losses by 50% and conduction losses in the VSI by 29.3%. At less than rated power the percentage of motor/VSI loss reduction enabled by the SCRs is even larger.

I. INTRODUCTION

A recent paper [3] used a fundamental frequency model to analyze the performance of the sinusoidal back-emf permanent magnet synchronous motor (PMSM) driven in constant power mode. The inverter included a common three phase voltage source inverter supplemented with an ac voltage controller between the inverter output and the motor. The ac voltage controller consists of three pairs of anti-parallel SCRs as shown in Fig. 1. Each SCR is a full ac switch. In steady state, the fundamental frequency components of the voltage across and current through the switch are 90 degrees out of phase reflecting the lossless behavior of the switch and giving rise to an "equivalent reactance" interpretation of the SCRs. The inverter of Fig. 1 is called the dual mode inverter controller (DMIC) by the present authors [1,2] and it has been shown that this configuration results, theoretically, in a constant power speed range (CPSR) that is infinite even if the motor inductance is low. On a per phase basis, a fundamental frequency phasor model has the form shown in Fig. 2 with winding resistance neglected. The notation shown in Fig. 2 and used in this paper is: N_B = rotational base speed, rpm; N = rotational speed, rpm; n = relative speed = N/N_B; p = number of poles; L = motor inductance, h; Ω_B = base speed, electrical radians per second; X_B = motor reactance at base speed = $\Omega_B L$, ohms; X_{thy} = equivalent reactance of ac voltage controller, ohms; E_B = RMS line-to-neutral back emf magnitude at base speed, volts; $\bar{E}$ = back emf phasor at speed, n, (reference phasor); $\bar{I}$ = motor current phasor = $I_r + jI_x$; $\overline{V}_{inv}$ = fundamental frequency voltage phasor applied by the inverter; V_{dc} = dc supply voltage; V_{max} = maximum rms magnitude of inverter voltage = $\sqrt{2}V_{dc} / \pi$; and δ = inverter lead angle.

As noted in [3], the equivalent reactance of the ac switch is not constant but varies with the firing angle of the SCRs. The firing angle of the SCRs also controls the developed power of the motor. Since the equivalent reactance of the switch varies with the developed power, one cannot infer that the equivalent reactance interpretation can be extended to a fixed equivalent inductance that is in series with the motor winding. Even so, reference [3] concludes "the use of back-to-back thyristors to control a surface PM ac synchronous machine is equivalent to adding extra inductance in each machine phase that is useful for extending the CPSR." This conclusion is misleading in two respects. First it implies that the value of the SCRs in the DMIC inverter lies exclusively in the ability to extend the CPSR of low inductance machines. Second, it implies that if the machine inductance can be made sufficiently large,

either by supplementary external inductance in series or through a winding design leading to high inductance, that the DMIC would have no value since such motor could meet CPSR requirement with the VSI.

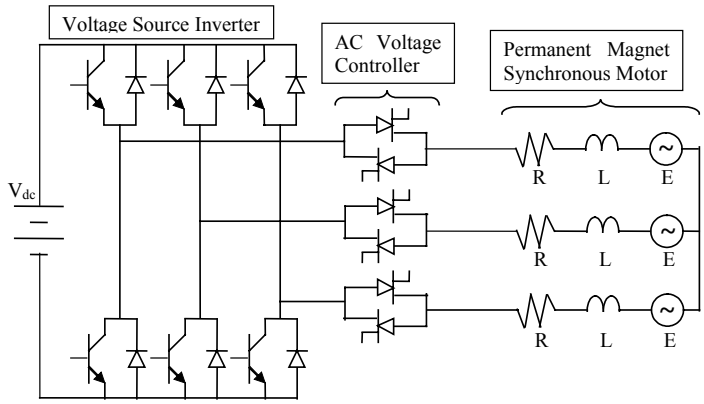

Fig. 1. DMIC inverter topology.

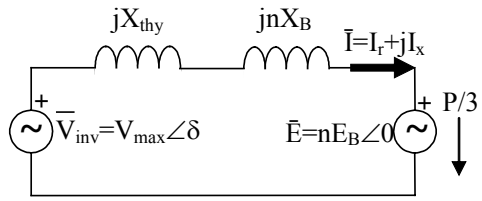

Fig. 2. Per phase fundamental frequency phasor model for constant power mode.

We have two objectives in this paper. The first is to show that the SCRs in the DMIC have far greater value than simply extending the CPSR. Specifically it is shown that during constant power operation the SCRs allow the rms motor current magnitude to be minimized for any given power level. Thus, the DMIC enables "dual modes" of optimal control. Above base speed the DMIC allows "maximum watts per rms amp" control during constant power operation. Below base speed the SCRs do not interfere in the inverter voltage magnitude control that allows "maximum Newton-meters per rms amp" during constant torque operation. The second objective is to show that the current minimization capability enabled by the SCRs in the DMIC inverter can result in substantially lower motor current than a common VSI drive even when the motor inductance is high. It is shown that the minimum current magnitude achieved through the DMIC is independent of speed and proportional to developed power. For a high inductance motor driven by a VSI the current magnitude is shown to be speed dependent but virtually independent of developed power level. At high speed the reduction in motor current magnitude is at least 0.7071 with the DMIC relative to the same motor driven by a VSI. Significant reduction in motor current reduces not only copper losses but also losses in the VSI. An economic evaluation of the DMIC must look past the added first cost

and additional losses due to the SCRs and consider the total value of loss reduction in the motor and the inverter over the life of the drive. The authors are conducting such evaluation in another study.

The fact that high machine inductance, or the addition of supplemental series inductance, can increase CPSR is not new as noted in previous works [4,5,6]. Removing the SCRs from Fig. 1 results in "conventional phase advance" (CPA) as described in [7]. To contrast the performance of CPA and DMIC we first consider the performance of a high inductance PMSM driven by CPA in Section II below. In Section III we show the current minimization made possible by the DMIC. The performance of CPA and DMIC are summarized in a single graph plotting normalized rms current versus normalized developed power for relative speeds above base speed

II. HIGH INDUCTANCE PMSM DRIVEN BY CPA

Assuming that the thyristors are removed from the DMIC inverter of Fig. 1 the topology then represents a PMSM driven by CPA and the fundamental frequency model of Fig. 2 has $X_{thy} = 0$ for all operating conditions.

Given the back emf voltage at base speed, E_B, and power rating of the motor, P_R, the rated current of the machine is

$$I_R = \frac{P_R}{3E_B} \quad . \tag{1}$$

The rated current will be the rms line current when operating at base speed and producing rated power provided that the dc supply voltage satisfies

$$V_{dc} = \frac{\pi}{\sqrt{2}} V_{max} \tag{2}$$

where

$$V_{max} \sqrt{E_B^2 + (X_B I_R)^2} \quad . \tag{3}$$

V_{max} is the maximum available rms line-to-neutral voltage applied to the motor by the inverter and the reactance, X_B, is the reactance of the machine at base speed.

When operating above base speed such that relative speed, n, is greater than one and producing power, P, the inverter lead angle δ is found from

$$\delta = \sin^{-1}\left(\frac{X_B P}{3V_{max} E_B}\right) = \sin^{-1}\left(\frac{P}{P_{max}}\right), \tag{4}$$

where

$$P_{max} = \frac{3V_{max}E_B}{X_B} \tag{5}$$

is the maximum power that can be developed. Clearly P_{max} has to be greater than or equal to the rated power, P_R. In some automotive applications a minimum value is specified for P_{max}. A low value of P_{max} resulting from a high machine inductance would mean that there is little margin for providing accelerating power above the rated power or for providing regenerative braking capability beyond the rated power.

Equation (4) shows that δ is independent of speed, i.e. it does not depend on n, such that constant power control is a simple matter of maintaining a constant inverter lead angle. Unfortunately, the rms motor current magnitude is not necessarily well behaved. For the fundamental frequency model, the rms current magnitude is

$$I = \frac{\sqrt{V_{max}^2 - 2nV_{max}E_B\cos\delta + n^2E_B^2}}{nX_B} \quad . \tag{6}$$

To ensure that the rms current given by (6) does not exceed the rated value in (1); the base speed reactance, X_B, must be sufficiently large. Observe that

$$\lim_{n\to\infty} I = \frac{E_B}{X_B} \quad . \tag{7}$$

Requiring the limit in (7) to be less than the rated current yields a motor inductance requirement that assures that the CPSR of the PMSM will be infinite

$$\frac{E_B}{X_B} = \frac{E_B}{\Omega_B L_\infty} = I_R \Rightarrow L_\infty = \frac{E_B}{\Omega_B I_R} = \frac{3E_B^2}{\Omega_B P_R} \quad . \tag{8}$$

The inductance value in Eq. (8) has been suggested as a requirement for passenger vehicle applications.

Let us assume that the motor inductance is the value for L_∞ given by Eq. (8) corresponding to an infinite CPSR such that,

$$\begin{aligned} V_{max} &= E_B\sqrt{2} \\ P_{max} &= P_R\sqrt{2} \\ \sin\delta &= \frac{P}{P_R\sqrt{2}} \\ \cos\delta &= \sqrt{1-\sin^2\delta} \end{aligned} \quad . \tag{9}$$

The rms motor current from (6) is then given by

$$I = I_R \sqrt{\frac{n^2 - 2n\sqrt{2 - \left(\frac{P}{P_R}\right)^2} + 2}{n^2}} \quad . \tag{10}$$

A plot of per unit rms current, I / I_R, versus per unit developed power, P / P_R, is shown in Fig. 3 for relative speeds of 2, 4, 6, 8, 10, 20 and ∞. The figure shows that when the motor inductance is sufficiently large, $L = L_\infty$ in this case, that any developed power up to the rated power can be achieved without exceeding the rms current rating of the motor. The "flatness" of the current versus power curves indicates that the copper losses in the motor are virtually independent of the developed power for the conventional phase advance strategy. Efficiency may be poor when operating conditions require a developed power less than the rated power. A method that can make the rms current proportional to output power can obviously reduce copper losses as well as VSI losses. In the case of the DMIC any reduction in copper losses can be applied to compensate for the increased losses in the SCRs and when there is a net reduction in total inverter plus motor losses, that reduction can be applied over the operating life of the drive towards the added first cost of the SCRs. In the next section we show the value of the motor current minimization and optimal watt per rms amp control enabled by DMIC.

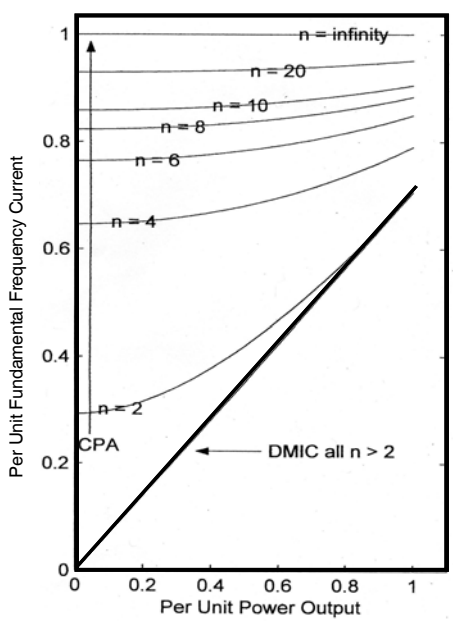

Fig. 3. Constant power operation of a PMSM motor comparing conventional phase advance control with dual mode inverter control.

III. PMSM CURRENT MAGNITUDE MINIMIZATION WHEN DRIVEN BY DMIC

Given that a PMSM with an inductance as large as that in (8) can achieve an infinite CPSR when driven by a VSI, is there any benefit to driving the same motor using the DMIC? To address this issue we use the fundamental frequency model of Fig. 2. Let the motor current phasor be written in rectangular form as

$$\bar{I} = I_r + j\,I_x \quad \text{and} \quad I = \left|\bar{I}\right| = \sqrt{I_r^2 + I_x^2} \quad , \tag{11}$$

where I_r is the component of motor current in phase with the back emf and I_x is the component in phase quadrature with the back emf. The question is, can the equivalent reactance of the SCRs, X_{thy}, be chosen so that desired power, P, is developed while the magnitude of the motor current, I, is minimized.

Observe that the value of the in phase component of motor current results in the developed power,

$$P = 3I_r nE_B \quad \text{and} \quad I_r = \frac{P}{3nE_b} \quad . \tag{12}$$

Since I_r is fixed per (12) the minimization of current magnitude, I, is the same as minimizing the magnitude of the phase quadrature component, I_x. Let

$$X = X_{thy} + nX_B \quad . \tag{13}$$

Then,

$$\bar{I} = \frac{\bar{V}inv - \bar{E}}{jX} = \frac{V_{max}}{X}\sin\delta + j\left[\frac{nE_b}{X} - \frac{V_{max}}{X}\cos\delta\right] = I_r + j\,I_x \quad . \tag{14}$$

Recognizing that

$$3\frac{V_{max}nE_B}{X}\sin\delta = P \quad and \quad \cos\delta = \sqrt{1 - \left(\frac{XP}{3nE_B V_{max}}\right)^2} \quad , \tag{15}$$

the phase quadrature component of motor current becomes

$$I_x = \frac{nE_b - V_{\max}\sqrt{1 - \left(\frac{XP}{3nE_B V_{\max}}\right)^2}}{X} \quad . \tag{16}$$

Differentiating I_x with respect to X, setting the derivative equal to zero, and solving for the current minimizing reactance, X^*, yields

$$X^* = \frac{3V_{\max}\sqrt{n^2E_B^2 - V_{\max}^2}}{P} = X_{thy}^* + nX_B \tag{17}$$

or,

$$X_{thy}^* = \frac{3V_{max}\sqrt{n^2E_B^2 - V_{max}^2}}{P} - nX_B = n\left(\frac{3V_{max}\sqrt{E_B^2 - \frac{V_{max}^2}{n^2}}}{P} - X_B\right) . \tag{18}$$

Expression (18) clearly shows that no fixed inductance can provide the same effect as the thyristors in the DMIC inverter. Specifically, observe that the reactance does not vary exactly linearly with speed, due to the $V_{\max}^2 / n^2$ inside the brackets in the second expression of (18), and that the reactance is inversely proportional to developed power, P. Thus, a fixed inductance can only achieve the same performance at a one speed-power state.

With the optimal value of thyristor reactance, the minimum rms motor current is

$$I^* = \frac{P}{3V_{max}} = \frac{P}{3\sqrt{E_B^2 + (X_B I_R)}} \quad . \tag{19}$$

Note that (19) is independent of speed and directly proportional to developed power. It can also be shown that the motor current is in phase with the inverter voltage phasor, such that the inverter operates at unity power factor.

Equation (19) applies whether the inductance is large or small. In cases where the motor is to provide substantial braking for the vehicle, the motor inductance, L, will necessarily need to be small such that $P_{\max}$ in (5) is substantially larger than the rated power, P_R. In such cases the CPA method of (8) would not yield adequate CPSR and DMIC would be essential. In this discussion, we want to show that DMIC has substantial potential benefit even when the motor inductance is large.

Letting the motor inductance be L_∞ from (8) and using the corresponding $V_{\max}$ from (9), the optimal rms fundamental frequency motor current magnitude is

$$I^* = \frac{P}{\sqrt{2}\,P_R} I_R \quad . \tag{20}$$

Note that (20) does not depend on speed. Although not shown here, (20) actually requires that the relative speed be greater than two. A plot of per unit motor current, I^* / I_R, versus per unit developed power, P / P_R, is shown in Fig. 3 where the single curve shown is valid for any speed at and above $n = 2$. The same set of axes was used to display the current versus power data for the same inductance level when the motor is driven by CPA.

Although a motor with inductance, L_∞, is considered well suited for high CPSR applications with CPA, the curves in Fig. 3 show that for relative speeds of two or greater that the motor current is always less for the same motor driven by DMIC, and for most operating conditions the current is substantially less with DMIC. Reductions in motor current will result in reduced motor losses, which vary with the square of rms current, and in reduced losses in the VSI components, which vary linearly with the rms motor current. For example, at high speed and rated power the rms motor current with the DMIC is 0.7071 that of the VSI driven motor. The motor losses are reduced by a factor of 50% while the VSI losses are decreased by 29.3%. At high speed and 70% of full power the rms current with the DMIC is 0.495 that of the VSI driven motor. The motor copper losses are reduced by 74.5% while the VSI losses are reduced by 50.5%. Depending on the application, particularly the speed/load profile, these life cycle loss reductions may more than compensate for the losses introduced by the addition of the SCRs.

IV. CONCLUSION

It has been shown that the DMIC provides minimization of the rms magnitude of the fundamental frequency motor current for any developed power level when operating in the high speed constant power mode. Thus, the DMIC provides maximum watts per rms amp control. This control can be provided whether the internal motor inductance is high or low. Such control is not possible even when the motor inductance is high if the motor is driven by CPA.

Recent laboratory investigation has demonstrated an 11.3 CPSR with DMIC and has shown that the inherent softness of the switching of the SCRs in the DMIC inverter allows "converter grade" SCRs to be used. This is important since the fundamental switching rate in high pole count PMSMs may be on the order of 1 kHz at top speed. In addition, converter grade SCRs are available in very large voltage ratings allowing higher back emf voltage/lower current designs to be assessed.

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