

dependent RC series connection in parallel to the depletion capacitance under the gate.

$D_i$  could not be clearly assessed in the MEMS-capacitors and the CMOS-capacitors due to the high  $I_i$  present. However, accounting for the leakage-induced tilt and shift in the post-bonding QS CV curve in Fig. 2, we observed very little distortion compared to the corresponding pre-bonding curve. This indicates that  $D_i$  in the CMOS-capacitors was not significantly affected by the anodic bonding.

**Oxide charge:** A change in the MOS flatband voltage  $V_{fb}$  implies a change in the fixed oxide charge.  $V_{fb}$  was observed to change only on the C2 MEMS-capacitors with  $d = 1 \mu\text{m}$ . The change was between 3 and 4 V, towards more negative  $V_{fb}$  values. This corresponds to an increase in positive fixed oxide charge of  $6.6 \times 10^{11} \text{cm}^{-2}$  to  $9.0 \times 10^{11} \text{cm}^{-2}$ . No significant change was observed on the other capacitors. The change in  $V_{fb}$  translates directly into a shift in the threshold voltage of the MOSFETs [8].

**Mobile ions:** Mobile ions, and especially sodium, can be extremely detrimental to integrated circuits, and great care is taken to avoid contamination during production. However, small quantities of mobile ions are tolerated. In all the CMOS-capacitors,  $N_m$  remained stable at  $\sim 2 \times 10^{10} \text{cm}^{-2}$  during the anodic bonding. In contrast, an increase of more than two orders of magnitude was observed on the C1 test-capacitors, with final values in the range  $2$  to  $4 \times 10^{12} \text{cm}^{-2}$ . The C2 test-capacitors had an increase of maximum  $2 \times 10^{10} \text{cm}^{-2}$ . These results indicate that the oxide was contaminated by mobile ions during anodic bonding, and that the contamination was much more severe outside the glass than within glass cavities. However, the results also show that an oxynitride layer on the chip surface provided sufficient protection of the oxide, and contamination can thus be avoided. The effect of the mobile ions on the MOSFET performance is similar to that of the oxide charges, and can be accounted for by adjusting the threshold voltage in the device model [8]. However, since the mobile charges move as a result of the electric field in the oxide, one has to expect a drift in the threshold voltage with time.

**Discussion and conclusion:** In previous works, we have argued that the effects on the gate oxide caused by anodic bonding are due to negative bias-temperature instability [9] and contamination by sodium ions transferred from the glass to the silicon structures [10]. Our results indicate that the effect of anodic bonding on gate oxide is dependent both on the gate oxide fabrication process and on the glass cavity depth  $d$ . We found that an oxynitride layer on the chip surface is to be recommended to avoid contamination from mobile ions during bonding. Hence, we observed that the oxide of the CMOS-capacitors, which has such a layer, was largely unaffected by the bonding process. This leads to the conclusion that the gate leakage in these devices was caused by a bonding-induced conducting path formed along the surface between the exposed gate electrode and the nearby substrate pad. A possible mechanism is sodium deposition originating from the glass cover. For the MEMS-capacitors and in the test-capacitors, the same process is probably taking place, in addition to the oxide degradation in these devices.

We have proposed efficient ways to incorporate the observed effects in the device simulations to ensure that the simulated output will be relevant for the wafer-level packaged device. To assess the effect of anodic bonding on a specific integrated system, we suggest that a test structure from the manufacturer in question is bonded to glass with the desired  $d$ .

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## Semi-insulating layers in 4H and 6H SiC by Si and C ion implantation

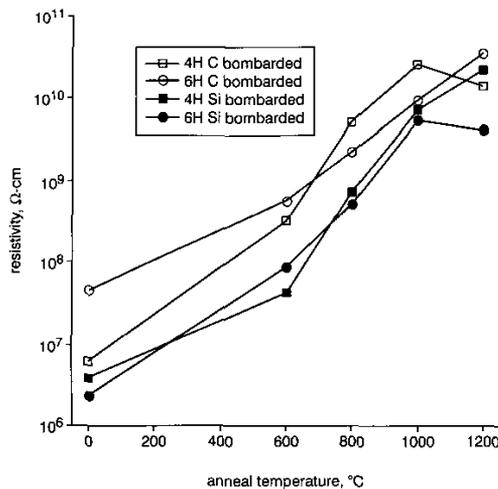
J.C. White, G.L. Harris and D.B. Poker

Semi-insulating regions have been obtained in 6H and 4H silicon carbide using ion implantation. The silicon carbide samples were implanted with either carbon or silicon ions followed by isochronal heat treatments. This leads to compensation, which is achieved by the lattice damage and by the thermal redistribution of atoms.

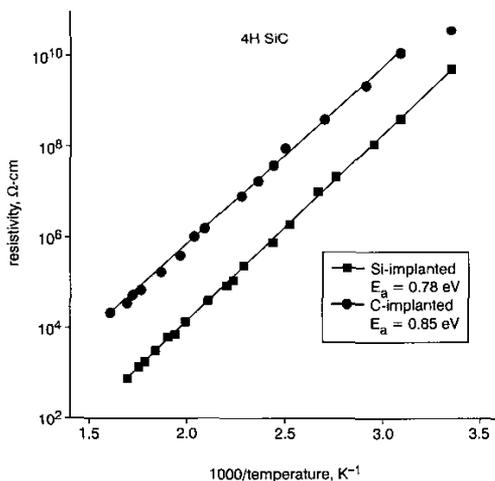
**Introduction:** Compensation of silicon carbide is of particular interest for obtaining semi-insulating or high resistive regions for interdevice isolation when the devices are made in the epilayers grown on semi-insulating silicon carbide. Presently, interdevice isolation in epilayers is primarily achieved by reactive ion etching of mesa regions. This step, however, is not compatible with planar processing technology in addition to bringing about low device yields. Ion implantation is highly desirable over mesa etching mainly due to planarity concerns. There are several studies on the topic of compensation using ion implanted hydrogen, but only a few using silicon or carbon ions to compensate the carriers [1–4]. The advantage of silicon and carbon is that it should produce regions of higher resistivity than hydrogen with more thermally stable deep level electron traps. In this Letter, we report on the incorporation of carbon and silicon concentrations into  $n$ -type 4H and 6H silicon carbide by ion implantation followed by isochronal heat treatments over the temperature range 600–1200°C.

**Experimental setup:** The material used in this experiment was  $n$ -type 4H and 6H SiC. The  $n$ -type bulk 4H had a resistivity of  $\sim 1 \Omega \text{cm}$  and the  $n$ -type bulk 6H had a resistivity of  $\sim 0.1 \Omega \text{cm}$ . Prior to implantation, 2000 Å-thick, 100  $\mu\text{m}$ -diameter nickel contacts were deposited on the face of the samples whereas the back of the samples were covered completely with nickel. The contacts were then alloyed at 1000°C. The resulting contact resistance was negligible when compared to the resistance of the processed samples. To create electron traps for compensation, multiple implants were then performed on the samples accelerating either Si or C ions in the energy range 0.4–3.0 MeV for Si and 0.5–4.5 MeV for C for a total concentration of  $\sim 1 \times 10^{19} \text{cm}^{-3}$ . The maximum implant depth was  $\sim 2 \mu\text{m}$ . The resistivity was then measured following 10 min anneals at 600, 800, 1000, 1200°C in an argon atmosphere. Temperature dependent resistivity measurements were carried out on the samples up to 400°C.

**Results and discussion:** The variation of resistivity with annealing temperatures for 4H and 6H SiC samples bombarded with Si and C ions is shown in Fig. 1. With the exception of the 1200°C anneal, the resistivity for each sample polytype increased as the annealing temperature was increased. At 1200°C there was a slight decrease in resistivity for 4H SiC samples bombarded with C and for 6H SiC samples bombarded with Si. The C bombardment produced the highest resistivity in the material. This occurred in the 6H polytype with a value of  $\sim 5 \times 10^{10} \Omega\text{-cm}$ . The increase in resistivity with annealing temperatures can be explained in terms of hopping conduction. Hopping conduction occurs when carriers hop from one defect site to another. This phenomenon occurs in ion implanted material thus causing increased carrier conduction. By repairing the lattice damage, the defect sites used for hopping or carrier conduction will decrease, leaving fewer intrastate transitions between the neighbouring defects sites for the carriers to hop, which invariably leads to less conductivity and higher resistance in the material. The maximum resistivity is obtained at a temperature that creates a balance between the electron traps created during ion bombardment and the free electron concentration.



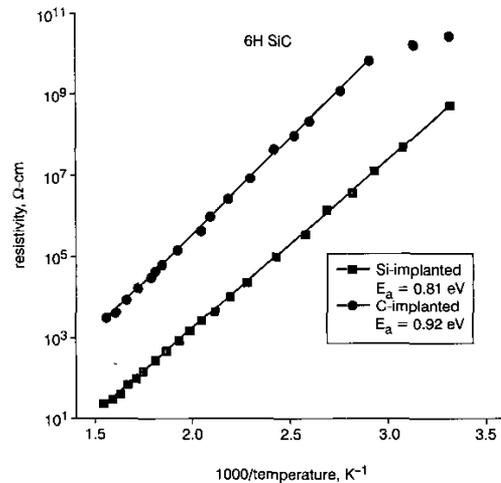
**Fig. 1** Variation of resistivity with annealing temperatures for Si and C bombarded 4H and 6H SiC samples



**Fig. 2** Variation of resistivity with  $1000/T$  for Si and C bombarded 4H SiC samples

The resistivity temperature dependence is shown for 4H and 6H SiC samples in Figs. 2 and 3, respectively. The Arrhenius relationship between temperature and resistivity,  $\rho \propto e^{-E_a/kT}$ , is used as a least squares fit with the fitting parameter being  $E_a$ . The activation energies created by the Si and C ions bombarded into 4H SiC were determined to be  $\sim 0.78$  and  $0.85$  eV, respectively, and  $\sim 0.81$  and  $0.92$  eV, respectively, for 6H SiC. The activation energies for 6H are similar to

the energies reported by Edwards *et al.* who reported a value of  $0.95$  eV for C bombarded samples and a value of  $0.8$  eV for Si bombarded samples [4]. To the best of our knowledge there are no similar reports for 4H.



**Fig. 3** Variation of resistivity with  $1000/T$  for Si and C bombarded 6H SiC samples

**Conclusion:** We have shown that by bombarding 4H and 6H SiC samples with silicon or carbon ions regions of semi-insulating or high resistivity are produced. These results can be used to obtain high-resistance regions for interdevice isolation and can also be applied to the development of other SiC technologies requiring highly resistive regions.

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#### Ambiguity in MUSIC and ESPRIT for direction of arrival estimation

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The Multiple Signal Classification (MUSIC) and Estimation of Signal Parameters via Rotational Invariance Techniques (ESPRIT) algorithms produce an ambiguity in the estimated direction-of-arrival results, when the antenna element spacing on a linear array is more than half a wavelength. The reason for this is investigated.