

Passivation of the 4H-SiC/SiO₂ Interface with Nitric Oxide

J.R. Williams¹, G.Y. Chung², C.C. Tin¹, K. McDonald³, D. Farmer³,
R.K. Chanana⁴, R.A. Weller⁵, S.T. Pantelides^{3,6}, O.W. Holland⁶,
M.K. Das⁷ and L.C. Feldman^{3,6}

¹ Department of Physics, Auburn University, Auburn, AL 36849, USA

² Sterling Semiconductor, Tampa, FL 33619, USA

³ Department of Physics and Astronomy, Vanderbilt University, Nashville TN 37235, USA

⁴ Alpha Industries, Inc., Haverhill, MA 01832, USA

⁵ Department of Electrical Engineering and Computer Science, Vanderbilt University,
Nashville, TN 37235, USA

⁶ Solid State Division, Oak Ridge National Laboratory, Oak Ridge, TN 37831, USA

⁷ Cree, Inc., Durham, NC 27713, USA

Keywords: Interface States, Inversion Channel Mobility, Nitric Oxide Passivation

Abstract. This paper describes a nitrogen-based passivation technique for interface states near the conduction band edge in 4H-SiC/SiO₂. These states were first proposed by Schorner, et al. [1], and their origin remains a point of discussion. However, there is now general agreement that these states are largely responsible for the lower channel mobilities that are reported for *n*-channel, inversion mode 4H-SiC MOSFETs. A post-oxidation anneal in nitric oxide at atmospheric pressure, 1175°C and 200-400sccm for 2hr reduces the interface state density at E_c-E ≈ 0.1eV by more than one order of magnitude to approximately 2x10¹²cm⁻²eV⁻¹. The effective channel mobility for lateral *n*-channel 4H-MOSFETs increases correspondingly from single digits to approximately 30-40cm²/V-s. The mobility for passivated devices exhibits a very weak temperature dependence compared to unpassivated devices for which the mobility increases in proportion to temperature to the power 1.9. The NO passivation process does not significantly affect the breakdown characteristics of thermal oxides on *n*- and *p*-4H-SiC, and the beneficial effects of passivation survive post-passivation processing procedures such as the high temperature anneals that are required to form source/drain ohmic contacts.

Introduction

Silicon carbide is the only wide band gap semiconductor that has a native oxide. Device-quality silicon dioxide can be grown on SiC using techniques that are basically the same as those used to grow SiO₂ on Si. This native oxide and other material properties such as large band gap, high thermal conductivity, high breakdown field strength and high saturated electron drift velocity make SiC metal-insulator-semiconductor devices very attractive for applications where high temperature, high power and high radiation must be considered. The 4H polytype has a larger band gap energy and a higher, more isotropic electron mobility, and is therefore the polytype of choice for high power applications. Blocking voltages for 4H-SiC MOSFETs have improved significantly over the past 10 years; however, almost no progress has been made in reducing the on-resistance of these devices. The on-resistance is dominated by the inversion channel resistance that is high because of low carrier mobility in the channel, the result being that the current handling capability of the device is severely limited.

The poor performance of 4H-MOSFETs is largely the result of a high interface state density located at approximately 2.9eV above the valence band edge [1]. This interface state density exists in all the polytypes of SiC, but represents a greater problem for 4H-SiC than for 6H-SiC because of the former polytype's wider band gap (~ 3.3eV compared to 3eV). High integrated interface state densities the order of 10¹³cm⁻² have been observed for both *n*- and *p*-4H-SiC [2-4].

These states are believed to result from carbon clusters that remain at the interface and defects in a near-interface sub-oxide that are produced when the oxidation process is terminated [5,6]. This defect density may be compared to a defect density of approximately 10^{10}cm^{-2} that is routinely achieved for Si/SiO₂. Therefore, field termination, carrier trapping and Coulomb scattering are much more serious problems for SiC MOSFETs than for Si devices.

A number of different approaches have been undertaken to improve the mobility for *n*-channel 4H-SiC MOSFETs. Sridevan, et al. [7] reported effective mobilities as high as $128\text{cm}^2/\text{V-s}$ for deposited oxides that were annealed sequentially in wet nitrogen at 1100°C , Argon at 1100°C and wet nitrogen at 950°C . However, these results have not been widely duplicated. Ogino, et al. [8] used low dose nitrogen implants in the *n*-channel region to control threshold voltages and reported higher mobilities ($\sim 99\text{cm}^2/\text{V-s}$) following implantation. Promising results have also been obtained Yano, et al. [9] who reported effective channel mobilities of approximately $30\text{cm}^2/\text{V-s}$ following oxidation of the $(11\bar{2}0)$ surface (the a-face) of 4H-SiC. Buried channel devices have recently been fabricated by Harada, et al. [10], and peak channel mobilities of around $140\text{cm}^2/\text{V-s}$ were reported for low gate voltages. However, the mobility decreased rapidly with increasing gate voltage, and was below $40\text{cm}^2/\text{V-s}$ at $V_g = 10\text{V}$ – an indication perhaps of problems with carrier confinement in the buried channel at higher gate voltages.

We have used post-oxidation anneals in nitric oxide similar to the those described by Li, et al. for 6H-SiC [11] to reduce the interface state density near the conduction band edge by more than one order of magnitude for *n*-4H-SiC MOS capacitors [12]. Furthermore, these anneals (2hr at 1175°C) improve the effective channel mobility by factors of $\times 10$ - $\times 15$ for lateral, *n*-channel MOSFETs fabricated with standard 4H-SiC [13].

We have also conducted passivation anneals with ammonia (NH₃), forming gas (N₂/5%H₂) and nitrous oxide (N₂O). Anneals in forming gas at temperatures up to 1000°C resulted in an improvement of about a factor of two for D_{it} at $E_c - E = 0.6\text{eV}$; however, at 0.15eV below the conduction band edge, no noticeable improvement was observed. Ammonia appears to be just as effective as NO in reducing $D_{it}(E_c)$ [14]; however, the breakdown field strength was found to be much lower for oxide layers passivated with NH₃. We attribute the lower breakdown field strength to the fact that nitrogen appears uniformly throughout the oxide layer as well as at the SiC/SiO₂ interface following NH₃ anneals, while nitrogen accumulates almost entirely at the interface following NO passivation [15]. For similar anneal conditions, the amount of incorporated nitrogen is much higher ($\sim \times 100$) for NH₃ compared to NO, and oxide layers annealed in ammonia are characterized by a ratio of 1.5 for oxygen loss to nitrogen gain. This ratio is consistent with the formation of nitrides and/or oxynitrides via the reactions $3\text{SiO}_2 + 4\text{NH}_3 \rightarrow \text{Si}_3\text{N}_4 + 6\text{H}_2\text{O}$ and $2\text{SiO}_2 + 2\text{NH}_3 \rightarrow \text{Si}_2\text{N}_2\text{O} + 3\text{H}_2\text{O}$ [16].

The results of our own SIMS measurements support those reported by Jamet and Dimitrijevic [17] that show that nitrogen build up at the 4H-SiC/SiO₂ interface is similar for N₂O and NO anneals carried out at 1150°C . These authors also report XPS results that show that NO and N₂O annealing produces chemically identical interfaces of improved quality as the result of carbon removal during the anneals. For passivation anneals at 1175°C , we observe that the oxide layer thickness increases by approximately 25% for N₂O, but only by about 6% for NO. We speculate that this may be one reason that we have observed no improvement in the interface state density near the 4H-SiC conduction band edge following N₂O anneals at temperatures between 1050 and 1175°C .

Considering both interface state passivation and oxide breakdown, we have achieved our best results using nitric oxide. The results of our NO passivation studies for 4H-SiC/SiO₂ are described in the remainder of this paper.

Experimental Procedure

Epitaxial layers grown by Cree, Inc. on standard 4H-SiC wafers were used for studies of *n*-4H MOS capacitors and *n*-channel 4H-MOSFETs. The nitrogen doping concentration and epilayer thickness were $8 \times 10^{16} \text{cm}^{-3}$ and $5 \mu\text{m}$ for the MOS capacitors, and mobility measurements were made for lateral MOSFETs fabricated by dry oxidation of $10 \mu\text{m} / 8 \times 10^{16} \text{cm}^{-3}$ epilayers and wet oxidation of $3 \mu\text{m} / 1 \times 10^{16} \text{cm}^{-3}$ epilayers – both doped with Al. Prior to oxidation, all samples were cleaned using procedures that have been described previously [18]. Our initial studies used oxide layers with thicknesses typically between 40 and 80nm that were grown using the wet, thermal techniques described in reference [19]. These techniques included the well-known “re-oxidation” step that effectively reduces the interface state density near mid-gap [20,21]. We have since switched to dry oxide growth using the same techniques described in [19] except that the re-oxidation anneal is no longer used. Rather, the oxidation process is terminated with a 30min Ar anneal at the growth temperature (1150°C), after which the sample is brought back to room temperature at $3.3^\circ\text{C}/\text{min}$ in flowing Ar.

MOS capacitors were characterized using standard high-low (1MHz-quasistatic) C-V techniques applied at room temperature for measurements near the conduction band edge. Sputtered Mo was used for $300 \mu\text{m}$ diameter gate contacts and large area ($> 25 \text{mm}^2$) backside contacts were formed on the n^+ -substrates using Ag colloidal paste.

Lateral MOSFETs were fabricated with both wet and dry oxides (see [19] for details). Following oxidation, MOSFETs with wet oxides were fabricated and characterized at Cree, and devices with dry oxides were fabricated and evaluated at Auburn. For all devices, long channel lengths and a “fat FET” design (i.e. large S/D dimensions) were used to minimize the source/drain resistance relative to the channel resistance. The source/drain contacts were not annealed prior to characterization, and effective channel mobilities were extracted from plots of drain current as a function of gate voltage for a fixed drain voltage of 50mV.

Results

Post-oxidation anneals in NO were carried out at atmospheric pressure for various times (0.5 - 6hr), temperatures ($1050 - 1175^\circ\text{C}$) and flow rates (200 - 800sccm) to optimize these parameters for the passivation process. Our standard NO anneal is now performed for 2hr at 1175°C and 400sccm. As stated previously, the thickness of the original oxide layer increases by approximately 6% during the anneal [15]. The effect of NO passivation on $D_{it}(E_c)$ is shown in Fig. 1. The magnitude of the interface state density for *n*-4H-SiC is reduced significantly to a value that is “6H-like” following the NO anneal. These results are in agreement with the assertion by Schorner, et al. [1] that substantially more interface states exist in the upper half of the band gap for 4H-SiC than for 6H-SiC. We attribute the reduction in $D_{it}(E_c)$ to the passivation of carbon cluster interface states that have energies in the top half of the SiC band gap [12,22].

The effect of nitrogen passivation on the effective mobility of 4H-MOSFETs is shown in Fig. 2 where a $\times 10$ - $\times 15$ improvement can be observed compared the single digit mobilities commonly reported for standard 4H devices. Results also suggest that a completely dry oxidation process may be used for MOSFET fabrication in order to take advantage of the higher breakdown voltage of dry oxides [23].

Previous investigations [8,24,25] of unpassivated MOSFETs fabricated with standard 4H-SiC have reported increasing mobility with increasing temperature. These observations were explained with the supposition of increased carrier concentration and reduced Coulomb

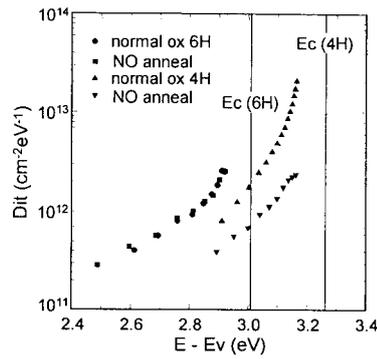


Fig. 1. The interface state density near the conduction band edge in *n*-4H-SiC/SiO₂ before and after nitric oxide passivation. Results for D_{it} for *n*-6H-SiC/SiO₂ are also shown for comparison.

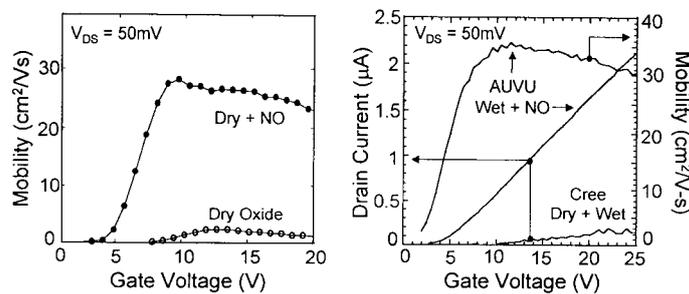


Fig. 2. The effect of NO passivation on the effective channel mobility of lateral 4H-SiC MOSFETs fabricated with dry and wet oxides.

scattering due to thermal emission of electrons from the interface traps near the conduction band. Yano, et al. [26] recently reported that the mobility for MOSFETs fabricated on the a-face of 4H-SiC has a negative temperature dependence. The authors suggest that the a-face has lower interface state density near the conduction band, so that carrier transport is more affected by phonon scattering.

Maximum field effect mobilities and threshold voltages as a function of temperature are shown in Fig. 3 for 4H-SiC MOSFETs with and without NO passivation. The mobility of the unpassivated device increases with increasing temperature in proportion to $T^{1.9}$, while the mobility of the passivated MOSFET remains almost unchanged. The threshold voltage of the unpassivated MOSFET decreases significantly from 7.5 to 3.9 V over the temperature range 300 to 473°K. However, the threshold voltage of the passivated MOSFET has only a weak dependence on temperature. Decreasing threshold voltage corresponds to the reduction of negative effective charge in the oxide or at the interface. For lateral 4H-MOSFETs, the negative charge is produced when electrons are trapped in acceptor-like interface states. The NO passivation process reduces the density of these states near the conduction band edge and therefore produces a weaker temperature dependence for V_{th} and for the effective channel mobility.

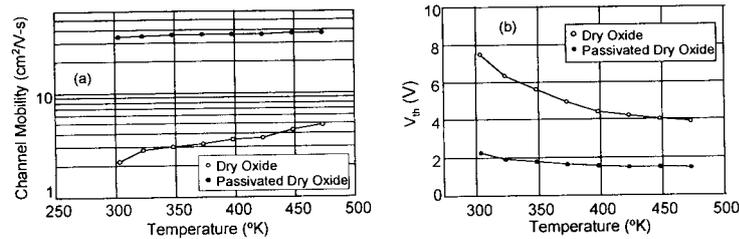


Fig. 3. Temperature dependence for (a) effective mobility and (b) threshold voltage for lateral 4H-SiC MOSFETs with and without NO passivation.

Summary

A nitrogen-based interface passivation process has been developed for 4H-SiC MOSFETs. The process is based on post-oxidation, high temperature anneals in nitric oxide, and results in a $\times 10$ - $\times 15$ increase in the effective channel mobility for lateral devices fabricated with either dry or wet thermal oxides. Peak effective mobilities of 30-35 cm²/V-s are among the highest yet reported for devices fabricated with thermal oxides and standard 4H-SiC. For both wet and dry oxides, the NO passivation process improves breakdown on *n*-4H-SiC, and produces only a small decrease in breakdown voltage for *p*-4H-SiC [19]. Other papers presented at this conference [27,28] show that the beneficial effects of NO passivation survive post-oxidation processing steps (e.g., source/drain contact anneals), and that passivation improves performance when applied to power device geometries.

Even so, the optimized NO passivation process reduces the interface state density for 4H-SiC to only $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_c - E = 0.1 \text{ eV}$, compared to a trap density of approximately $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ for passivated Si/SiO₂. Clearly, further work will be required to determine conclusively whether other kinds of states exist at the 4H-SiC/SiO₂ interface, and, if so, whether additional techniques can be developed to passivate these states.

Acknowledgements: This work was supported by DARPA Contract MDA972 98-1-0007 (program manager, D. Radack; technical monitors, J. Zolper and G. Campisi), EPRI Contract W0806905 (program managers J. Melcher and B. Damsky; technical monitor, F. Goodman), and ONR Grant N000140110616 (program manager, J. Zolper). Research at Oak Ridge National Laboratory sponsored by the Division of Material Sciences, U.S. Department of Energy, under contract DE-AC05-00OR22725 with UT-Battelle, LLC.

References

1. R. Schorner, P. Friedrichs, D. Peters and D. Stephani, *IEEE Elect. Dev. Lett.* **20** 241 (1999).
2. G.Y. Chung, C.C. Tin, J.H. Won and J.R. Williams, *Matls. Sci. Forum* **338-342** 1097 (2000).
3. M.K. Das, B.S. Um and J.A. Cooper, Jr., *Matls. Sci. Forum* **338-342** 1069 (2000).
4. N.S. Saks, S.S. Mani and A.K. Agarwal, *Appl. Phys. Lett.* **76(10)** 2250 (2000).
5. V.V. Afanasev, M. Bassler, G. Pensl and M. Schulz, *Phys. Stat. Sol. (A)* **162** 321 (1997).
6. G.G. Jernigan, R.E. Stahlbush, M.K. Das, J.A. Cooper and L.A. Lipkin, *Appl. Phys. Lett.* **74(10)** 1448 (1999).
7. S. Sridevan and B.J. Baliga, *IEEE Elect. Dev. Lett.* **19(7)** 228 (1998).

8. S. Ogino, T. Oikawa and K. Ueno, *Mats. Sci. Forum* **338-342**, 1101 (2000).
9. H. Yano, T. Hirao, T. Kimoto, H. Matsunami, K. Asano and Y. Sugawara, *Mats. Sci. Forum* **338-342** 1105 (2000).
10. S. Harada, S. Suzuki, J. Senzaki, R. Kozugi, K. Adachi, K. Fukuda and K. Arai, *IEEE Electron Dev. Lett.* **22(6)** 272 (2001).
11. H. Li, S. Dimitrijević, H.B. Harrison and D. Sweatman, *Appl. Phys. Lett.* **70(15)**, 2028 (1997).
12. G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, M. Di Ventura, S.T. Pantelides, L.C. Feldman and R.A. Weller, *Appl. Phys. Lett.* **76(13)** 1713 (2000).
13. G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R.K. Chanana, R.A. Weller, M. Di Ventura, S.T. Pantelides, L.C. Feldman, O.W. Holland, M.K. Das and J.W. Palmour, *IEEE Elect. Dev. Lett.* **22(4)** 176 (2001).
14. G.Y. Chung, C.C. Tin, J.R. Williams, K. McDonald, R.A. Weller, M. Di Ventura, S.T. Pantelides and L.C. Feldman, *Appl. Phys. Lett.* **77(22)** 3601 (2000).
15. K. McDonald, R.K. Chanana, R.A. Weller, L.C. Feldman, G.Y. Chung, C.C. Tin and J.R. Williams, "Nitrogen incorporation in 4H-SiC/SiO₂ by NO and NH₃ anneals", paper presented at the *Fall, 2000 Meeting of the Mats. Res. Soc.*
16. K. McDonald, Ph.D. Dissertation, Vanderbilt University, 2001.
17. P. Jamet and S. Dimitrijević, *Appl. Phys. Lett.* **79(3)** 323 (2001).
18. G.Y. Chung, C.C. Tin, J. H. Won, J.R. Williams, K. McDonald, R.A. Weller, S.T. Pantelides and L.C. Feldman, *Proc. 2000 IEEE Aerospace Conf.* 1 1001 (2000).
19. J.R. Williams, G. Chung, C.C. Tin, K. McDonald, D. Farmer, R.K. Chanana, R.A. Weller, S.T. Pantelides, O.W. Holland, M.K. Das and L.C. Feldman, *Mat. Res. Soc. Symp. Proc.* **640** H3.5.1 (2000).
20. L.A. Lipkin and J.W. Palmour, *J. Electronic Matls.* **25(5)** 909 (1996).
21. M.K. Das, J.A. Cooper and M.R. Melloch, *J. Electronic Matls.* **27(4)** 353 (1998).
22. S.T. Pantelides, R. Buczko, G. Duscher, S.J. Pennycook, L.C. Feldman, M. Di Ventura, S. Wang, S. Kim, K. McDonald, R.K. Channa, R.A. Weller, G.Y. Chung, C.C. Tin, T. Isaacs-Smith and J.R. Williams, *Mat. Res. Soc. Symp. Proc.* **640** H3.3.1 (2001).
23. L.A. Lipkin and J.W. Palmour, *IEEE Trans. Electron Dev.* **46(3)** 525 (1999).
24. S. Harada, R. Kosugi, J. Senzaki, S. Suzuki, W. J. Cho, K. Fukuda and K. Arai, *Mat. Res. Soc. Symp.* **640** H.37.1 (2001).
25. R. Singh, S. Ryu and J.W. Palmour, *Mat. Sci. Forum*, **338-342** 1271 (2000).
26. H. Yano, T. Hirao, T. Kimoto and H. Matsunami, *Appl. Phys. Lett.* **78** 374 (2001).
27. C.-Y. Lu, J.A. Cooper, G. Chung, J.R. Williams, K. McDonald and L.C. Feldman, *Effect of Process Variations on 4H Silicon Carbide MOSFET Mobility*, ICSCRM 01.
28. M.K. Das, G. Chung, J.R. Williams, N.S. Saks, L.A. Lipkin and J.W. Palmour, *High Current, NO Annealed Lateral 4H-SiC MOSFETs*, ICSCRM 01.