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IR Imaging of Integrated Circuit Power Transistors During Operation

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ABSTRACT

An infrared microscope was used to study the surface temperature profiles of power transistor arrays in integrated circuits (IC) during operation. Each transistor array was set to conduct current for 20-50 microseconds. The integration time of the IR camera is adjusted. to be between 2 and 10 microseconds. A thorough study of the camera's timing characteristics allows its precise synchronization to. transient thermal events in the transistor arrays. Progressively adding incremental delay times to the synchronization pulses allows the complete characterization of the thermal transients as a function of time and location. The IR microscope timing characteristics were determined by imaging an incandescent lamp filament during pulsed operation. Examples of heat pulses in a lamp filament and power transistors are given.

Keywords: infrared imaging, IR microscope, transistor, triggering, synchronization and integrated circuit

1. INTRODUCTION

Thermal transients are defined as high-speed temperature variations in a material as a result of optical or electrical stimulus. In most cases, the duration of a thermal transient is extended by the thermal mass' of the material. Researchers have shown that these kinds of thermal transients can be observed using IR camera based Focal Plane Array technology[1-3]. Careful triggering and synchronization are needed to study these transients. In some special cases, for example heat pulses in a silicon based device, the thermal transients cool very fast due to the high thermal conductivity of silicon and the small mass of material involved Cooling in such a device takes about the same time duration as heating. In other words, the entire transient only lasts on the order of 20 µs to 50 us. Using commercial IR cameras to capture such fast transients is not a straightforward task.

There are two major 'difficulties to capture a high-speed transient. First, the transient duration, 20-50 µs, is much faster compare to the IR camera frame speed. The state-of-the-art IR cameras in the market take images at < 1 kHz without windowing. The time interval between each image is still too long (1000 µs). Secondly, the IR detectors in a camera need to have a fixed integration time, usually on the-order of 1 millisecond, to collect photons. This integration time is too long for the microsecond thermal transients. Instead of capturing the peak temperature of the transients, only the average temperature' is obtained. Shorter integration time is possible, but the trade-off is a decrease in temperature resolution.

A practical case was presented to us when the temperature profile of power transistor arrays in an IC device was of interest. Used in a high current short duty pulsed application, power and energy density in the transistor arrays are very high compared to more conventional applications. The temperatures of the transistors were estimated to reach over 150°C within 20 µs. In the process of trying to capture such a transient,. we discovered a third difficulty of the IR imaging system: The precise synchronization of the IR camera is unknown. There is an unexpected delay even when the IR camera is operating

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under "external sync" and "triggering" modes. To our knowledge only one commercial IR camera, the Indigo Phoenix™ system, provides user controlled delay time [2].

Giving the three major difficulties of capturing the high-speed thermal transients, a research project was conducted. Using the existing Raytheon Radiance HS™ IR camera, an incandescent lamp filament, and a special test circuit the timing of the IR camera was systematically studied. The fixed delay time of the IR camera was not on the order of microseconds as expected, but rather on the order of several milliseconds. This delay caused the IR camera to miss the transients even under the "external sync" mode. By constructing precisely controlled delay trigger pulses and running the lamp filament at 5 Hz the heating and cooling curves of the filament were captured. Because the temperature of the filament is over 400°C during the pulse, an integration time of 10 µs was used. This allowed the peak temperature to be captured by sweeping the delay in the heating pulse across the integration time of the camera.

This article describes the study of the IR camera triggering and synchronization mechanisms and presents IR images of power transistor arrays in an IC package. With the use of a microscope lens the IR imaging technique has shown its promising application in the microelectronic industry.

2. DETERMINATION OF THE INTEGRATION DELAY TIME IN AN IR CAMERA

A Raytheon, Radiance HS®, camera was used in this study. Three camera clock modes are available in this camera 1) video, 2) internal clock from computer and 3) external synchronization signals (normally 3-5 volts square waves or pulses). The software allows the user to choose the image acquisition to start at the rising or trailing edge of the external sync signal. The maximum frame speed of the camera is 141 Hz at 256 x 256 pixel format. The integration time can vary from 2 µs to 12 ms. A microscope with 4 X objective lens was used. The field of view of the lens is altered by the position of the focusing ring from 1.4 mm x 1.4 mm to 2.0 mm x 2.0 mm. This results in a spatial resolution of 5.4 µm and 7.8 µm per pixel, respectively.

In our previous study [1], the assumption was that the IR camera starts integration immediately after the triggering signal of the external sync pulse. This assumption held in the past mainly because the thermal transients we studied were on the order of milliseconds and the larger thermal mass also extended the duration of the thermal transients. When presented with a microsecond heating pulse, the IR camera was not able to capture the heating under external sync mode. One clue we observed was random flashing of the device under video or internal clock sync modes. This led us to believe that there is an unknown delay time in the integration circuit. As shown in Figure 1. the expected case is a), in which all the pulses are in sync, but the real case is b), in which a fixed. delay time, t_d, exists.

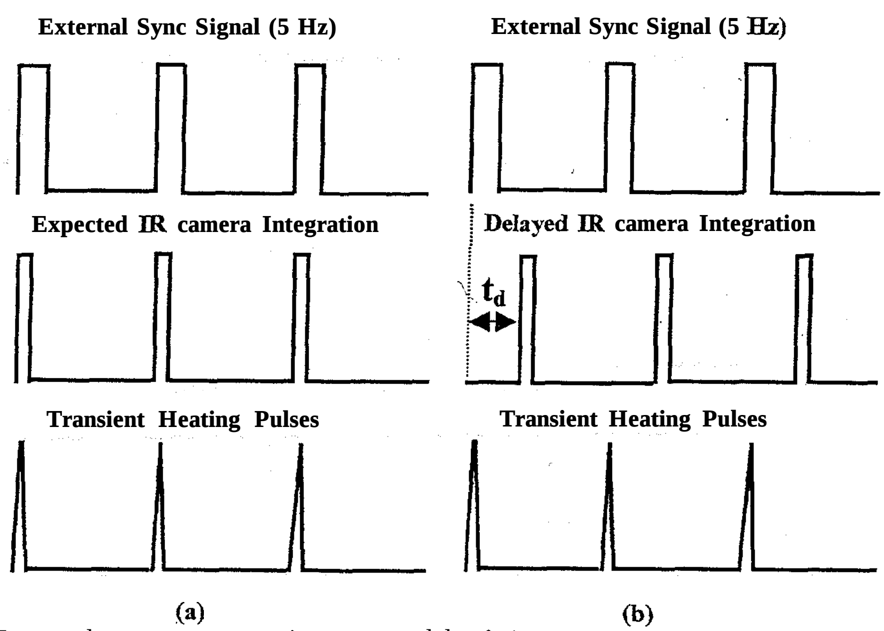

Figure 1 a) Expected IR camera operation with no delay in integration; b) &expected delay in integration

To study the delayed start of integration, an incandescent lamp filament was used. A test circuit was built to provide puls power to the lamp. Using precisely controlled electrical pulse energy techniques the lamp filament is forced to heatup ve fast, typically in less than 5 μs. The cooling however is much slower. Because the pulse energy circuit also provides a lon tail-out energy to keep the filament hot for several milliseconds once the initial heating has occurred. The pulsed pow circuit also allowed the beginning of the lamp temperature rise to be exactly synchronized to external pulses.

To view the filament using the microscope, the top cover of the lamp was cut off. Since we were driving the lamp to onl about 400°C (no visible light from the lamp), the exposure to air did not affect the filament. As shown in Figure 2, a mast signal generator running at 5 Hz was used. It drove a second signal generator with delay function (running on extern triggering mode) to turn the lamp on for 5-20 μs. Thus, the lamp was also running at 5 1%. The 200 ms between each pul was long enough to allow the filament to cool back to room temperature.- The master signal generator was also used as th external sync source for the IR camera. Therefore, the IR camera starts integration after the unknown delay time, t_d.

To find t_d, the sharp rising edge of the filament was used and a delay time was dialed into the second signal generator. Th delayed IR camera integration caught part of the long cooling tail, so a dim filament could be seen without delay. B increasing the delay time systematically, the lamp intensity increased until the peak is passed. Since the heating curve wa very steep, a sudden drop in filament intensity should be observed. The disappearing of the filament was used to match th on-set of the IR camera integration. The pulse sweeping sequence is shown schematically in Figure 3. When the heatin pulse moves closer to the true integration pulse, the IR intensity of the filament should increase accordingly.

As shown in Figure 4, the peak temperature dropped suddenly near 7 ms indicating the true integration delay time. Aft sweeping through the delay range with 1 ms steps, smaller steps, 10 μs, between 6-7 ms were used. For a fixed integratio time (10 μs or 2 μs) the entire temperature profile of the transient can be studied by sweeping the delay in the heating puls Figure 5 show IR images taken'at eight different delay times. The filament intensity increased until 7 ms. Therefore, t_d wa determined to be between 6 ms and 7 ms. To further determine t_d similar tests with 10 μs steps were carried out. As shown i Figure 6, t_d was at 6.98 ms. Note the camera does not start integrating until the end of a frame cycle when the camera runs a maximum speed of 141 Hz (7.092 ms).

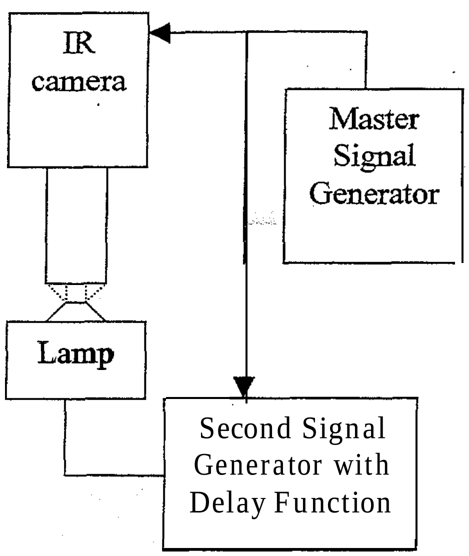

Figure 2. Test set up for a lamp filament.

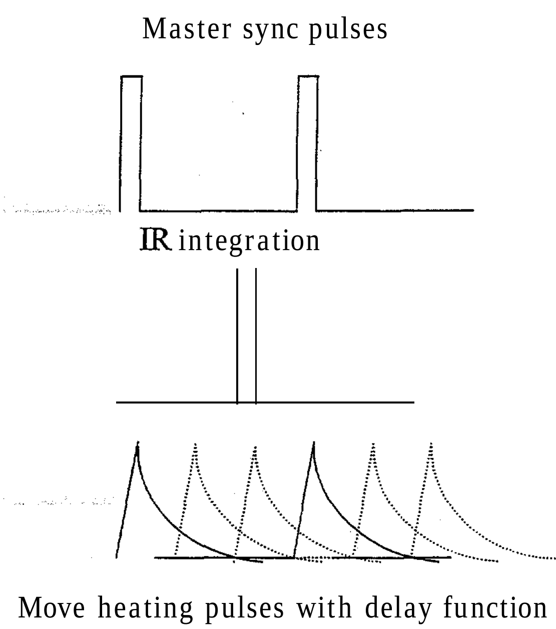

Figure 3. With fixed sync pulses and unknown integration delay, moving the heating pulse will determine the t_d.

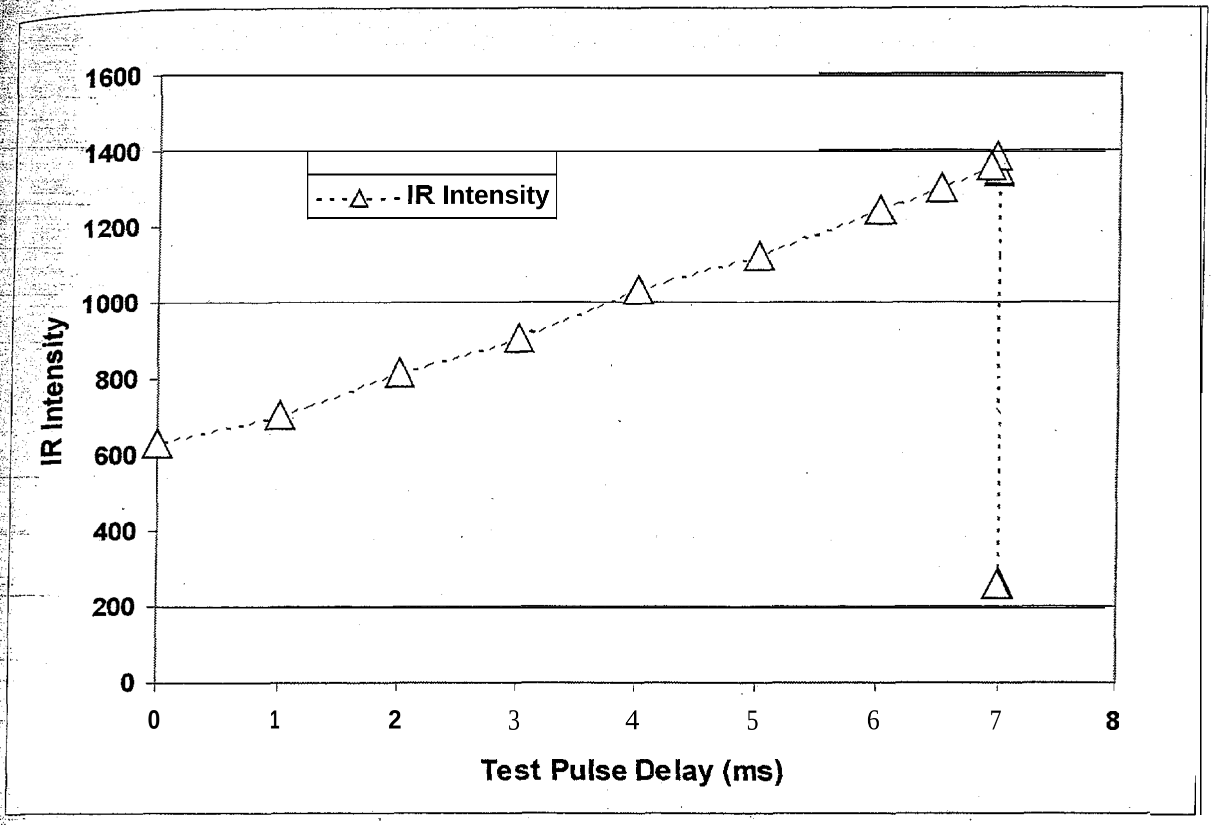

Figure 4. IR intensity vs heating pulse delay showing the integration star@ near 7 ms.

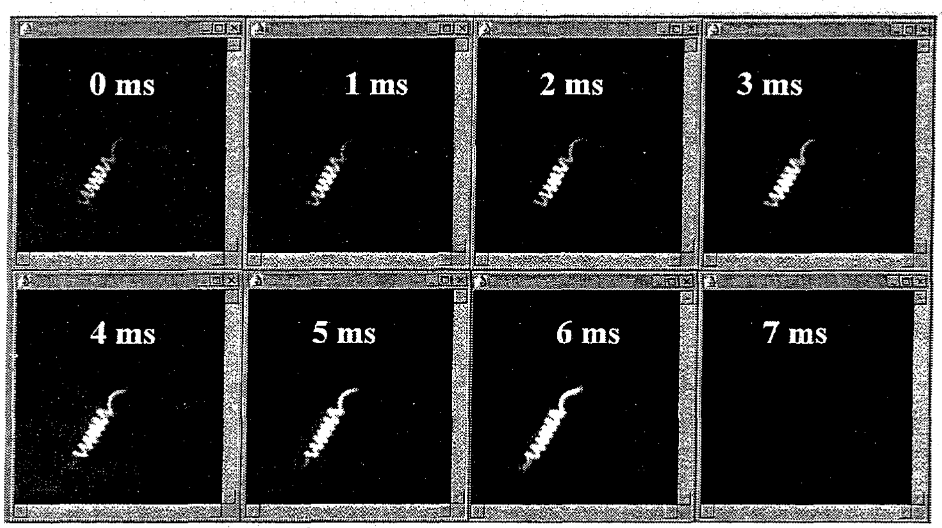

Figure 5. IR images of the filament with 1 ms step increasing delay time.

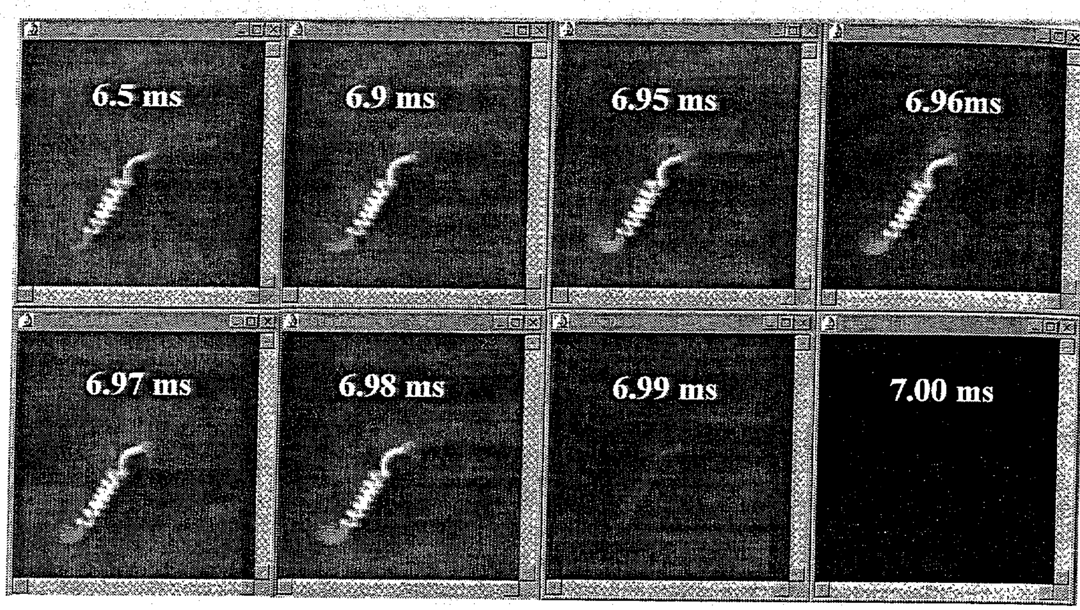

Figure 6. IR images taken with 6.50 ms to 7.00 ms delay time.

3. THERMAL TRANSIENTS IN POWER TRANSISTORS

The tests of the lamp filament determined the delay time of the JR camera. Using a similar set up as shown in Figure 2, the power transistor device was also set up to run at 5 Hz. Although the device was designed to operate in single pulse mode, 200 ms is enough for the device to operate, completely cool down and wait for the next puke. A series of pulse widths and energy were used in the tests. The temperature of the power IC was calibrated by heating an IC unit uniformly up to 150° C with the IR camera set for 10 μs integration time. Snap shots were taken at each temperature. The resulting calibration curve is shown in Figure 7. The data were taken to 150" C because any temperature above that is considered harmful to the ICs. The temperatures below 150° C were determined using second power polynomial curve tit. Above 150" C, the IC temperature was estimated by an extrapolation of the calibration curve.

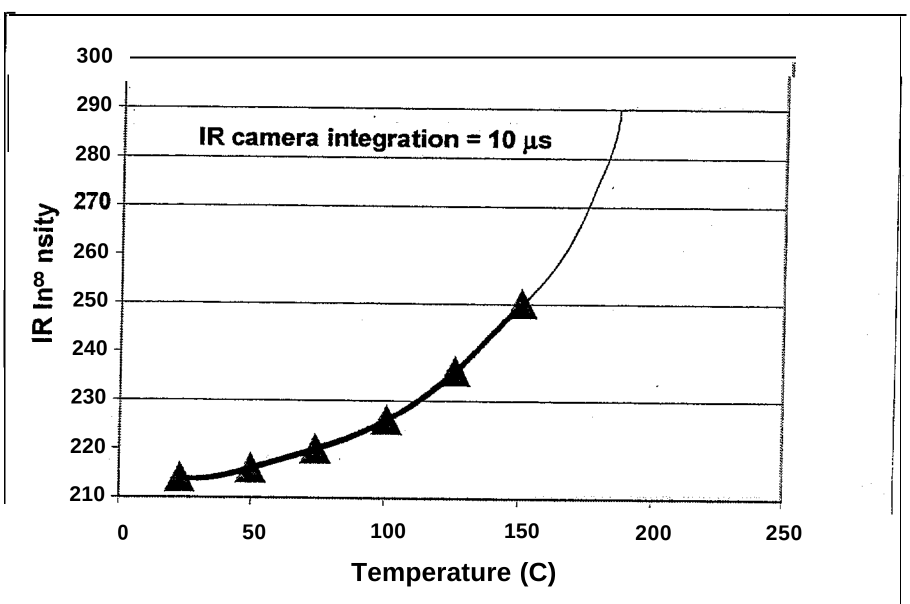

Figure 7. Temperature calibration curve for 10 μs integration

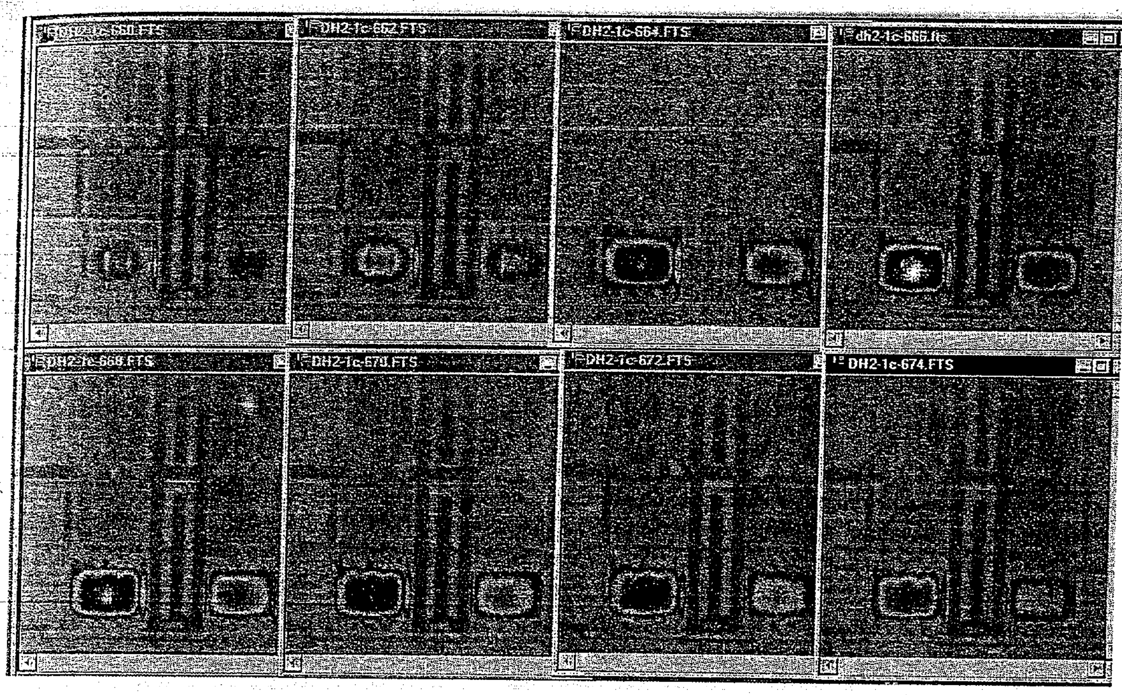

Figure 8. IR images of a power IC show relatively uniform temperature distribution. An obvious energy imbalance was observed between the two units.

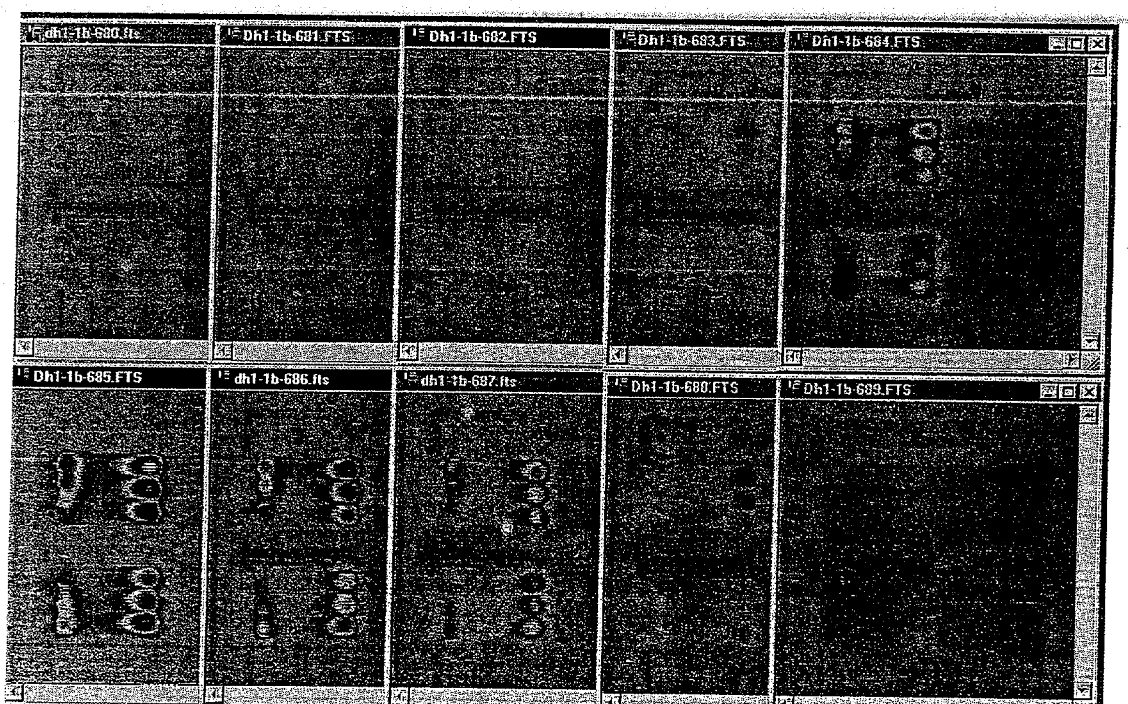

Figure 9. IR images showing non-uniform temperature distributions in power transistors (pulse: 50 μs, 50 A)

The active area of the IC silicon die is about 2 mm x 2 mm. An IR microscope Can image the entire area with abo coverage per pixel. During each test, two matched identical transistor arrays on the IC were powered up. Eac contained multiple transistors. In an ideal case, the same amount of power will be delivered to each array, and eac will heat up uniformly. Figure 8 shows a series of IR images of a power IC with increasing delay time. The tempera the IC increased and then cooled down. Using 10 μs delay time steps the heating and cooling edges were captured. T temperature was about 155" C. The temperature distribution within each transistor array was relatively uniform. The c the unit had the highest temperature and the edges had lower temperature. The IR images showed clearly that one a generally higher temperatures. The thermal image test data provides valuable information to the transistor designe degree of dynamic power matching between the transistors. Based on this test data, the transistor designs will be m slightly to achieve more uniform matching of temperature rise.

In another unit, 50 μs, 50 A, pulses at 5 Hz were used during the tests. The IR camera integration time was 10 μs. As in Figure 9, six consecutive images showed temperature increase, with one showing the highest temperature. Unl device shown in Figure 7, non-uniform temperature distribution within each array was observed. The transistor array much higher temperature (over 165" C) at the ends. Again, this image data provides valuable information to the tr designers indicating how the geometry of the transistor structure should be modified to achieve more uniform temp distributions.

4. CONCLUSIONS

The IR camera integration delay time was determined using an incandescent lamp filament with systematic input pulse In the "external sync" mode, the integration did not start until nearly 7 ms after the rising edge of the sync pulse information was used to adjust the IR camera to capture high-speed transients in power ICs. The thermal images pr evidence of energy imbalance and non-uniform temperature distribution in the transistor units. This image data is u direct design improvements to the transistor geometry to affect an improved dynamic temperature balance.

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