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CONTROL OF SURFACE MOUNTED PERMANENT MAGNET MOTORS WITH SPECIAL APPLICATION TO FRACTIONAL-SLOT MOTORS WITH CONCENTRATED WINDINGS

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Control of Surface Mounted Permanent Magnet Motors with Special Application to Fractional-Slot Motors with Concentrated Windings

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CONTENTS

	Page
LIST OF FIGURES	iv
LIST OF TABLES	v
ACROYNMS	vi
EXECUTIVE SUMMARY	vii
1. INTRODUCTION	1
1.1 BACKGROUND AND SUMMARY	1
1.2 ORGANIZATION OF THE REPORT	3
2. ANALYSIS OF THE PMSM WHEN DRIVEN BY CPA	5
3. ANALYSIS OF THE PMSM WHEN DRIVEN BY DMIC	15
3.1 HIGH-INDUCTANCE PMSM DRIVEN BY CPA	16
3.2 PMSM CURRENT MAGNITUDE MINIMIZATION WHEN DRIVEN BY DMIC	19
3.3 COMPARISON OF MOTOR-CURRENT MAGNITUDE WITH CPA AND DMIC AT HIGH SPEED AND VARIABLE LOAD	24
3.4 STEADY-STATE CONTROL INCLUDING WINDING RESISTANCE AND ROTATIONAL LOSSES	26
3.4.1 Amplitude-Modulation Index and Inverter-Lead Angle for CPA	26
3.4.2 Amplitude-Modulation Index and Inverter-Lead Angle for DMIC	28
4. INVERTER LOSSES	31
4.1 CONDUCTION LOSSES	31
4.2 SWITCHING LOSSES	43
4.3 REVERSE-RECOVERY LOSSES	44
4.4 INVERTER SEMICONDUCTOR SELECTIONS FOR THE MOTOR 1 AND MOTOR 2 DESIGNS AND LOSS-MODEL PARAMETERS	46
4.5 INTEGRATED MOTOR/INVERTER MODEL SIMULATION	47
5. IMPACT OF SUPPLY VOLTAGE, INDUCTANCE, AND INVERTER TOPOLOGY ON DRIVE PERFORMANCE	56
5.1 IMPACT OF MOTOR INDUCTANCE BEING HIGHER THAN “OPTIMAL”	56
5.2 IMPACT OF DC SUPPLY VOLTAGE GREATER THAN THE MINIMUM	59
5.3 CPA VS. DMIC	62
5.4 INVERTER VERSUS CONVERTER-GRADE THYRISTORS IN THE DMIC	65
6. CONCLUSIONS	67
7. REFERENCES	69
APPENDIX A.1: 600 V, 75 A, IGBT MODULE – FAIRCHILE FMG1G75US60H	70

CONTENTS (cont'd)

Page

APPENDIX A.2: 800 V, 45 A, INVERTER-GRADE THYRISTOR MODULE – EUPEC TT46F08 79

APPENDIX A.3: 1400 V, 61 A, CONVERTER-GRADE THRISTOR MODULE – EUPEC TT61N 82

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LIST OF FIGURES

Figure		Page
1	Motor/inverter schematic for PMSM driven by CPA	5
2	Fundamental-frequency model of one phase of a PMSM	6
3	Constant-power performance of the PMSM driven by sinusoidal PWM and CPA	13
4	DMIC inverter topology	15
5	Per-phase fundamental-frequency phasor model for constant-power mode	15
6	Constant-power operation of a PMSM motor comparing CPA control with DMIC	19
7	Constant-power performance of the PMSM driven by DMIC	23
8	RMS motor current vs. power output during high-speed operation of Motor 1 with 146.1 V and 203.8 Vdc supply voltages when driven by CPA or by DMIC	25
9	RMS motor current vs. power output during high-speed operation of Motor 1 and Motor 2 with 203.8 Vdc supply	25
10	Transistor with bypass diode and thyristor equivalents for determining conduction losses	31
11	Per-phase model used to calculate average and rms device currents	33
12	Time-domain simulation of Motor 2 at 540 rpm and 60% rated torque with 207.4 Vdc supply, and a carrier frequency of 8505 Hz	37
13	Time-domain simulation of Motor 2 at 540 rpm, 60% rated torque with 207.4 Vdc supply, and a carrier frequency of 2025 Hz	38
14	Per-phase fundamental-frequency model of the Motor 1 design driven by CPA at 3000 rpm and 1500 W useful output power with rotational losses included	39
15	Time-domain simulation results of the CPA simulator driving the Motor 2 design at 3000 rpm and 1500 W output with rotational losses included	41
16	Per-phase fundamental-frequency model of the Motor 2 design driven by DMIC at 3000 rpm and 1500 W useful output power with rotational losses included	41
17	Time-domain simulation results of the DMIC simulator driving the Motor 1 design at 3000 rpm and 1500 W output with rotational losses included	43
18	Simplified description of switching dynamics during turn-on and turn-off	44
19	Reverse-recovery current and voltage	45
20	Simulation of Motor 1 driven by CPA, operating at full load (6000 W) from a 151 Vdc supply voltage	48
21	Simulation of Motor 1 driven by DMIC, operating at full load (6000 W) from a 151 Vdc supply voltage	50
22	Simulation of Motor 1 driven by CPA, operating at quarter of load (1500 W) from a 151 Vdc supply voltage	52
23	Simulation of Motor 1 driven by DMIC, operating at quarter load (1500 W) from a 151 Vdc supply voltage	54
24	Performance comparison of Motor 1 (with 151 Vdc supply voltage) and Motor 2 (with 208 Vdc supply voltage) when driven by CPA over the full torque-speed envelope	56
25	Comparison of Motor 1 performance when operating from 151 V and 208 Vdc supply voltages when driven by CPA	60
26	Comparison of Motor 1 driven by CPA and DMIC from a 151 Vdc supply voltage	63
27	Efficiency difference between inverter and converter-grade SCRs with Motor 1 driven by DMIC with a 151 Vdc supply voltage	66

LIST OF TABLES

Table		Page
1	Parameters of Motor 1 and Motor 2	3
2	Calculations for Motor 1 and Motor 2	14
3	Comparison of theoretical and simulated Motor 2 and inverter-current magnitudes at 540 rpm, 60% rated torque, and dc supply of 207.4 V	39
4	Typical semiconductor parameters	47

ACRONYMS

ac	alternating current
CPA	conventional phase advance
CPSR	constant power speed ratio
d-axis	direct-axis
dc	direct current
DMIC	dual mode inverter control
emf	electromotive force
IGBT	insulated gate bipolar transistor
Nm	Newton meter
ORNL	Oak Ridge National Laboratory
PMSM	permanent magnet synchronous motor
PWM	pulse width modulation
q-axis	quadrature-axis
rms	root mean square
rpm	revolutions per minute
SCR	silicon controlled rectifier
VSI	voltage-source inverter

EXECUTIVE SUMMARY

It is well known that the ability of the permanent magnet synchronous machine (PMSM) to operate over a wide constant power speed range (CPSR) is dependent upon the machine inductance. Early approaches for extending CPSR operation included adding supplementary inductance in series with the motor and the use of anti-parallel thyristor pairs in series with the motor-phase windings. The motor control method that requires increased inductance is compatible with a voltage-source inverter (VSI) controlled by pulse-width modulation (PWM) and is called the conventional phase advance (CPA) method. The thyristor method has been called the dual mode inverter control (DMIC). Neither of these techniques has met with wide acceptance since they both add cost to the drive system and have not been shown to have attractive cost/benefit ratio. Recently a method has been developed to use fractional-slot concentrated windings to significantly increase the machine inductance. This latest approach has the potential to make the PMSM compatible with CPA without supplemental winding inductance. If the performance of such a drive is acceptable, the method may make the PMSM an attractive option for traction applications requiring a wide CPSR.

A 30 pole, 6 kW, 6000 maximum revolutions per minute (rpm) prototype of the fractional-slot PMSM has been designed, built, and tested at the University of Wisconsin. This machine has significantly more inductance than is typical of regular PMSMs. The prototype is to be delivered in late 2005 to the Oak Ridge National Laboratory (ORNL) for testing and development of a controller that will achieve maximum efficiency. In advance of the test/control development effort, ORNL has used the PMSM models developed over a number of previous studies to study how steady-state performance of high-inductance PMSM machines relates to control issues. This report documents the results of this preliminary investigation.

A major conclusion of this study is that, while a method of incorporating high winding inductance in PMSM design may solve the CPSR problem, it can make it difficult to meet efficiency objectives at medium to high speed especially under less than full-load conditions. Since a traction drive may spend considerable operating time near one half maximum speed, and at approximately one quarter full load, achieving high efficiency under such conditions may be a challenge.

The main problem found with high-inductance machines driven by CPA is that the motor current at high speed depends solely on machine parameters and is virtually independent of the load level and the direct current (dc) supply voltage. Thus, the motor current is virtually the same at no load as at full load resulting in poor efficiency at less than full-load conditions. The DMIC technology is shown to produce motor current at high speed that is proportional to load and has the potential to maintain high efficiency at full and partial load conditions.

An important concern with the DMIC is the reverse-recovery losses of the thyristors at high speed. Because the turn-off of the thyristors in the DMIC is naturally soft, it is possible that economical converter-grade components can be used provided the fundamental switching frequency is on the order of 1 kHz or less. The cost and additional losses associated with the thyristors used in the DMIC may be offset by efficiency enhancement.

The amount of inductance that enables the motor to achieve infinite CPSR is given by

$$L_{\infty} = \frac{E_b}{\Omega_b I_R}$$

where

E_b is the root mean square (rms) magnitude of the line-to-neutral back-electromotive force (emf) at base speed,

Ω_b is the base speed in electrical radians per second, and

I_R is the rms current rating of the motor windings.

The prototype machine that is to be delivered to ORNL has about 1.7 times as much inductance. The inventors of the fractional-slot concentrated-winding method, who designed the prototype machine, remarked that they were "too successful" in incorporating inductance into their machine and that steps would be taken to modify the design methodology to reduce the inductance to the optimum value. This study shows a significant advantage of having the higher inductance rather than the optimal value because it enables the motor to develop the required power at lower current thereby reducing motor and inverter losses and improving efficiency. While an inductance higher than the value cited above is warranted, it still does not ensure that the motor current is proportional to load; consequently, the problem of low efficiency at high speed and partial load is not resolved but is only mitigated.

A common definition of "base speed" is the speed at which the voltage applied to the motor armature is equal to the magnitude of the back-emf. The results in this study indicate that the dc supply voltage should be adequate to drive rated current into the motor winding at the specified base speed. At a minimum, this requires sufficient voltage to overcome not only the back-emf but also the voltage drop across the internal impedance of the machine. For a high-inductance PMSM, the internal impedance at base speed can be considerable and substantial additional voltage is required to overcome the internal voltage drop. It is further shown that even more voltage than the minimum required for injecting rated current at base speed can be beneficial by allowing the required power to be developed at lower current, which reduces losses in the motor and inverter components. Further, it is shown that the current is minimized at a unique speed which varies with voltage; consequently, there may be room for optimization if the drive spends a substantial amount of its operating life at partial load.

In this study, fundamental-frequency phasor models are developed for a synchronous PMSM and the two control systems that drive them, which are CPA and DMIC. The models are compared with detailed simulations to show their validity. The findings of this study are demonstrated on two example motors, one with inductance sufficient to allow infinite CPSR and one with inductance 1.7 times higher. The results, which compare the two control systems, will be used to design a traction-drive control system with optimized efficiency to drive the fractional-slot motor with concentrated windings. The goal is to meet the FreedomCAR and Vehicle Technologies specifications.

1. INTRODUCTION

It is well known that the ability of the permanent magnet synchronous machine (PMSM) to operate over a wide constant power speed range (CPSR) is dependent upon the machine inductance [1,2,3,4,5]. Early approaches for extending CPSR operation included adding supplementary inductance in series with the motor [1] and the use of anti-parallel thyrsistor pairs in series with the motor-phase windings [5]. The increased inductance method is compatible with a voltage-source inverter (VSI) controlled by pulse-width modulation (PWM) which is called the conventional phase advance (CPA) method. The thyristor method has been called the dual mode inverter control (DMIC). Neither of these techniques has met with wide acceptance since they both add cost to the drive system and have not been shown to have an attractive cost/benefit ratio. Recently a method has been developed to use fractional-slot concentrated windings to significantly increase the machine inductance [6]. This latest approach has the potential to make the PMSM compatible with CPA without supplemental external inductance. If the performance of such drive is acceptable, then the method may make the PMSM an attractive option for traction applications requiring a wide CPSR.

A 30 pole, 6 kW, 6000 maximum revolutions per minute (rpm) prototype of the fractional-slot PMSM design has been developed [7]. This machine has significantly more inductance than is typical of regular PMSMs. The prototype is to be delivered in late 2005 to the Oak Ridge National Laboratory (ORNL) for testing and development of a suitable controller. In advance of the test/control development effort, ORNL has used the PMSM models developed over a number of previous studies to study the steady-state performance of high-inductance PMSM machines with a view towards control issues. The detailed steady-state model developed includes all motor and inverter-loss mechanisms and will be useful in assessing the performance of the dynamic controller to be developed in future work. This report documents the results of this preliminary investigation.

1.1 BACKGROUND AND SUMMARY

The late Peter Wood, a well known figure in the field of power electronics, once characterized the nature of problem solving in power electronics as akin to eliminating bulges in a bag of water. If a particular bulge in the bag represents a problem and depressing the bulge represents a solution then one needs to be aware that while the target bulge may be gone, another bulge may have surfaced some where else on the bag. A major conclusion of this study is that while a method of incorporating high winding inductance in PMSM design may solve the CPSR problem it can make it difficult to meet efficiency objectives at medium to high speed, especially under less than full-load conditions. Since a traction drive may spend considerable operating time near one half maximum speed, and at approximately one quarter full load, the lack of high efficiency under such conditions may be a problem.

The main problem found with high-inductance machines driven by CPA is that the motor current at high speed depends solely on machine parameters and is virtually independent of load level and the direct current (dc) supply voltage. Thus, the motor current is virtually the same at no load as at full load resulting in poor efficiency at less than full-load conditions. The DMIC technology is shown to produce a motor current at high speed that is proportional to load and has the potential to maintain high efficiency at full and partial load conditions [8]. However, an important concern with the DMIC is found to be the reverse-recovery losses of the thyristors at high speed. Because the turn-off of the thyristors in the DMIC is naturally soft, it is possible that economical converter-grade components can be used provided the fundamental switching frequency is on the order of 1 kHz or less. The high-pole count (30 poles) of the prototype motor results in a fundamental rate of 1.5 kHz at top speed of 6000 rpm and results in substantial recovery losses in the thyristors. The reverse-recovery losses can be reduced by using inverter-grade components which are available but at higher cost. The cost and additional losses associated with the thyristors used in the DMIC may be offset by efficiency enhancement.

Another significant issue regarding high-inductance PMSMs uncovered in this study involves the amount of inductance required to meet CPSR requirements. It is generally believed that there is an "optimum value" for field weakening that is given by

$$L_\infty = \frac{E_b}{\Omega_b I_R}$$

where

E_b is the root mean square (rms) magnitude of the line-to-neutral back-emf at base speed, Ω_b is the base speed in electrical radians per second, and
I_R is the rms current rating of the motor windings.

The prototype machine that is to be delivered to ORNL has about $1.7L_\infty$. The inventors of the fractional-slot concentrated-winding method, who designed the 6-kW prototype machine, remarked that they were "too successful" in incorporating inductance into their machine and that steps would be taken to modify the design methodology to reduce the inductance to the optimum value. This study will show a significant advantage of having the higher inductance rather than the "optimal" value. Specifically, it is shown that the higher inductance enables the motor to develop the required power at lower current thereby reducing motor and inverter losses and improving efficiency. While an inductance higher than the value cited above is warranted, it still does not make the motor current proportional to load. Consequently, the problem of low efficiency at high speed and less than full load is not resolved, it is only mitigated.

A final point uncovered in this study concerns the dc supply voltage that provides the underlying source for the traction drive. A common definition of "base speed" is the speed at which the voltage applied to the motor armature is equal to the magnitude of the back-emf. The results in this study indicate that the dc supply voltage should be adequate to drive rated current into the motor winding at the specified base speed. At a minimum, this requires sufficient voltage to overcome not only the back-emf but also the voltage drop across the internal impedance of the machine. For a high-inductance PMSM, the internal impedance at base speed can be considerable and substantial additional voltage is required to overcome the internal voltage drop. It is further shown that even more voltage than the minimum required for injecting rated current at base speed can be beneficial. In particular, this allows the required power to be developed at lower current and reducing losses in the motor and in the inverter components. Further, it is shown that the current is minimized at a unique speed which varies with voltage. Consequently, there may be room for optimization. For example, if the drive spends a substantial amount of its operating life in the vicinity of one half of maximum speed then it can be desirable to choose a dc supply voltage which causes the motor current to achieve its minimum value at half full speed.

The findings of this study are demonstrated on two "example motors" whose parameters are given in Table 1. The motor referred to as Motor 2 is patterned after the high-inductance prototype that is to be delivered to ORNL. The motor referred to as Motor 1 has the "optimal" inductance value as indicated by the above formula. The parameters of the two cases are identical except for the winding inductance. The parameters in Table 1 were taken from [9].

Table 1. Parameters of Motor 1 and Motor 2

Parameter	Motor 1	Motor 2
Number of poles	30	30
Base speed	900 rpm	900 rpm
Top speed	6000 rpm	6000 rpm
CPSR requirement	6.667:1	6.667:1
Back-emf magnitude at base speed, Eb (rms volts per phase)	46.5 @ 900 rpm	46.5 @ 900 rpm
Voltage constant, Kv (rms volts per elec. rad/sec)	0.03289	0.03289
Rated power	6 kW	6 kW
Rated torque	63.66 Nm	63.66 Nm
Rated rms current	43.0 A	43.0 A
Resistance per phase	71 mΩ	71 mΩ
Inductance per phase	765 μH	1300 μH
Rotational losses $P_{rot}(n)$ @ n = rpm/900		
1000 rpm (n = 1.11)	8.3 W	8.3 W
2000 rpm (n = 2.22)	33.3 W	33.3 W
3000 rpm (n = 3.33)	75 W	75 W
4000 rpm (n = 4.44)	133.3 W	133.3 W
5000 rpm (n = 5.56)	208.3 W	208.3 W
6000 rpm (n = 6.67)	300 W	300 W

1.2. ORGANIZATION OF THE REPORT

The main body of the report consists of Sections 2–6. Sections 2 and 3 present phasor models of the PMSM when driven by CPA and DMIC respectively. These models allow simple analysis of steady-state operation without resorting to a detailed time-domain simulation that includes PWM switching operations. Since the DMIC was originally developed for low-inductance machines, special consideration is given to the implications of using the DMIC in combination with a high-inductance PMSM. It is shown that the DMIC provides for motor-current magnitude minimization where the rms current is directly proportional to load. This enables the DMIC to maintain high efficiency at light load conditions and is in sharp contrast with the CPA where the motor current is virtually independent of load resulting in poor efficiency under low-load conditions. The amplitude modulation and inverter-lead angle required by PWM to support any speed/load combination is developed in Section 3.4 for both the CPA and DMIC drives. Inverter-loss modeling is presented in Section 4 where inverter-component losses are calculated based on the solution of the phasor model of the motor. Expressions are developed to resolve the solution of the phasor model into the conduction, switching, and reverse-recovery losses of the inverter components. These expressions allow inverter losses to be estimated without time-domain simulation of the PWM. The motor/inverter models are integrated and used to study the control and efficiency of both the CPA and DMIC drives. It is shown that the efficiency of the CPA and DMIC drives for the example motors are almost the same during high-speed operation at full load; but, the DMIC is clearly higher efficiency during high speed/moderate to light load conditions. Section 5 considers the impact of motor inductance, dc supply voltage, and inverter configuration (CPA or DMIC) on current, losses, and efficiency performance. It is shown that for CPA drives the efficiency is enhanced by having the motor inductance exceed the accepted "optimal" value. The efficiency improvement is through reduction in the motor current resulting from the higher reactance. A dc supply voltage higher than the minimum needed

to support rated torque at base speed is shown to improve high-speed efficiency. For the DMIC inverter, it is shown that the converter-grade thyristor reverse-recovery losses can be large during high-speed operation, especially for pole counts as large as the example motors which have 30 poles. When the reverse-recovery losses are too large they can be reduced using inverter-grade thyristors, but this will entail higher cost. Finally, Section 6 contains the conclusions of this work.

The next section contains a discussion of the means for theoretical analysis of the performance of the PMSM driven by CPA.

2. ANALYSIS OF THE PMSM WHEN DRIVEN BY CPA

Figure 1 shows a schematic of the three-phase PMSM driven by a VSI as used in CPA. The figure also defines some of the parameters and notation used in this discussion. The resistors R and R_{rot} represent the copper losses and the speed sensitive rotational losses respectively. The value of R_{rot} can be calculated for any given speed using knowledge of the back-emf rms magnitude and the watt value of rotational losses as contained in Table 1. At relative speed n, the value of $R_{rot}(n)$ is calculated as

$$R_{rot}(n) = \frac{3\left(nE_b\right)^2}{P_{rot}(n)} \quad . \tag{1}$$

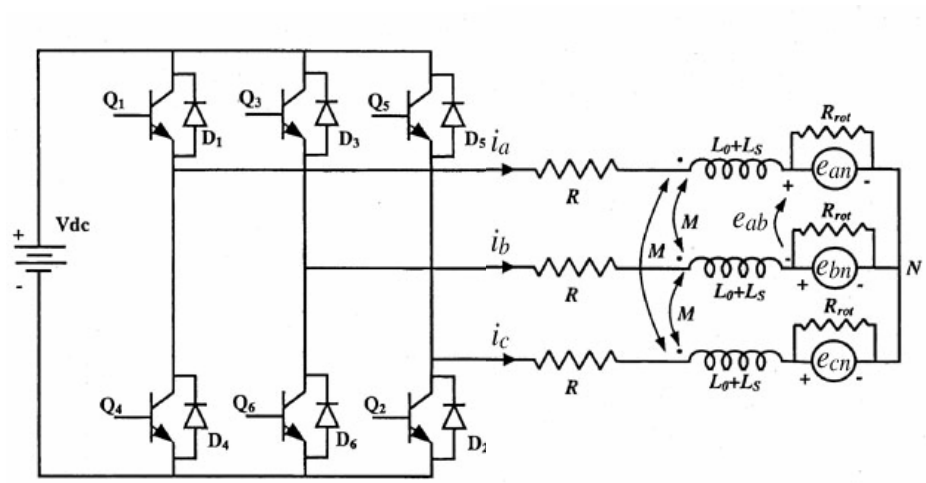


Fig. 1. Motor/inverter schematic for PMSM driven by CPA.

p = number of poles
N = actual mechanical rotor speed in rpm
N_b = mechanical base speed in rpm
n = relative speed = $\dfrac{N}{N_b}$
Ω_b = base speed in electrical radians/sec
= $\dfrac{p}{2} \cdot \dfrac{2\pi N_b}{60}$
Ω = actual rotor speed in electrical radians/sec
= $n\Omega_b$
E_b = rms magnitude of the phase-to-neutral emf at base speed
I_R = rated rms motor current
P_R = rated output power = $3E_bI_R$
L_s = self inductance per phase
L_o = leakage inductance per phase
M = mutual inductance
L = equivalent inductance per phase = $L_o + L_s + M$
R = winding resistance per phase

v_{an} = applied phase A to neutral voltage
e_{an} = phase A to neutral back-emf
e_{ab} = phase A to phase B (line-to-line) back-emf.

The detailed technical assessment of Motor 1 and Motor 2 includes the evaluation of losses, not only in the motor but also in the inverter. The main focus in Sections 2 and 3 is on CPSR performance and current-magnitude control and the discussion is greatly simplified by neglecting the losses. Unless otherwise specified, the discussion in the remainder of this section and the next assumes that the winding resistance, R, is zero and the rotational-loss resistance, R_{rot}, is infinite.

The transistors in the inverter of Fig. 1 are typically controlled by sinusoidal PWM which uses a triangular carrier wave and three sinusoidal reference waves to decide the switching pattern. A detailed PSPICE simulator is available to analyze the performance of the PMSM as displayed in Fig. 1 and controlled by PWM when operating at constant speed. Since the objective here is to focus on CPSR, efficiency, and steady-state control, the details of PWM control are intentionally omitted and a simplified per phase fundamental-frequency model is developed. Such a model is shown in Fig. 2 which is a phasor model of the motor drive at a selectable but constant speed.

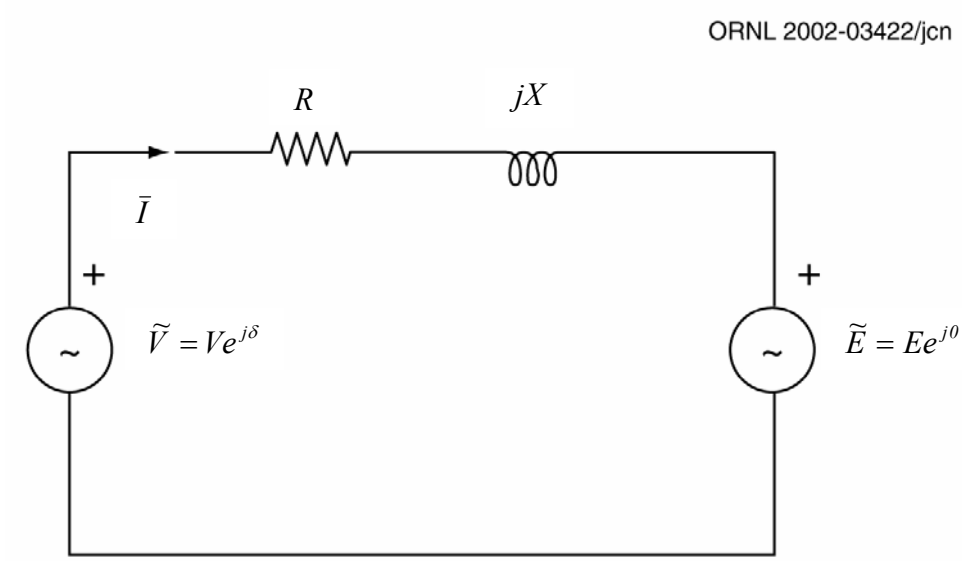


Fig. 2. Fundamental-frequency model of one phase of a PMSM.

In the per phase model of Fig. 2, the phasor $\overline{V}$ represents the fundamental frequency line-to-neutral voltage applied to the motor by the inverter. V is the rms magnitude and δ is the inverter-lead angle. Phasor $\overline{E}$ represents the phase-to-neutral motor back-emf and is chosen as the reference phasor, such that the angle of $\overline{E}$ is zero. The magnitude of the emf is linear in motor speed and the voltage constant, K_v, has units of rms volts per electrical radian per second. Thus, the rms value of the back-emf at any speed is given by

$$
\begin{aligned}
E &= K_v \Omega \\
&= \frac{\Omega}{\Omega_b} K_v \Omega_b \ , \\
&= n E_b
\end{aligned}
\tag{2}
$$

where

E_b is the rms magnitude of the line-to-neutral back-emf at base speed and
n is relative speed.

Similarly, the motor reactance can be expressed as

$$
\begin{aligned}
X &= \Omega L \\
&= \frac{\Omega}{\Omega_b} \Omega_b L \ , \\
&= n X_b
\end{aligned}
\tag{3}
$$

where X_b is the reactance at base speed.

We should distinguish between "base speed" and "true base speed." Base speed is the highest speed at which rated torque is required, and the power developed at this speed is the rated power of the motor drive. True base speed is the highest speed at which rated torque can be developed. The true base speed is exactly the same as base speed when the dc supply voltage is selected as the minimum value that permits rated torque to be developed at the base speed and is given by

$$
V_{dc-\min} = \frac{\pi}{\sqrt{2}} \sqrt{E_b^2 + \left(X_b I_R \right)^2} \ . \tag{4}
$$

This expression assumes that the PWM control will be in full over-modulation when developing rated torque at base speed. Note that Eq. (4) insures that sufficient dc supply voltage is provided so that at base speed the driving voltage is sufficient to overcome the back-emf voltage <u>and</u> the internal impedance of the motor while supplying the rated current to the windings. For Motor 1 of Table 1 with an inductance of $765 \mu H$, the value of Eq. (4) is 146.1 V, while for Motor 2 having inductance of $1300 \mu H$, the required dc supply is 203.8 V. This difference in dc supply voltage is not particularly significant since when both motors develop rated power, the higher supply voltage will operate at a lower current. If the dc supply voltage is less than $V_{dc-\min}$, it will not be possible to develop rated torque at the specified base speed; i.e., the true base speed will be less than the specified value. If the dc supply voltage is larger than $V_{dc-\min}$, then the true base speed is larger than the specified value. Letting the true base speed be denoted as n_{bt} we have

$$
n_{bt} = \frac{V_{dc}}{V_{dc-\min}} \cdot n_b \ . \tag{5}
$$

When a dc supply larger than the minimum is used, the rated torque can be developed at a speed higher than base speed resulting in greater power-conversion capability; however, the drive control can be configured to preclude using this extra capability; i.e., the control can restrict the maximum torque above the base speed. Even though control may be used to constrain the torque-speed envelope, the addition of surplus dc supply voltage may allow reduced current magnitude at high speed, thereby reducing inverter and motor copper losses and improving efficiency. This possibility is discussed further in Section 3.

Up to base speed, the magnitude of the applied voltage, V, and the lead angle, δ, can be adjusted allowing the motor-current phasor to be put in phase with the back-emf. This maximizes the torque produced per amp. Voltage magnitude, V, and lead angle, δ, required to support any relative speed below base speed, $n \le 1$, and rms current, I, is found from

$$\begin{aligned}\bar{V} &= nE_b + jnIX_b \\ &= \sqrt{(nE_b)^2 + (nIX_b)^2}\angle \tan^{-1}\left(\frac{nIX_b}{nE_b}\right) \\ &= n\sqrt{E_b^2 + (X_b I)^2}\angle \tan^{-1}\left(\frac{IX_b}{E_b}\right) \\ &= V\angle\delta\end{aligned} . \tag{6}$$

The rms magnitude of $\bar{V}$ increases with speed and is limited by the available dc supply voltage. Assuming that the dc supply voltage is the minimum value and that full over-modulation is allowed, the maximum magnitude is obtained at base speed where $n = 1$ and rated rms motor current is $I = I_R$, then

$$V_{\max} = \sqrt{(E_b)^2 + (I_R X_b)^2} = \sqrt{(E_b)^2 + (I_R \Omega_b L)^2} . \tag{7}$$

Similarly, the lead angle δ at base speed and rated current is given by

$$\delta = \tan^{-1}\left(\frac{I_R X_b}{E_b}\right). \tag{8}$$

The power developed at base speed and rated current is the rated power of the motor and since the current is in phase with the back-emf we have

$$P_R = 3E_b I_R . \tag{9}$$

Let us now restrict our attention to operation above base speed such that $n > 1$ and $V = V_{\max}$. Neglecting the armature resistance, the phasor current of the motor is

$$\begin{aligned}\bar{I} &= \frac{V_{\max}}{nX_b}\sin\delta + j\left[\frac{E_b}{X_b} - \frac{V_{\max}}{nX_b}\cos\delta\right], \\ &= I_r + j\, I_x\end{aligned} \tag{10}$$

where I_r is the component of current in phase with the back-emf and produces useful torque. This component is like the quadrature-axis (q-axis) current in the d-q model and can be referred to as the torque-producing component. I_x is the component of current that is orthogonal to the back-emf and results in no net torque production. This component is like the direct-axis (d-axis) current in the d-q model and can be referred to as the field-weakening current. The total motor current has rms magnitude

$$\begin{aligned} I &= \sqrt{I_r^2 + I_x^2} \\ &= \frac{\sqrt{V_{\max}^2 - n2V_{\max}E_b\cos\delta + n^2E_b^2}}{nX_b} \end{aligned} \quad (11)$$

The total power injected into the motor by the inverter is

$$P_{in} = 3\,\mathrm{Re}(\overline{V}\ \overline{I}^*) = \frac{3V_{\max}E_b}{X_b}\sin\delta\,, \quad (12)$$

while the total power converted by the motor is

$$\begin{aligned} P_m &= 3\,\mathrm{Re}(\overline{E}\overline{I}^*) = \frac{3V_{\max}E_b}{X_b}\sin\delta \\ &= P_{\max}\sin\delta \end{aligned}\,, \quad (13)$$

where

$$P_{\max} = 3\frac{V_{\max}E_b}{X_b} \quad (14)$$

is the maximum power that can possibly be converted, which corresponds to the lead angle being 90°. Since we have neglected the winding resistance, P_{in} equals P_m and the common value is

$$\begin{aligned} P_m &= P_{in} = \frac{3V_{\max}E_b}{X_b}\sin\delta \\ &= P_{\max}\sin\delta \end{aligned}\,. \quad (15)$$

This expression shows that it is easy to control the motor to deliver rated power above base speed. All that is necessary is that the inverter-lead angle, δ, be held fixed at that value which causes P_m in Eq. (15) to be equal to the rated value, P_R, given in Eq. (9) that is

$$\begin{aligned} \delta &= \sin^{-1}\left(\frac{X_bP_R}{3V_{\max}E_b}\right) \\ &= \cos^{-1}\left(\frac{E_b}{V_{\max}}\right) \end{aligned}\,. \quad (16)$$

While constant lead angle control allows the PMSM to operate at constant power above base speed, it is not a certainty that doing so results in operating within the rated current. The critical factor is the motor inductance as shown below.

Equation (11) gives the rms motor current, I, when operating at any speed above base speed. Using lead angle, δ, from Eq. (16) so that rated power is produced, we require that the rms current in Eq. (11) be no greater than the rated value I_R, that is

$$\begin{aligned} I &= \frac{\sqrt{V_{\max}^2 - 2nV_{\max}E_b\cos\delta + n^2E_b^2}}{nX_b} \\ &= \frac{\sqrt{V_{\max}^2 + n(n-2)E_b^2}}{n\Omega_b L} \\ &\le I_R \end{aligned} . \tag{17}$$

There is a well defined speed at which the current magnitude is minimal. Setting the derivative of Eq. (17) with respect to relative speed n equal to zero and solving for this speed yields

$$n_{\min} = \frac{V_{\max}}{E_b\cos\delta} . \tag{18}$$

With this value of n substituted into Eq. (17), the minimum current is found to be

$$I_{\min} = \frac{P}{3V_{\max}} . \tag{19}$$

Note that this minimum-current magnitude is independent of motor parameters and depends linearly on the developed power and inversely on the maximum fundamental inverter voltage. Since $V_{\max}$ can be increased by raising the dc supply voltage, there may be reduction in motor and inverter losses when V_{dc} is increased above the minimum level required to sustain rated power at base speed. It can be shown that for speeds less than $n_{\min}$, the inverter-power factor is lagging; while for speeds above $n_{\min}$, the inverter-power factor is leading. Thus, the inverter operates at the optimum unity power-factor condition at only one speed, namely $n_{\min}$. For Motor 1 of Table 1, the values of $n_{\min}$ and $I_{\min}$ are 2.00 (1800 rpm) and 30.41 A; while for the higher inductance Motor 2, the corresponding values are 3.89 (3500 rpm) and 21.81 A respectively.

Observe from Eqs. (10) and (17) that, as the speed approaches infinity, the motor-current magnitude approaches a limiting value given by

$$\lim_{n\to\infty} I_r = \lim_{n\to\infty} \frac{V_{\max}}{nX_b}\sin\delta = 0$$

$$\lim_{n\to\infty} I_x = \lim_{n\to\infty}\left(\frac{E_b}{X_b} - \frac{V_{\max}}{nX_b}\cos\delta\right) = \frac{E_b}{X_b} = \frac{E_b}{\Omega_b L} \quad . \tag{20}$$

$$\lim_{n\to\infty} I = \lim_{n\to\infty}\frac{\sqrt{V_{\max}^2 + n(n-2)E_b^2}}{nX_b} = \frac{E_b}{X_b} = \frac{E_b}{\Omega_b L} = I_{CH}$$

The limiting rms current magnitude in Eq. (20) is called the "characteristic current" [6] denoted as I_{CH}. The characteristic current in Eq. (20) is larger than the minimum current in Eq. (19). For Motor 1 in Table 1, the characteristic current evaluates to 43.0 A, which is exactly the same as the rated current of the motor; while for Motor 2 the characteristic current is 25.3 A, which is less than rated current. Note that the characteristic current depends only on motor parameters (E_b, Ω_b, L) and is independent of motor load and dc supply voltage. Also note that at high speeds, the torque-producing current, I_r, approaches zero so that the limiting current at high speed is solely due to field-weakening current, I_x. This result has a positive implication for being able to operate over a wide CPSR while remaining within the motor-current rating. Unfortunately, there is also an adverse implication towards efficiency when operating at high speed and at less than full load. The impact on efficiency is considered later. At the moment, we consider the positive impact on CPSR when the machine inductance is sufficiently large.

If we require the limiting rms current in Eq. (20), which is the characteristic current, to be less than or equal to the rated current, I_R, then we have an inductance requirement that yields an infinite CPSR, which is

$$L_\infty = \frac{E_b}{\Omega_b I_R} \, . \tag{21}$$

This inductance value is sometimes cited as the "optimal" value for field weakening [6]. Any PMSM having an inductance with the value in Eq. (21) or higher will have an unlimited CPSR. Applying Eq. (21) to the parameters of the example motors in Table 1 where both machines have $E_b = 46.5$ V, $\Omega_b = 1413.7$ elec. rad/sec, $I_R = 43.0$ A, the value of L_∞ is found to be 765 μH which is the per phase inductance of Motor 1. Motor 2 has an inductance of 1300 μH which exceeds the "optimal" value by a factor of 1.7. The assertion that the inductance in Eq. (21) is optimal is tied to a notion of base speed where the voltage magnitude applied by the inverter is maximal and is exactly equal to the magnitude of the back-emf. When this is the case,

$$V_{\max} = E_b \Rightarrow V_{dc} = \frac{\pi E_b}{\sqrt{2}} \, , \tag{22}$$

and from Eq. (14)

$$P_{\max} = \frac{3V_{\max}E_b}{\Omega_b L_\infty} \equiv P_R \, . \tag{23}$$

In this case, the rated power is the maximum power that can be developed. If $V_{\max}$ is restricted to the value E_b, then any machine with an inductance larger than L_∞ would not be able to develop rated power at high speed. Although not shown here, when the dc supply is restricted as in Eq. (22), a motor with the "optimal inductance" would be able to develop rated power at high speed but not at base speed. A motor with an inductance larger than L_∞ wouldn't be able to develop rated power at base speed or at high speed. The restriction on the dc supply such that the maximum applied voltage balances the back-emf at base speed is highly artificial. It is reasonable that the applied voltage at base speed be sufficient to overcome not only the back-emf but also the voltage drop across the internal impedance at base speed, as is the case when the dc supply is determined using Eq. (4). When the dc supply is selected by Eq. (4), there will be sufficient voltage to develop rated power at base speed and a surplus power capability at high speed, that is $P_{\max}$ will exceed P_R. If desired, the surplus power capability can be made inaccessible by the control system.

For a finite CPSR requirement, the inequality in Eq. (17) at a relative speed, n, equal to the CPSR, yields a minimum requirement on the motor inductance,

$$L_{\min} = \frac{\sqrt{V_{\max}^2 + CPSR\left(CPSR - 2\right)E_b^2}}{CPSR\,\Omega_b I_R}. \tag{24}$$

And when $V_{\max}$ is determined from Eq. (7) and substituted into Eq. (17), the equivalent requirement is

$$L_{\min} = \sqrt{\frac{CPSR - 1}{CPSR + 1}} * \frac{E_b}{\Omega_b I_R} = \sqrt{\frac{CPSR - 1}{CPSR + 1}} * L_\infty . \tag{25}$$

This expression shows that even for a modest finite CPSR, such as 4:1, the minimum inductance is $0.77 L_\infty$, which is a significant fraction of inductance for infinite CPSR.

The CPSR performance envelopes of Motor 1 and Motor 2, when driven by CPA, are shown in Fig. 3 with winding resistance, rotational losses, and inverter losses neglected. Both motors have an infinite CPSR. However note that the higher inductance motor, Motor 2 with 1300 μH per phase, operates at a lower current when developing the 6 kW rated power at high speed. It is shown in Section 3.3 that the lower characteristic current/high-inductance machine, Motor 2, has higher efficiency at full and partial load than the lower inductance machine, Motor 1. However, the part load efficiency of both of these examples can be quite poor since the motor current approaches the characteristic value at high speed independent of load.

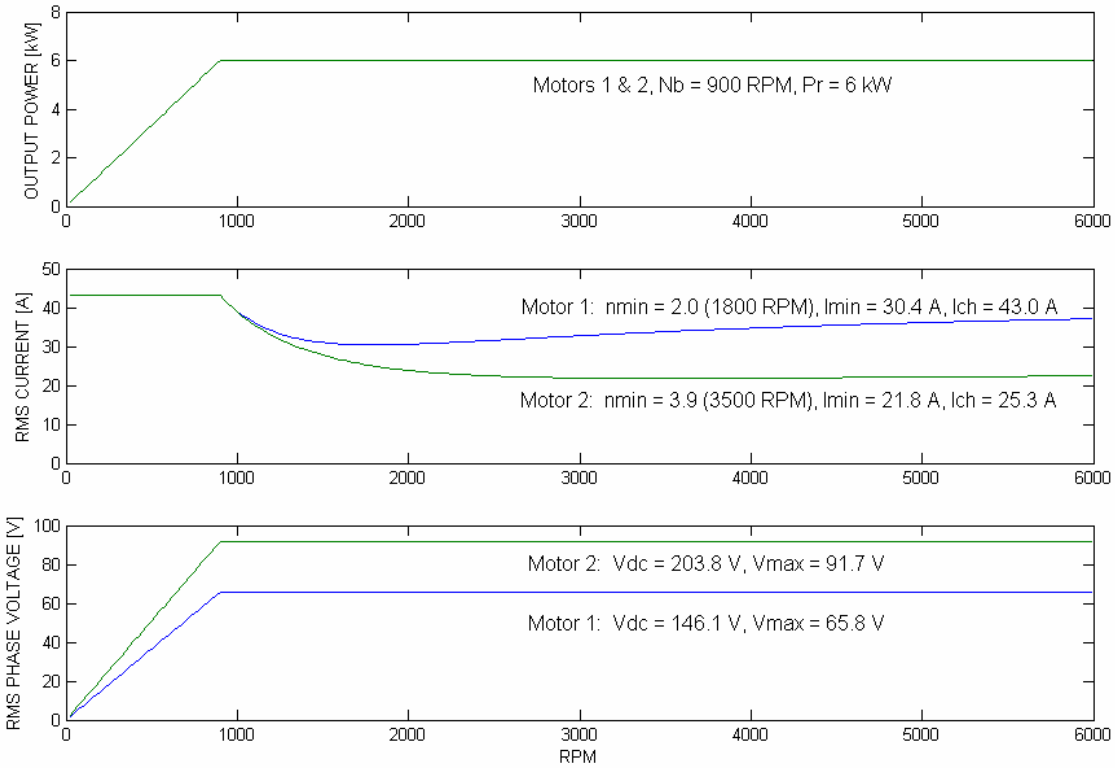


Fig. 3. Constant-power performance of the PMSM driven by sinusoidal PWM and CPA.

In summary, the key parameter in determining the CPSR capability of the sinusoidal back-emf PMSM when driven by CPA is the motor inductance.

To illustrate the use of the various formulas, the design parameters of the Motor 1 and Motor 2 designs from Table 1 are applied to Eqs. (4), (7), (14), (18), (19), (20), (21), (23), and (25) and presented in Table 2.

Table 2. Calculations for Motor 1 and Motor 2

Parameter	Motor 1	Motor 2
P_R	6 kW	6 kW
Ω_b	1413.7 elec rad/sec	1413.7 elec rad/sec
E_b	46.5 Vrms	46.5 Vrms
I_R	43.0 Arms	43.0 Arms
L	765 μH	1300 μH
L_∞ Eq. (2)	765 μH	765 μH
$L_{\min}$ (for CPSR=6.667) Eq. (25)	658 μH	658 μH
$n_{\min}$ Eq. (18)	2.00 (1800 rpm)	3.89 (3500 rpm)
$I_{\min}$ Eq. (19)	30.41 A	21.80 A
Characteristic Current $I_{CH} = E_b / X_b$ Eq. (20)	43.0 A	25.3 A
$V_{\max}$ Eq. (7)	65.77 Vrms/67.96 Vrms*	91.7 Vrms/93.6 Vrms*
V_{dc} Eq. (4)	146.1 V/150.9 V	203.8 V/207.4 V
$P_{\max}$ Eq. (14)	8.48 kW/8.36 kW**	6.96 kW/6.95 kW**
CPSR (when driven by CPA)	∞	∞

*The second value of $V_{\max}$ corrects for the winding resistance, i.e. $V_{\max}$ is computed as

$$V_{\max} = \sqrt{(E_b + I_R R)^2 + (\Omega_b L I_R)^2} \ . \tag{26}$$

**With winding resistance included,

$$P_{\max} = \frac{3\left[V_{\max} E_b - E_b^2 \cos\left(\tan^{-1}\left(\frac{X_b}{R}\right)\right)\right]}{\sqrt{R^2 + X_b^2}} \ . \tag{27}$$

In the next section the analysis of the PMSM driven by DMIC is discussed.

3. ANALYSIS OF THE PMSM WHEN DRIVEN BY DMIC

The previous section contained a discussion of the PMSM when driven by CPA. The focus in that section was on the relationship between CPSR and motor inductance. Although the DMIC was originally intended for motors with low inductance, it has recently been shown to have the potential for significant loss reduction for PMSMs with large inductance. To make this latter point, an abbreviated treatment of the PMSM is given below that slightly overlaps the previous discussion in Section 2. The mechanism through which the DMIC is able to achieve an infinite CPSR, even though the motor inductance may be small, will be made clear within the discussion.

A recent paper [8] used a fundamental-frequency model to analyze the performance of the sinusoidal back-emf PMSM driven in constant-power mode by DMIC. The inverter includes a common three-phase voltage-source inverter supplemented with an alternating current (ac) voltage controller between the inverter output and the motor. The ac voltage controller consists of three pairs of anti-parallel silicon controlled rectifiers (SCRs) as shown in Fig. 4.

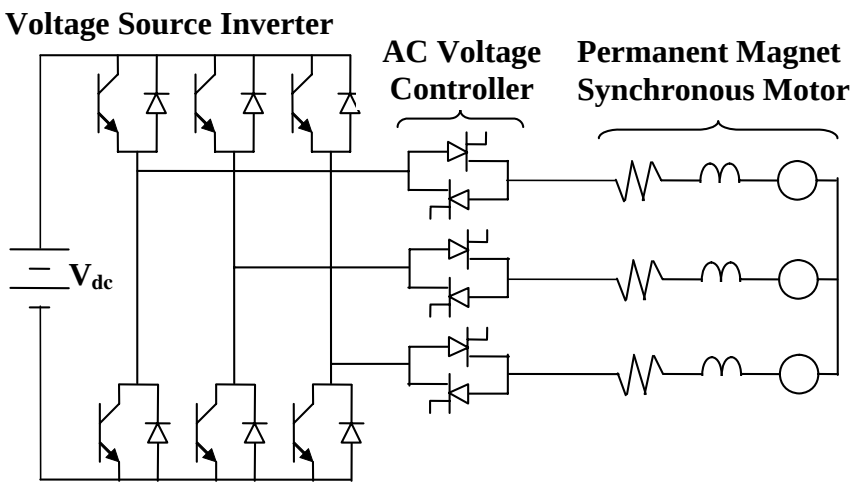


Fig. 4. DMIC inverter topology.

Each SCR pair is a full ac switch. In steady state, the fundamental-frequency components of the voltage across and current through the switch are 90° out of phase reflecting the lossless behavior of the switch and giving rise to an "equivalent reactance" interpretation of the SCRs. On a per phase basis, a fundamental-frequency phasor model has the form shown in Fig. 5 with winding resistance and rotational losses neglected. In the figure, the parameter X_{thy} is the equivalent reactance of an SCR pair.

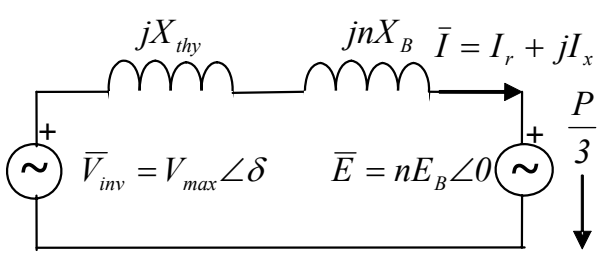


Fig. 5. Per-phase fundamental-frequency phasor model for constant-power mode.

As noted in Ref. [8], the equivalent reactance of the ac switch is not constant but varies with the firing angle of the SCRs. The firing angle of the SCRs also controls the developed power of the motor. Since the equivalent reactance of the switch varies with the developed power, one cannot infer that the equivalent reactance interpretation can be extended to a fixed equivalent inductance that is in series with the motor winding. Note that the total reactance presented to the inverter is the sum of the thyristor reactance and the motor reactance, $X_{thy} + nX_b$. Thus, no matter how small the machine reactance may happen to be, the thyristor reactance can be adjusted, through firing angle control, to make the motor behave as though it were a high-reactance machine. This is why the DMIC achieves an infinite CPSR even when the motor inductance is less, even substantially less than the minimum required to be driven by CPA.

The discussion in this section is based on Ref. [8] and has two main objectives. The first is to show that the SCRs in the DMIC have greater value than simply extending the CPSR. Specifically, it is shown that during constant-power operation they allow the rms motor-current magnitude to be minimized for any given power level. Thus, the DMIC enables "dual modes" of optimal control. Above base speed, the DMIC allows control for maximum watts per rms amp during constant-power operation. Below base speed, the SCRs do not interfere in the inverter-voltage magnitude control for maximum Newton-meters (Nm) per rms amp during constant-torque operation. The second objective is to show that the current minimization capability enabled by the SCRs in the DMIC inverter can result in substantially lower motor current than a common VSI drive employing CPA even when the motor inductance is high. It is shown that the minimum-current magnitude achieved with the DMIC is independent of speed and proportional to developed power. For a high-inductance motor driven by a VSI using CPA, the current magnitude is shown to be speed dependent but virtually independent of developed power level. At high speeds, the reduction in motor-current magnitude is at least 0.7071 with the DMIC relative to the same motor driven by a VSI. Significant reduction in motor current reduces not only copper losses but also losses in the VSI. An economic evaluation of the DMIC must look past the added initial cost and additional losses due to the SCRs and consider the total value of loss reduction in the motor and the inverter over the life of the drive.

The fact that high-machine inductance, or the addition of supplemental series inductance, can increase CPSR is not new as noted in previous works [1,4,5]. Removing the SCRs from Fig. 4 results in CPA. To contrast the performance of CPA and DMIC, we first consider the performance of a high-inductance PMSM driven by CPA in Section 3.1 below. In Section 3.2, we show the current minimization made possible by the DMIC. The performance of CPA and DMIC are summarized in a single graph plotting normalized rms current versus normalized developed power for relative speeds above base speed.

3.1 HIGH-INDUCTANCE PMSM DRIVEN BY CPA

Assuming that the thyristors are removed from the inverter of Fig. 4, the fundamental-frequency model of Fig. 5 has $X_{thy} = 0$ for all operating conditions. The model then represents a PMSM driven by CPA.

The discussion of the CPA driven PMSM in Section 2 focused on the relationship between the motor inductance and CPSR. In this section, it is assumed that the inductance is sufficiently large to meet a wide CPSR requirement and the focus is on the dependence, or lack thereof, of rms motor-current magnitude on speed, developed power, and available dc supply voltage.

From Section 2, when operating above base speed, the rms fundamental-frequency voltage applied by the inverter is

$$V = V_{\max} = \frac{\sqrt{2}V_{dc}}{\pi}. \tag{28}$$

The inverter-lead angle depends on the dc supply voltage and the developed power and is found from Eq. (13) to be

$$\delta = \sin^{-1}\left(\frac{X_b P}{3V_{\max}E_b}\right), \tag{29}$$

and from Eq. (11) the resulting rms motor current at speed, n, is

$$I = \frac{\sqrt{V_{max}^2 - 2nV_{max}E_b \cos\delta + n^2E_b^2}}{nX_b}. \tag{30}$$

Note that at any finite speed, the rms current depends, at least to some degree, on dc supply voltage through its dependence on $V_{\max}$, on the developed power through its dependence on δ, and on motor parameters, E_b and X_b; however, for high speed the rms current approaches the "characteristic current" given by

$$\lim_{n\to\infty} I = \frac{E_b}{X_b} = \frac{E_b}{\Omega_b L}. \tag{31}$$

The characteristic current depends only on motor parameters. When the inductance is sufficiently large, the characteristic current is less than the rated motor current, and this is what enables the CPA driven PMSM to operate with an infinite CPSR. There are, however, two potential drawbacks for wide CPSR drives controlled by CPA.

The first drawback is that, at sufficiently high speed, the rms motor current approaches the characteristic current which is independent of load, P. This means that the motor current is almost the same at no load as it is at full load. Consequently, the CPA drive cannot provide optimum "watts per amp" control at high speed and the efficiency may be poor when the load varies substantially at high speed.

One should expect that, if additional dc supply voltage were provided beyond the minimum necessary to produce rated torque at base speed, the result should be reduced motor current; however, as the speed increases, the motor current approaches the characteristic current which is independent of the dc supply voltage. Thus, the second drawback is that increases in dc supply voltage beyond the minimum required to support base-speed conditions are not effective in enhancing the efficiency of the wide CPSR drive at high speed.

If the motor inductance is the value given in Eq. (21) corresponding to an infinite CPSR, it follows from Eqs. (7), (9), (14), and (13) that

$$
\begin{aligned}
V_{\max} &= E_b\sqrt{2} \\
P_{\max} &= P_R\sqrt{2} \\
\sin\delta &= \frac{P}{P_R\sqrt{2}} \\
\cos\delta &= \sqrt{1-\sin^2\delta}
\end{aligned}
\quad . \tag{32}
$$

Then the rms motor current from Eq. (30) is given by

$$
I = I_R\sqrt{\frac{n^2 - 2n\sqrt{2-\left(\frac{P}{P_R}\right)^2} + 2}{n^2}} \quad . \tag{33}
$$

A plot of per unit rms current, I/I_R, versus per unit developed power, P/P_R, is shown in Fig. 6 for relative speeds of 2, 4, 6, 8, 10, 20, and ∞. The figure shows that when the motor inductance is sufficiently large, $L = L_\infty$ in this case, any developed power up to the rated power can be achieved without exceeding the rms current rating of the motor. Note that even though the inductance is large, the motor-current magnitude increases with speed. The "flatness" of the current versus power curves indicates that the copper losses in the motor are virtually independent of the developed power for the CPA strategy. Efficiency may be poor when high-speed operating conditions require a developed power less than the rated power. A method that can make the rms current proportional to output power can obviously reduce motor copper losses as well as the losses in the VSI inverter. In the next section, it is shown that the DMIC enables motor-current magnitude minimization or, equivalently, optimal watt per rms amp control.

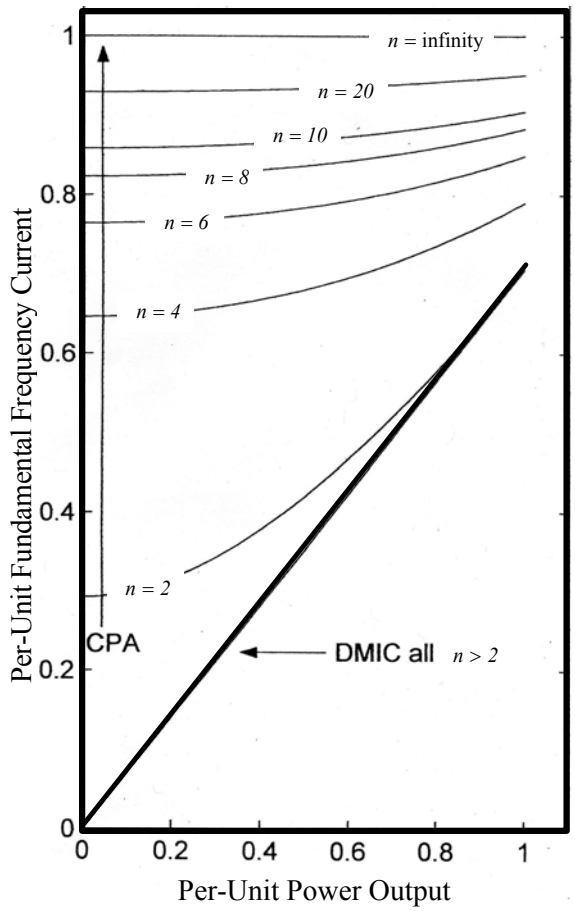


Fig. 6. Constant-power operation of a PMSM motor comparing CPA control with DMIC.

3.2 PMSM CURRENT MAGNITUDE MINIMIZATION WHEN DRIVEN BY DMIC

Given that a PMSM with an inductance as large as that in Eq. (21) can achieve an infinite CPSR when driven by a VSI, is there any benefit to driving the same motor using the DMIC? To address this issue, we use the fundamental-frequency model of Fig. 5. Let the motor-current phasor be written in the rectangular form

$$\begin{aligned} \overline{I} &= I_r + j\, I_x \\ I &= \left|\overline{I}\right| = \sqrt{I_r^2 + I_x^2} \end{aligned} \quad , \tag{34}$$

where

I_r is the torque-producing component of motor current that is in phase with the back-emf, and

I_x is the field-weakening component that is in phase quadrature with the back-emf.

The question is, can the equivalent reactance of the SCRs, X_{thy}, be chosen so that desired power, P, is developed while the magnitude of the motor current, I, is minimized? If so, the DMIC provides optimal

"watts per rms amp" control. This is a distinctly different form of high-speed control than CPA where the high-speed rms current is virtually the same at no load as at full load.

Observe that the value of the in-phase component of motor current results in the developed power

$$\begin{aligned} P &= 3I_r nE_b \\ I_r &= \frac{P}{3nE_b} \end{aligned} . \tag{35}$$

Since I_r is fixed per Eq. (35), the minimization of current magnitude, I, is the same as minimizing the magnitude of the phase quadrature component, I_x. Let

$$X = X_{thy} + nX_b \tag{36}$$

so that

$$\begin{aligned} \overline{I} &= \frac{\overline{V}_{inv} - \overline{E}}{jX} = \frac{V_{\max}}{X}\sin\delta + j\left[\frac{nE_b}{X} - \frac{V_{\max}}{X}\cos\delta\right]. \\ &= I_r + j\, I_x \end{aligned} \tag{37}$$

Recognizing that

$$\begin{aligned} 3\frac{V_{\max} nE_b}{X}\sin\delta &= P \\ \cos\delta &= \sqrt{1 - \left(\frac{XP}{3nE_b V_{\max}}\right)^2} \end{aligned} , \tag{38}$$

we find that the phase quadrature component of motor current becomes

$$I_x = \frac{nE_b - V_{\max}\sqrt{1 - \left(\frac{XP}{3nE_b V_{\max}}\right)^2}}{X} . \tag{39}$$

Differentiating I_x with respect to X, setting the derivative equal to zero, and solving for the current minimizing reactance, X^*, yields

$$X^* = \frac{3V_{\max}\sqrt{n^2E_b^2 - V_{\max}^2}}{P} = X_{thy}^* + nX_b \tag{40}$$

or

$$X_{thy}^{*} = \frac{3V_{\max}\sqrt{n^2E_b^2 - V_{\max}^2}}{P} - nX_b$$

$$= n\left(\frac{3V_{\max}\sqrt{E_b^2 - \frac{V_{\max}^2}{n^2}}}{P} - X_b\right)$$

with, . (41)

$$I_x^{*} = \frac{P}{3V_{\max}}\sqrt{1-\left(\frac{V_{\max}}{nE_b}\right)^2}$$

$$I_r^{*} = \frac{P}{3nE_b}$$

.

Equation (41) for X^{*}_{thy} clearly shows that no fixed inductance can provide the same effect as the thyristors in the DMIC inverter. Specifically, observe that the reactance doesn't vary exactly linearly with speed due to the $V_{\max}^2/n^2$ inside the brackets in the second expression of Eq. (41), and that the reactance is inversely proportional to developed power, P. Thus, a fixed inductance can only achieve the same performance as DMIC at a single speed and power condition.

The anti-parallel SCR pair cannot have a negative reactance, the minimum value of X_{thy} is zero. A value of X_{thy} equal to zero would mean that the thyristors were being fired such that they function as a short circuit. The value of n in Eq. (41) must be sufficiently large such that X_{thy} has a non-negative value. For any given load power, P, the minimum value of n, which occurs when the bracketed term in Eq. (41) is zero, is

$$n_{\min} = \frac{V_{\max}}{E_b\cos\delta} = \frac{V_{\max}}{E_b\cos\left(\sin^{-1}\left(\frac{P}{P_{\max}}\right)\right)}, \tag{42}$$

where $P_{\max}$ is the maximum power-conversion capability of the motor as given by Eq. (14). Notice that the expression for $n_{\min}$ with the DMIC given by Eq. (42) is the same as that single speed at which the CPA driven machine operates at an inverter-power factor of unity and given by Eq. (18). It is shown below that the inverter-power factor with the DMIC is unity for all speeds greater than $n_{\min}$. This contrasts with the CPA drive where the inverter operates at unity-power factor only at the single speed $n_{\min}$. Above speed $n_{\min}$, the inverter-power factor is leading for the CPA drive.

With the optimal value of thyristor reactance, the rms motor current, which is minimum because the inverter-power factor is unity for all speeds above $n_{\min}$, is

$$I^* = \frac{P}{3V_{max}} = \frac{P}{3\sqrt{E_b^2 + \left(X_b I_R\right)^2}} \quad . \tag{43}$$

Note that this minimum current with DMIC is the same as the minimum current with CPA as given by Eq. (19). The difference, however, is that the DMIC drive operates at this minimum-current magnitude for all speeds greater than $n_{\min}$; whereas the current increases above $n_{\min}$ for the CPA drive.

Note that Eq. (43) is independent of speed and directly proportional to developed power. Also note that for any load level, P, an increase in dc supply voltage, which increases $V_{\max}$, will decrease the rms motor current since I varies as $V_{\max}^{-1}$. Thus, high-speed operation with the DMIC can benefit from extra supply voltage through a reduction in motor and inverter losses. This feature of DMIC is distinctly different from CPA where rms motor current at high speed is nearly independent of dc supply voltage. Also, since we have neglected losses, the power supplied by the inverter is the same as the converted power, that is

$$\begin{aligned} P &= 3\,\mathrm{Re}\left(\overline{V}\ \overline{I}^*\right) = 3\,\mathrm{Re}\left(V_{\max}\angle\delta\ I^*\angle\theta\right) \\ &= 3\ V_{\max}\ \frac{P}{3V_{\max}}\cos\left(\delta-\theta\right) \\ &= P\cos\left(\delta-\theta\right) \\ &\Rightarrow \cos\left(\delta-\theta\right) = 1 \Rightarrow \delta = \theta \end{aligned} \quad . \tag{44}$$

Thus, the motor-current phasor is in phase with the inverter-voltage phasor, such that the inverter operates at unity-power factor.

Equation (43) applies whether the inductance is large or small. In cases where the motor is to provide substantial regenerative braking for the vehicle, Eq. (14) shows that the inductance will necessarily need to be small such that $P_{\max}$ is substantially larger than the rated power, P_R. In such cases, the CPA method would not yield adequate CPSR and DMIC would be essential. In this discussion, we will show that DMIC has substantial potential benefit even when the motor inductance is large.

Letting the motor inductance be L_∞ from Eq. (21) and using the corresponding $V_{\max}$ from Eq. (32), the optimal rms fundamental-frequency motor-current magnitude is

$$I^* = \frac{P}{\sqrt{2}\ P_R} I_R \,. \tag{45}$$

Note that Eq. (45) does not depend on speed. However, for the case under discussion, Eq. (42) requires that the relative speed be greater than or equal to two in order for Eq. (45) to be valid. A plot of per-unit motor current, I^* / I_R, versus per-unit developed power, P / P_R, is shown in Fig. 6 where the single curve shown is valid for any speed at and above $n = 2$. For convenience, the same set of axes was used to display the current versus power data for the same inductance level when the motor is driven by CPA.

Although a motor with inductance, L_∞, is considered well-suited for high CPSR applications with CPA, the curves in Fig. 6 show that for relative speeds of two or greater, the motor current is always less for the same motor driven by DMIC and for most operating conditions the current is substantially less with DMIC. Reductions in motor current will result in reduced motor copper losses, which vary with the square of rms current and reduce the losses in the inverter components that vary with the first power of the rms motor current. For example, at high speed and rated power, the rms motor current with the DMIC is 0.7071 that of the CPA driven motor. The motor losses are reduced by a factor of 50% while the inverter losses are decreased by 29.3%. At high speed and 70% of full power, the rms current with the DMIC is 49.5% that of the VSI driven motor. The motor copper losses are reduced by 75.5% while the inverter losses are reduced by 50.5%. Depending on the application, particularly the speed/load profile, these loss reductions may more than compensate for the losses introduced by the addition of the SCRs and the value of the energy recovery over the life of the drive may more than offset the initial first cost of the SCRs.

When driven by DMIC, the CPSR performance envelopes of Motor 1 and Motor 2 are shown in Fig. 7 with winding resistance, rotational losses, and inverter losses neglected. The figure can be compared with Fig. 3, which is the analogous plot for the two motors when driven by CPA. Note that the DMIC drives operate at the minimum-current magnitude for all speeds greater than $n_{\min}$.

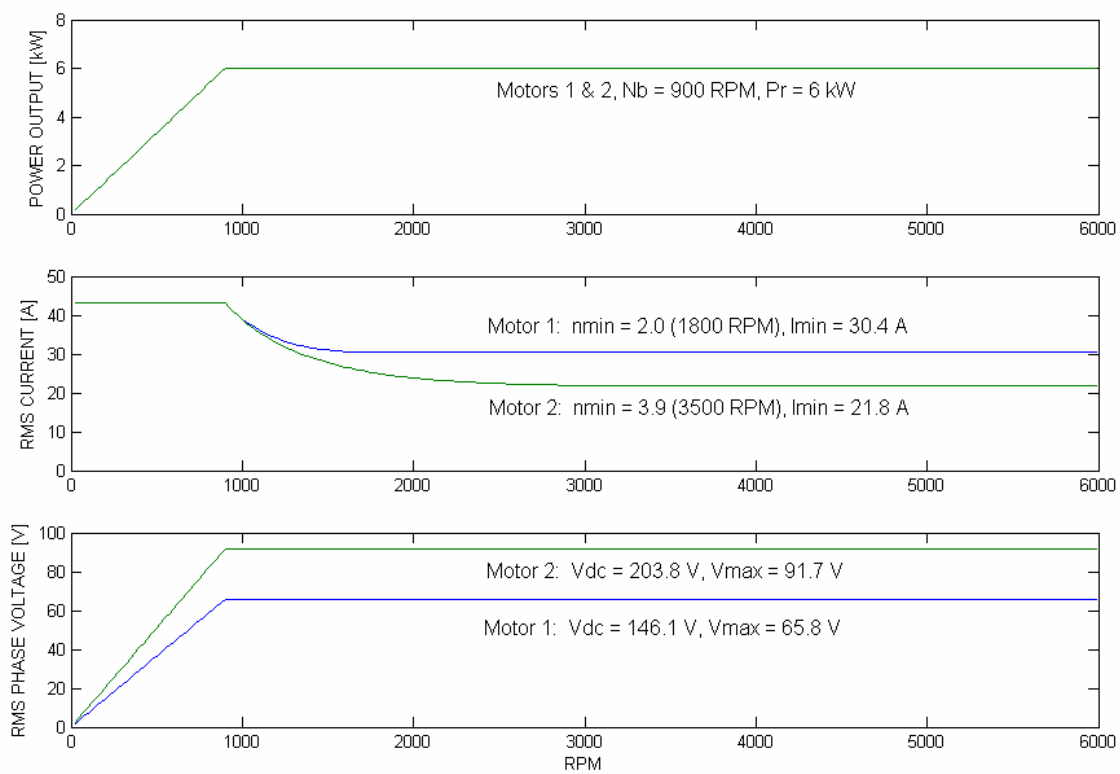


Fig. 7. Constant-power performance of the PMSM driven by DMIC.

The Motor 1 and Motor 2 designs are examined in the next section with respect to the current-magnitude control properties at high speed and variable load with CPA and DMIC.

3.3 COMPARISON OF MOTOR-CURRENT MAGNITUDE WITH CPA AND DMIC AT HIGH SPEED AND VARIABLE LOAD

The example motors of Table 1 differ only in their inductance. Neglecting winding resistance, the 765 μH machine (Motor 1) requires a dc supply of 146.1 V to operate at rated torque at base speed while remaining within the 43 A rated current. Motor 2, with 1300 μH inductance, requires a supply of 203.8 V_{dc} to achieve rated torque at base speed and rated current. The discussion in the previous sections suggested that increased dc supply voltage could improve efficiency of a CPA or DMIC driven motor by reducing the motor current, with the greatest benefit observed with the DMIC. To demonstrate this fact, the rms fundamental-frequency motor current versus useful output power for Motor 1 is displayed in Fig. 8 for supply voltages of 146.1 V and 203.8 V. All loss mechanisms were neglected in constructing the figure. For each supply voltage, current versus power output is plotted for several different speeds. For the 146.1 V case, a single plot suffices to characterize the DMIC for all speeds larger than a relative speed of 2; i.e. 1800 rpm or greater. For the CPA drive at 146.1 V, curves are drawn for 1800, 2510, 3600, 6000 rpm, and infinite speed. For the infinite-speed case, the rms current is the characteristic current of 43 A independent of the supply voltage. For Motor 1, 43 A is also the rated current. Note that as the rpm increases from 1800 rpm towards 6000 rpm, the motor current increases and becomes insensitive to power level. For the second set of curves drawn for the 203.8 V supply, the magnitude of the current for a given speed is reduced from the same speed for the lower supply voltage level. This is seen for both the DMIC and for CPA. However, the current-magnitude reduction is greatest with the DMIC. For the DMIC case, a single curve again captures the behavior at all speeds greater than twice the "true base speed." With the supply voltage raised from the minimum level of 146.1–203.8 V, the base speed increases, per Eq. (5), from 900–1255 rpm (203.8 x 900/146 V). The single curve drawn for the DMIC applies to all speeds twice this value at and above 2510 rpm. The figure clearly shows that providing additional dc supply voltage beyond the minimum needed to support base-speed condition is beneficial in reducing motor current and, therefore, reducing motor copper losses. In the inverter, there may be some increase in switching and reverse-recovery losses due to the additional supply voltage, but there will be reductions in conduction losses that are at least proportional to the reduction in current if not more. Since the conduction losses are typically the main inverter-loss mechanism, the inverter losses will also decline with higher supply voltage.

Figure 9 shows the high-speed current-magnitude control capability of CPA and DMIC for Motor 1 and Motor 2 when both machines operate from a 203.8 Vdc supply. The plot for Motor 1 in Fig. 7 is identical to the plot for 203.8 V_{dc} shown in Fig. 9; however, Fig. 9 shows the added benefit of having an inductance that is greater than the "optimal" value of L_∞. Recall that the inductance of Motor 1 is exactly L_∞, 765 μH, while Motor 2 has significantly more inductance (1300 μH). When comparing the two figures observe that when the motor is driven by CPA, the higher inductance results in a lower current magnitude at any given speed and power level thereby improving efficiency. Also note that for the high-inductance machine that the curves for the various speeds shown; 1800, 3600, and 6000 rpm are much closer to the performance of the DMIC driven motor which has a single curve describing all operating speeds greater than 1800 rpm. While the performance with CPA is closer to the DMIC for a high-inductance machine, the current with the DMIC drive is always at least as low as with the CPA, such that the DMIC should have an efficiency advantage especially at high speed and less than full load. Although not shown here, a further increase in dc supply voltage, say from 203.8–250 V, would further reduce the motor current with DMIC, but has a very modest impact on the CPA drive. Figure 9 clearly indicates that it may be very advantageous to have an inductance greater than L_∞. Thus, it is difficult to accept L_∞ as an "optimum" design target for traction drives.

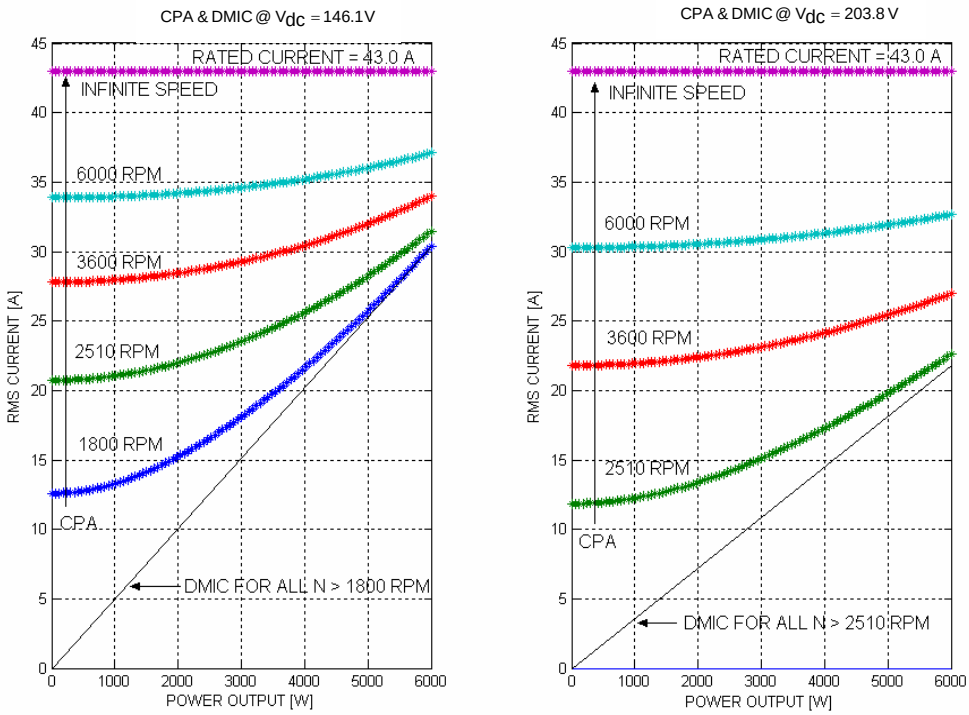


Fig. 8. RMS motor current vs. power output during high-speed operation of Motor 1 with 146.1 V and 203.8 Vdc supply voltages when driven by CPA or by DMIC.

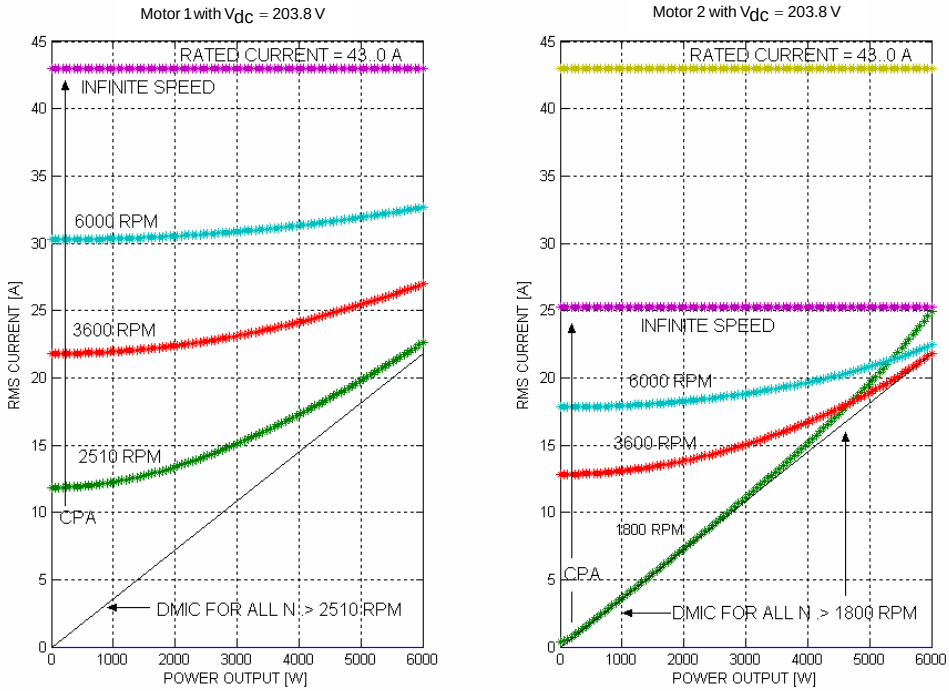


Fig. 9. RMS motor current vs. power output during high-speed operation of Motor 1 and Motor 2 with 203.8 Vdc supply.

The results in this section highlight the key difference between CPA and DMIC with respect to motor-current-magnitude control during high-speed operation. At high speed, the rms motor current for the two different PMSM motor control methods approach

$$\begin{aligned} I_{CPA} &= \frac{E_b}{X_b} = \frac{E_b}{\Omega_b L} \\ I_{DMIC} &= \frac{P}{3V_{\max}} = \frac{\pi P}{3\sqrt{2}V_{dc}} \end{aligned} . \tag{46}$$

The motor current at high speed with CPA is the characteristic current which depends only on motor parameters. This has both positive and negative implications. On the positive side, if the motor inductance is sufficiently large, then the characteristic current is less than the rated current thereby enabling operation in a wide CPSR. On the negative side, two points can be made. First, the characteristic current is independent of load, meaning that the efficiency can be poor under light load and variable load conditions at high speed. Second, since the characteristic current is independent of dc supply voltage, providing a dc supply voltage beyond what is necessary to support rated torque at base speed cannot reduce the motor current at high speed. The motor current at high speed with DMIC is proportional to load power such that good efficiency can be maintained under light load and variable load conditions. Also, the high-speed current is independent of machine inductance. Whether the inductance is large or small, the high-speed current will be the same. The difference in behavior between a large or small motor inductance will lie in the firing of the thyristors, which will always adjust the total inductance to minimize the rms amps per developed watt. Finally, with the DMIC the high-speed current is inversely proportional to supply voltage. Therefore, significant reduction in motor-current magnitude and attendant reductions in motor and inverter losses can be achieved by providing more supply voltage than is required to support the specified base-speed conditions.

3.4 STEADY-STATE CONTROL INCLUDING WINDING RESISTANCE AND ROTATIONAL LOSSES

The analysis given above neglected winding resistance and rotational losses. Neglecting these factors made the analysis simpler and led to compact expressions which provide considerable insight into the control of the PMSM traction drive in the constant-torque and constant-power modes. However, the control objective is to develop the required motor torque/power while minimizing the losses using sinusoidal PWM. In PWM control, there are two variables; the amplitude-modulation index, m_a, which has been defined as the ratio of the applied fundamental-frequency phase voltage, and the inverter-lead angle, δ, which will be used with the PWM reference signals. In this section, expressions are given for m_a and δ for the PMSM traction drive that include winding resistance and rotational losses. The availability of these expressions will be useful in analyzing the performance of the dynamic PWM controller developed during future work. The CPA drive is addressed in Section 3.4.1 while the corresponding results for the DMIC drive are given in Section 3.4.2.

3.4.1 Amplitude-Modulation Index and Inverter-Lead Angle for CPA

During low-speed operation in the constant-torque mode, both the amplitude-modulation index and the inverter-lead angle can be adjusted. This allows the motor current to be placed in phase with the motor emf. Since all of the motor current produces torque, the rotor copper losses are minimized by this maximum torque per amp control. The required torque is

$$I_r = \frac{T}{3K_t} = \frac{T_{out} + T_{rot}(n)}{3K_t} \tag{47}$$

where T_{out} is the useful output torque and T_{rot} is the torque required to supply rotational losses. Using the equivalent circuit of Fig. 2 with $X = n\,X_b$, the applied fundamental-frequency voltage required to drive this current into the motor is

$$\begin{aligned} V\angle\delta &= nE_b + I_r\left(R + jnX_b\right) \\ &= \sqrt{\left(nE_b + RI_r\right)^2 + \left(nX_bI_r\right)^2}\angle\tan^{-1}\left(\frac{nX_bI_r}{nE_b + RI_r}\right). \end{aligned} \tag{48}$$

The necessary amplitude-modulation index is

$$m_a = \frac{V}{\frac{V_{dc}}{2\sqrt{2}}} = \frac{2\sqrt{2}\sqrt{\left(nE_b + RI_r\right)^2 + \left(nX_bI_r\right)^2}}{V_{dc}}, \tag{49}$$

while the lead angle is given by

$$\delta = \tan^{-1}\left(\frac{nX_bI_r}{nE_b + RI_r}\right). \tag{50}$$

Note that the amplitude-modulation index and the lead angle depend on speed and on load. Assuming full overmodulation, the constant-torque control region ends at the "true base speed" n_{bt} which causes the amplitude-modulation index to be equal to $\frac{4}{\pi}$; i.e., the true base speed is the solution of

$$\frac{4}{\pi} = \frac{2\sqrt{2}\sqrt{\left(n_{bt}E_b + RI_r\right)^2 + \left(n_{bt}X_bI_r\right)^2}}{V_{dc}} \tag{51}$$

which has solution

$$n_{bt} = \frac{\sqrt{\frac{2V_{dc}^2}{\pi^2}\left(E_b^2 + X_b^2I_r^2\right) - R^2X_b^2I_r^4} - E_bRI_r}{\left(E_b^2 + X_b^2I_r^2\right)}. \tag{52}$$

Above the true base speed is the constant-power mode. The torque-producing component of current required to sustain speed and load is given by

$$I_r = \frac{P}{3nE_b} = \frac{P_{out} + P_{rot}(n)}{3nE_b} \tag{53}$$

where P is the total required power, P_{out} is the useful output power, and P_{rot} is the power supplied to rotational losses. Since the applied voltage is maximum in this mode

$$m_a = \frac{4}{\pi}, \tag{54}$$

while the appropriate inverter-lead angle is

$$\delta = \theta_z - \cos^{-1}\left(\frac{\frac{ZP}{3} + (nE_b)^2 \cos\theta_z}{nE_b V_{\max}}\right), \tag{55}$$

where,

$$\begin{aligned} V_{\max} &= \frac{\sqrt{2}V_{dc}}{\pi} \\ Z &= \sqrt{R^2 + (nX_b)^2} \\ \theta_z &= \tan^{-1}\left(\frac{nX_b}{R}\right) \end{aligned} \tag{56}$$

The lead angle of Eq. (55) assures that the required power is developed but does not guarantee that the rms motor-current magnitude is within rating unless the inductance is L_∞ or greater.

3.4.2 Amplitude-Modulation Index and Inverter-Lead Angle for DMIC

Operation of the DMIC is identical to that of CPA through the speed, $n_{\min}$, at which the CPA drive achieves unity-power factor. Thus, in the constant-torque mode we have

$$\begin{aligned} m_a &= \frac{2\sqrt{2}\sqrt{(nE_b + RI_r)^2 + (nX_b I_r)^2}}{V_{dc}} \\ \delta &= \tan^{-1}\left(\frac{nX_b I_r}{nE_b + RI_r}\right) \\ 0 \le n \le n_{bt} &= \frac{\sqrt{\frac{2V_{dc}^2}{\pi^2}\left(E_b^2 + X_b^2 I_r^2\right) - R^2 X_b^2 I_r^4} - E_b R I_r}{\left(E_b^2 + X_b^2 I_r^2\right)} \end{aligned} \tag{57}$$

The constant-power region is divided into two zones. The first is between the true base speed and the speed, $n_{\min}$, at which the CPA drive reaches unity inverter-power factor. When resistance is included, this speed can be calculated as

$$n_{\min} = \frac{P}{3I\sqrt{E_b^2 - I^2 X_b^2}}, \tag{58}$$

where P is the total power converted which is the sum of the useful output power, P_{out}, and the rotational power losses P_{rot} and I is the minimum-current magnitude given by

$$I = \frac{V_{\max} - \sqrt{V_{\max}^2 - 4R\frac{P}{3}}}{2R}. \tag{59}$$

The amplitude modulation and inverter-lead angles are

$$\begin{aligned} m_a &= \frac{4}{\pi} \\ \delta &= \theta_z - \cos^{-1}\left(\frac{\frac{ZP}{3} + \left(nE_b\right)^2 \cos\theta_z}{nE_b V_{\max}}\right) \\ n_{bt} &\le n \le n_{\min} \end{aligned} \tag{60}$$

where Z and θ_z are from Eq. (56). During the above constant-power zone, the thyristors are operated as a short circuit, i.e. X_{thy} is zero.

In the second constant-power region, which is above $n_{\min}$, the amplitude-modulation index and lead angle are found from

$$
\begin{aligned}
m_a &= \frac{4}{\pi} \\
I &= \frac{V_{\max} - \sqrt{V_{\max}^2 - 4R\frac{P}{3}}}{2R} \\
I_r &= \frac{P}{3nE_b} \\
I_x &= \sqrt{I^2 - I_r^2} \\
\delta &= \tan^{-1}\left(\frac{I_x}{I_r}\right) \\
n_{\min} &\le n < \infty
\end{aligned}
\tag{61}
$$

If desired, the equivalent reactance of the thyristors can be computed as

$$
X_{thy} = n\left(\frac{I_x E_b}{I^2} - X_b\right) \tag{62}
$$

The expressions for m_a and δ in this section for both CPA and DMIC, were derived based on an algebraic fundamental-frequency phasor model. The expressions have been found to be very accurate when used in detailed time-domain simulation that includes PWM switching. The analysis thus far incorporates winding resistance and rotational losses but neglects losses in the inverter. Inverter losses are an important factor in overall drive efficiency. The next section discusses the calculation of inverter losses based on the use of the fundamental-frequency phasor model.

4. INVERTER LOSSES

Losses in inverter components include

- Blocking losses,
- Conduction losses,
- Switching losses (transistors), and
- Reverse-recovery losses (diodes and thyristors)

Blocking losses are very small relative to the other inverter-loss mechanisms and are neglected in this work. The remaining loss mechanisms are important and must have a proper accounting. The method used to model and calculate the various inverter loss types are discussed individually below.

4.1 CONDUCTION LOSSES

Figure 10 shows "equivalents" of a transistor and bypass diode and thyristor that can be useful in determining the conduction losses.

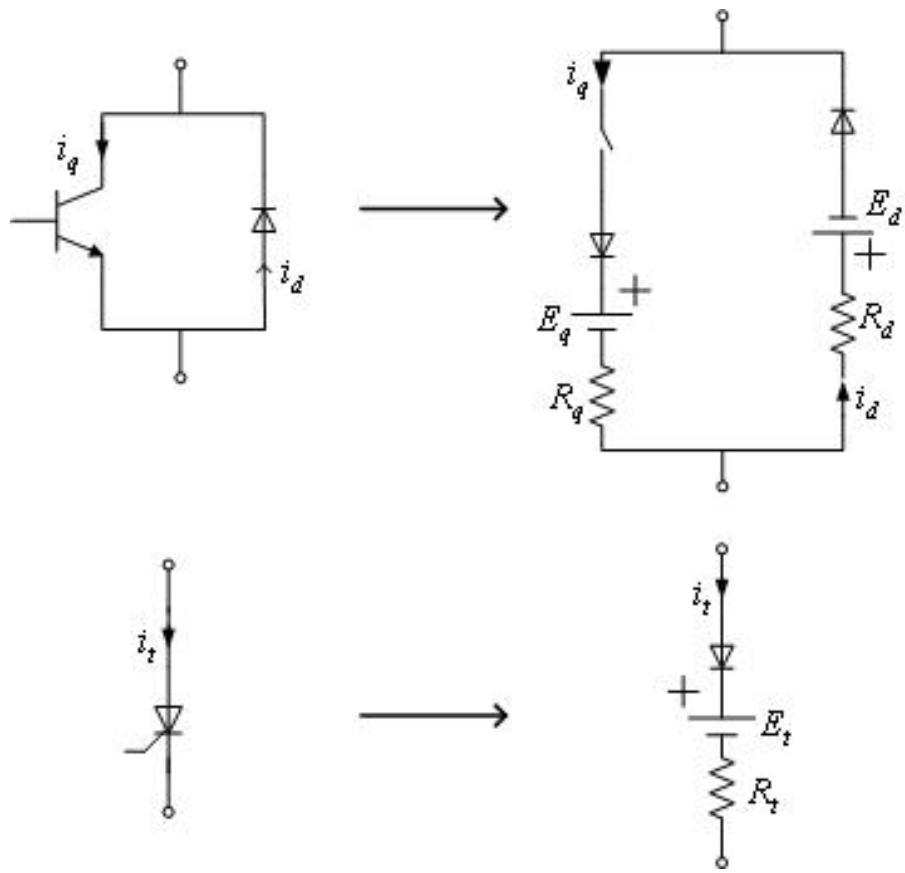


Fig. 10. Transistor with bypass diode and thyristor equivalents for determining conduction losses.

The notations used in the figure are as follows:

$R_q =$ transistor resistance

$E_q =$ transistor forward voltage drop

$R_d =$ diode resistance

$E_d =$ diode forward voltage drop

$R_t =$ thyristor resistance

$E_t =$ thyristor forward voltage drop

The conduction losses of the transistor, diode, and thyristor are computed as

$$\begin{aligned} P_{q-c} &= \text{transistor conduction losses} \\ &= I_{q-avg}E_q + I_{q-rms}^2 R_q \\ P_{d-c} &= \text{diode conduction losses} \\ &= I_{d-avg}E_d + I_{d-rms}^2 R_d \\ P_{t-c} &= \text{thyristor conduction losses} \\ &= I_{t-avg}E_t + I_{t-rms}^2 R_t \end{aligned} \tag{63}$$

where

$I_{q-avg} =$ average transistor current

$I_{q-rms} =$ rms transistor current

$I_{d-avg} =$ average diode current

$I_{d-rms} =$ rms diode current

$I_{t-avg} =$ average thyristor current

$I_{t-rms} =$ rms thyristor current

The device parameters ($E_q, R_q, E_d, R_d, E_t,\ R_t$) are generally contained on device-data sheets or can be derived from device data. These parameters may be given in ranges of minimum, typical, and maximum and may be temperature/voltage sensitive. Thermal modeling is not incorporated in this work and all parameters will be determined at a single device temperature such as 125°C. Voltage effects will be incorporated whenever possible and generally involve scaling parameters up or down based on dc supply voltage. The critical values needed to calculate the conduction losses are the average and rms currents through the transistors, diodes, and thyristors. Since PWM action is involved during low-speed motor operation, these currents are difficult to evaluate accurately without using time-domain simulation of a detailed inverter model. While such a detailed simulation model is available, the engineering time to calculate inverter losses using such an approach would be prohibitive. An alternative approach uses the simplified fundamental-frequency models applied in Sections 2 and 3 to estimate the device currents needed to calculate conduction losses. These losses are then combined with switching and reverse-recovery loss calculations, which will be described subsequently.

Approximate values of the device average and rms currents can be obtained using the per-phase fundamental-frequency model shown in Fig. 11. The model applies for both CPA and DMIC but, X_{thy} is zero for all operating conditions when using CPA.

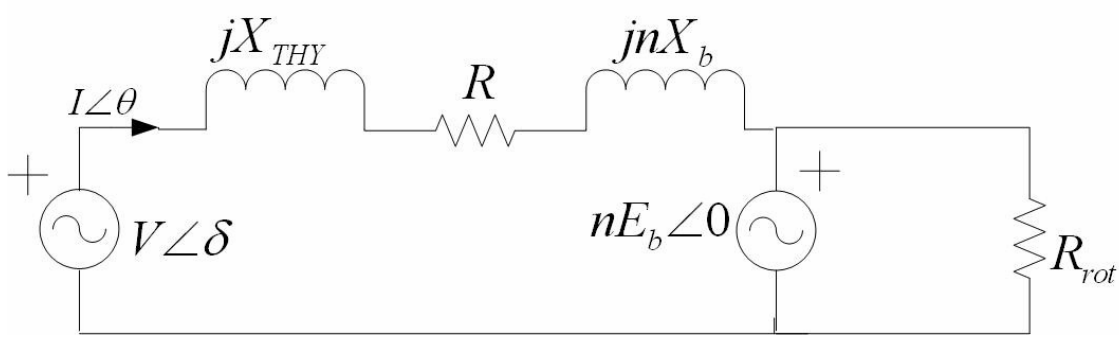


Fig. 11. Per-phase model used to calculate average and rms device currents.

The model of Fig. 11 explicitly represents motor copper and rotational losses since

$$P_{cu} = 3I^2R$$
$$P_{rot} = 3\frac{\left(nE_b\right)^2}{R_{rot}} \quad . \tag{64}$$

In this study, the winding resistance is fixed for both the example motor designs. No correction is attempted for temperature or skin effect. Similarly the speed sensitive losses are fixed functions of speed, as shown in Table 1, and are not corrected for operating conditions such as current level or temperature. Inverter losses are not explicitly represented in the model of Fig. 11. The average and rms device currents required to compute conduction losses will be determined based on the rms motor current, I, and on the phase relationship between motor-current phasor, $\overline{I}$, and the inverter voltage and back-emf phasors, $\overline{V}$ and $\overline{E}$, respectively.

If the current and back-emf phasors are known, then combined with knowledge of the machine impedance at the given speed

$$\overline{V} = \overline{E} + \overline{I}\left(R + jX\right) \quad . \tag{65}$$

Let the motor back-emf be the phasor reference and let

$$\begin{aligned} m_a &= \text{ amplitude modulation index} \\ &= \frac{2\sqrt{2}V}{V_{dc}} \quad . \\ \delta &= \text{ inverter lead angle} \\ \theta &= \text{ angle of motor current phasor} \end{aligned} \tag{66}$$

Due to the fact that the voltage-phasor magnitude, V , is limited by the dc supply voltage, the amplitude-modulation index lies in the range

$$0 \le m_a \le \frac{4}{\pi} \quad , \tag{67}$$

where 4/π is the first term in the fundamental Fourier expansion of a square wave.

Approximate values of the average and rms device currents for a CPA drive can be calculated as

$$\begin{aligned} I_{q-avg} &= \sqrt{2} I \left(\frac{1}{2\pi} + \frac{m_a \cos(\delta - \theta)}{8} \right) \\ I_{d-avg} &= \sqrt{2} I \left(\frac{1}{2\pi} - \frac{m_a \cos(\delta - \theta)}{8} \right) \\ I_{q-rms} &= \sqrt{2} I \sqrt{\frac{1}{8} + \frac{m_a \cos(\delta - \theta)}{3\pi}} \\ I_{d-rms} &= \sqrt{2} I \sqrt{\frac{1}{8} - \frac{m_a \cos(\delta - \theta)}{3\pi}} \end{aligned} , \tag{68}$$

while the approximate values for a DMIC drive can be calculated from

For $n < n_{\min} = \dfrac{V_{\max}}{E_b \cos\delta} = \dfrac{V_{\max}}{E_b \cos\left(\sin^{-1}\left(\dfrac{P}{P_{\max}}\right)\right)}$

$$
\begin{aligned}
I_{q-avg} &= \sqrt{2}I\left(\frac{1}{2\pi} + \frac{m_a \cos(\delta-\theta)}{8}\right) \\
I_{d-avg} &= \sqrt{2}I\left(\frac{1}{2\pi} - \frac{m_a \cos(\delta-\theta)}{8}\right) \\
I_{t-avg} &= \frac{\sqrt{2}I}{\pi} \\
I_{q-rms} &= \sqrt{2}I\sqrt{\frac{1}{8} + \frac{m_a \cos(\delta-\theta)}{3\pi}} \\
I_{d-rms} &= \sqrt{2}I\sqrt{\frac{1}{8} - \frac{m_a \cos(\delta-\theta)}{3\pi}} \\
I_{t-rms} &= \frac{I}{\sqrt{2}}
\end{aligned}
$$

For $n > n_{\min}$

$$
\begin{aligned}
I_{q-avg} &= \frac{\sqrt{2}I}{\pi} \\
I_{d-avg} &= 0. \\
I_{t-avg} &= \frac{\sqrt{2}I}{\pi} \\
I_{q-rms} &= \frac{I}{\sqrt{2}} \\
I_{d-rms} &= 0 \\
I_{t-rms} &= \frac{I}{\sqrt{2}}
\end{aligned}
\quad . \tag{69}
$$

These equations are adapted from the work described in Refs. [10] and [11]. The formulas apply for speed conditions above and below base speed. Above base speed, the motor terminal voltage V is at the maximum value and the amplitude-modulation index is at its upper limit ($4/\pi$). The expressions rely on the motor and inverter-component currents being dominated by their fundamental-frequency components; which means that the effects of harmonic currents introduced by PWM and/or by six-step switching are neglected.

To assess the accuracy of the above formulas, two load conditions (one below and one above base speed) are investigated using a detailed time-domain switching model to calculate average and rms device currents, which are then compared with the approximate values given above. The Motor 2 design is used for the demonstration.

The first operating condition is 60% of base speed, n = 0.6 or 540 rpm, and 60% of rated torque (38.2 Nm). The dc supply voltage is assumed to be 207.4 V. Rotational losses are neglected. In this case, the rms motor current is 60% of its rated value

$$I = 0.6 I_R = 25.8 \text{ A} . \tag{70}$$

The motor current is in phase with the back-emf in order to maximize the torque per amp so that $\theta = 0$. The applied fundamental-frequency phase voltage necessary to support this condition given by Eq. (48) is

$$V\angle\delta = nE_b + I\left(R + jnX_b\right) = 41.1557\angle 43.7443^o . \tag{71}$$

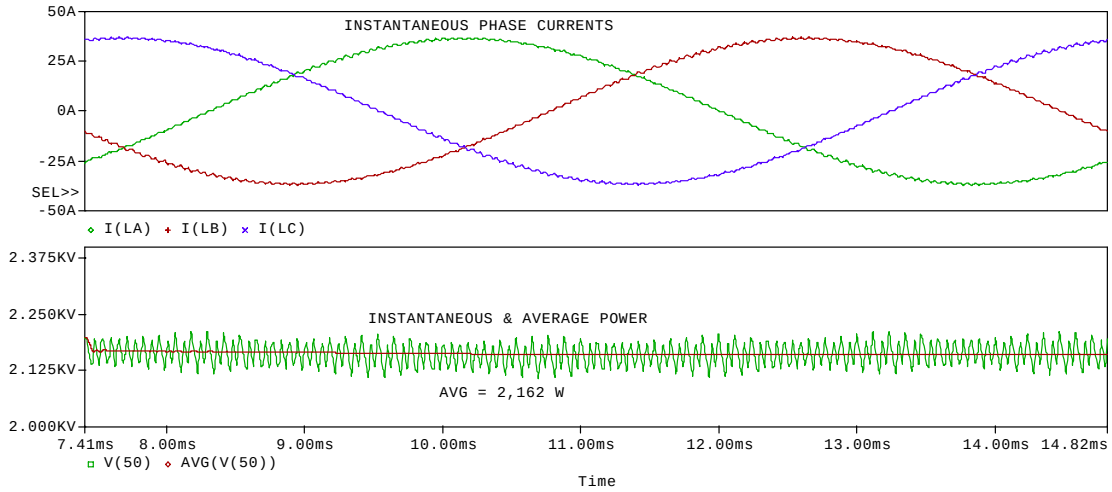
This result applies for both CPA and DMIC since the thyristors, which are fired so that $X_{thy} = 0$, do not participate in the PWM control at low speed. Thus,

$$\begin{aligned} m_a &= \frac{2\sqrt{2}41.1557}{207.4} = 0.5617 \\ \delta &= 43.7443^o \\ \theta &= 0^o \end{aligned} . \tag{72}$$

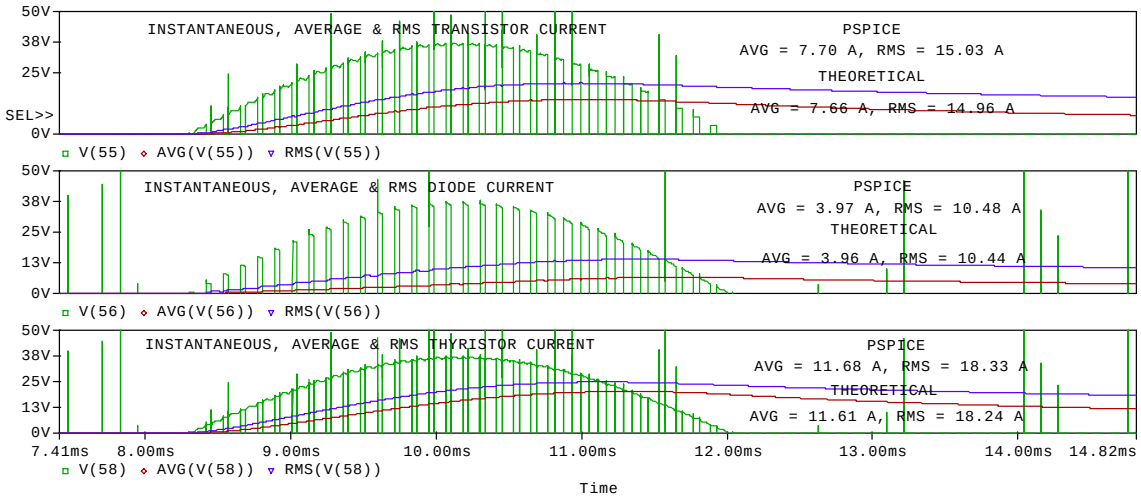
Applying the device-current formulas, Eqs. (51) and (52)

$$\begin{aligned} I_{q-avg} &= 7.66 \text{ A} \\ I_{q-rms} &= 14.96 \text{ A} \\ I_{d-avg} &= 3.96 \text{ A} \\ I_{d-rms} &= 10.44 \text{ A} \\ I_{t-avg} &= 11.61 \text{ A} \\ I_{t-rms} &= 18.24 \text{ A} \end{aligned} . \tag{73}$$

A detailed PSPICE time-domain simulator, which represents inverter components as ideal switches but includes PWM switching operations, was used to calculate the same values of current. Instantaneous and rms motor current and instantaneous, average, and rms values of transistor, bypass diode, and thyristor currents are shown in Fig. 12 for a PWM carrier frequency of 8505 Hz (frequency modulation index of 63). Figure 13 is the detailed simulation results for a carrier frequency of 2025 Hz (frequency modulation index of 16). The simulated quantities and theoretical values are compared in Table 3.

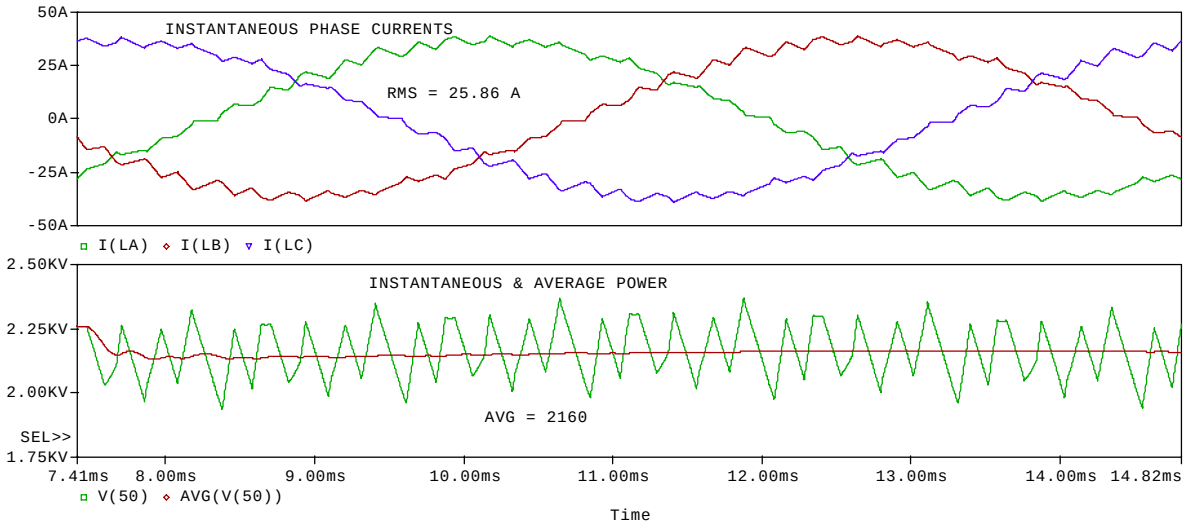


a. Motor currents and power.

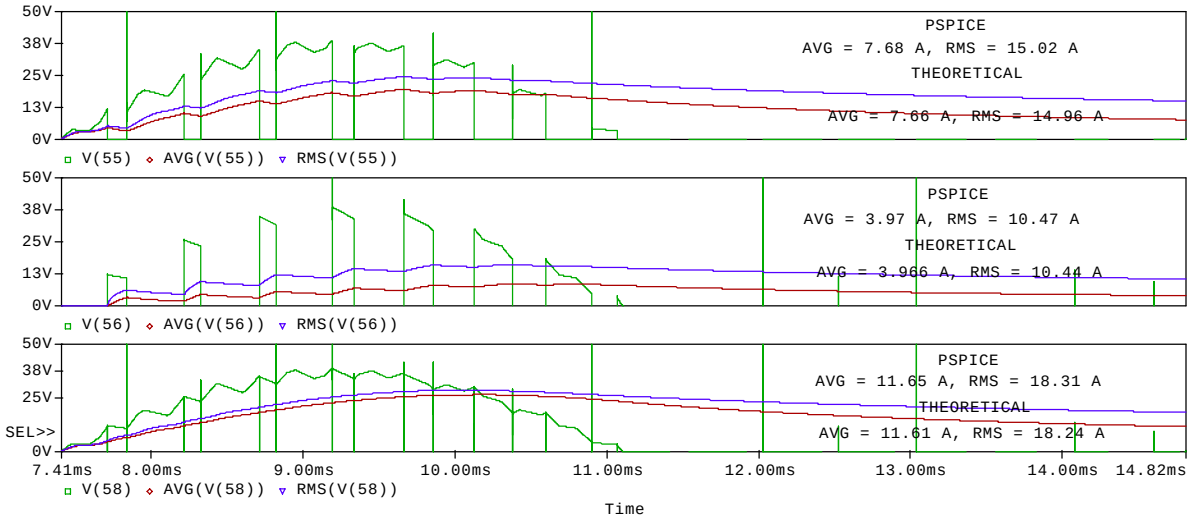


b.Transistor, bypass diode, and thyristor currents.

Fig. 12. Time-domain simulation of Motor 2 at 540 rpm and 60% rated torque with 207.4 Vdc supply, and a carrier frequency of 8505 Hz.



a. Motor currents and power.



b. Transistor, bypass diode, and thyristor currents.

Fig. 13. Time-domain simulation of Motor 2 at 540 rpm, 60% rated torque with 207.4 Vdc supply, and a carrier frequency of 2025 Hz.

Table 3. Comparison of theoretical and simulated Motor 2 and inverter-current magnitudes at 540 rpm, 60% rated torque, and dc supply of 207.4 V.

	Theoretical	fc = 8505 Hz	fc = 2025 Hz
Parameter			
P_{out}	2160 W	2162 W	2160 W
I (rms motor current)	25.8 A	25.8 A	25.9 A
I_{q-avg}	7.66 A	7.70 A	7.68 A
I_{q-rms}	14.96 A	15.03 A	15.02 A
I_{d-avg}	3.96 A	3.97 A	3.97 A
I_{d-rms}	10.44 A	10.48 A	10.47 A
I_{t-avg}	11.61 A	11.68 A	11.65 A
I_{t-rms}	18.24 A	18.33 A	18.31 A

The results in Table 3 show that the simplified fundamental-frequency model predicts average and rms inverter-component currents with accuracy within 1% of simulated values for this low-speed operating point. The table also shows that switching frequency has only a minor effect on the device-current magnitudes computed with the detailed time-domain simulator. The time-domain simulator involves numerical simulation and small differences resulting from computational precision are to be expected. The results indicate that the fundamental-frequency model predicts average and rms inverter-component currents during low-speed operation with sufficient accuracy to have confidence in the results obtained with this simplified model.

As a final test of the simplified model, the Motor 2 design was examined at a high-speed operating condition; 3000 rpm (n = 3.333) and 25% of rated power (1500 W). Since the CPA and DMIC differ in their performance for this operating condition, both drive options were considered.

Figure 14 shows the simplified per-phase fundamental-frequency model solved for this operating condition for the CPA drive method including rotational losses. In constructing the phasor solutions, the analyses in Sections 2 and 3 were suitably modified to include the effects of copper and rotational losses. Note that the motor efficiency calculated based on Fig. 14 is 93.7%. While not shown here, the efficiency of Motor 1, which has the "optimal" inductance, at the same operating condition and using the same dc supply voltage is only 91.3%.

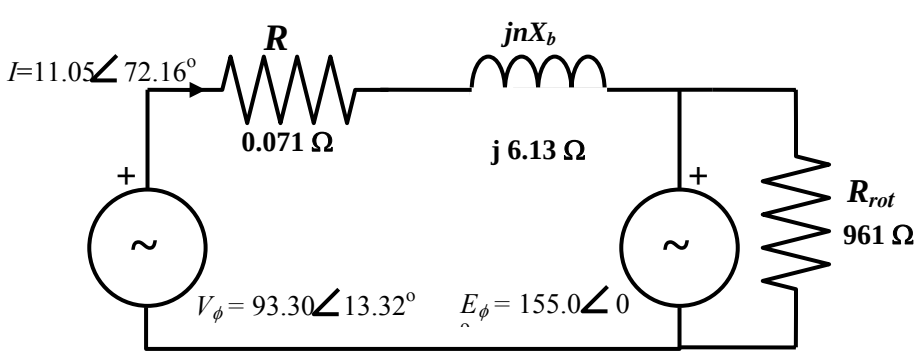


Fig. 14. Per-phase fundamental-frequency model of the Motor 1 design driven by CPA at 3000 rpm and 1500 W useful output power with rotational losses included.

From Fig. 14 we find that

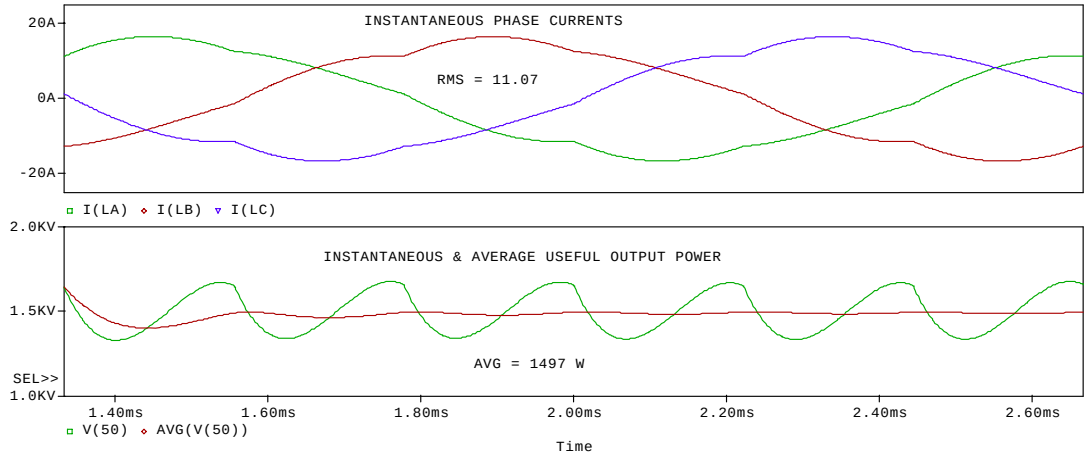
$$\begin{aligned} m_a &= \frac{4}{\pi} \\ I &= 11.05 \text{ A} \\ \delta &= 13.32^{\circ} \\ \theta &= 72.16^{o} \end{aligned} \quad . \tag{74}$$

This load condition was simulated using the detailed time-domain CPA simulator. Simulation results showing phase currents, developed power, and average and rms transistor and bypass diode currents are given in Fig. 15. The device-current magnitudes computed with the fundamental-frequency model formulas are compared below with the values from the simulation

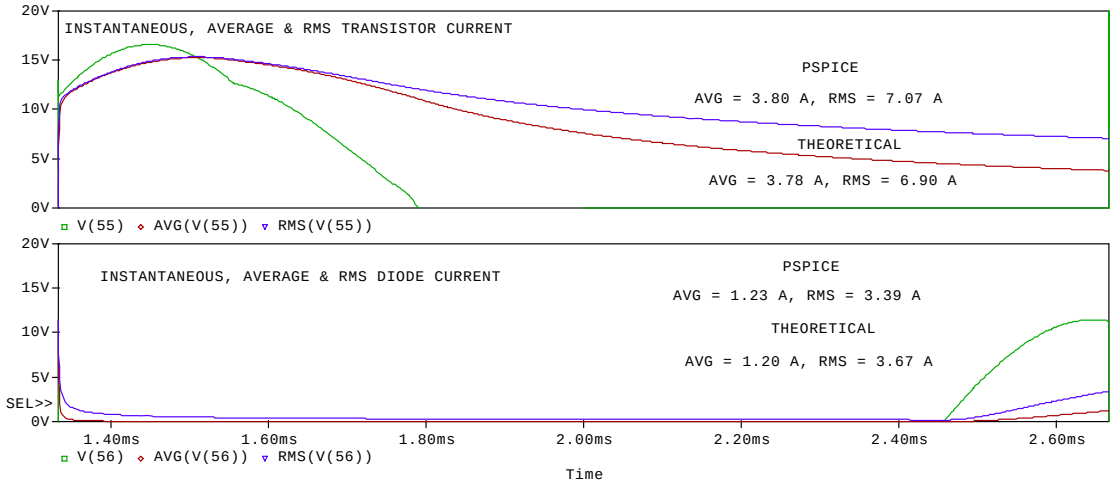
$$\begin{aligned} I &= 11.05 \text{ A (model), 11.07 (simulation)} \\ I_{q-avg} &= 3.78 \text{ A (model), 3.80 (simulation)} \\ I_{q\text{-}rms} &= 6.90 \text{ A (model), 7.07 (simulation)} \\ I_{d-avg} &= 1.20 \text{ A (model), 1.23 A (simulation)} \\ I_{d-rms} &= 3.67 \text{ A (model), 3.39 A (simulation)} \end{aligned} \quad . \tag{75}$$

The agreement between the simplified model and the detailed simulation is not quite as good at high speed as what was observed below base speed. Perhaps the difference lies in the low-frequency harmonics introduced at high speed by six-step switching. However, transistor average and rms currents between the simplified model and the simulation are within 2.5%. While the difference in rms diode current is more than 7.5%, the average diode currents are within 2.5% of each other. Diode-conduction losses are generally a factor of two smaller than transistor-conduction losses. Except at very high diode currents, the conduction losses of the diodes will be weighted more heavily towards the contribution of the forward voltage drop and average current than by the diode resistance and rms current. Based on this assessment, the simplified model is still considered sufficiently accurate to be used to predict the losses of the CPA driven Motor 1 and Motor 2 designs.

The same high-speed operating condition was examined using the DMIC. Figure 16 is a solved per-phase fundamental-frequency model of the condition using the DMIC.



a. Motor currents and power.



b. Transistor, bypass diode, and thyristor currents.

Fig. 15. Time-domain simulation results of the CPA simulator driving the Motor 2 design at 3000 rpm and 1500 W output with rotational losses included.

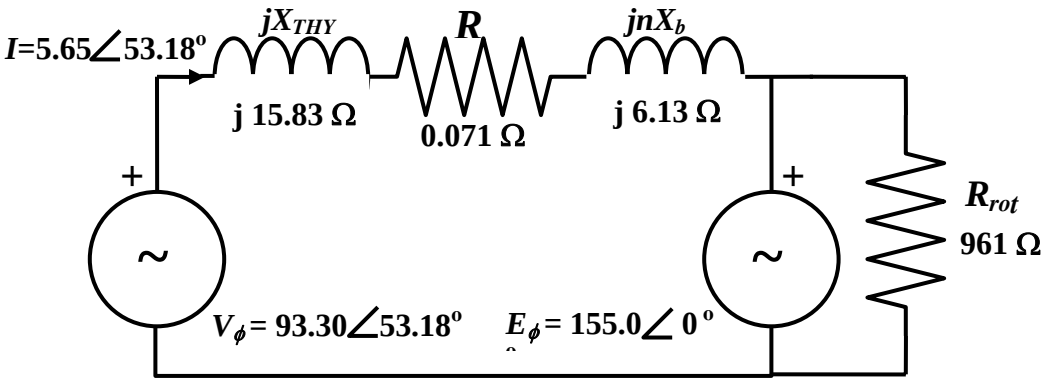


Fig. 16. Per-phase fundamental-frequency model of the Motor 2 design driven by DMIC at 3000 rpm and 1500 W useful output power with rotational losses included.

Observe that the motor efficiency of the DMIC driven Motor 2 at 3000 rpm at 1500 W of useful output is 94.8%. Although not shown here, the motor efficiency of Motor 1 driven at the same condition and from the same dc supply would also be 94.8%.

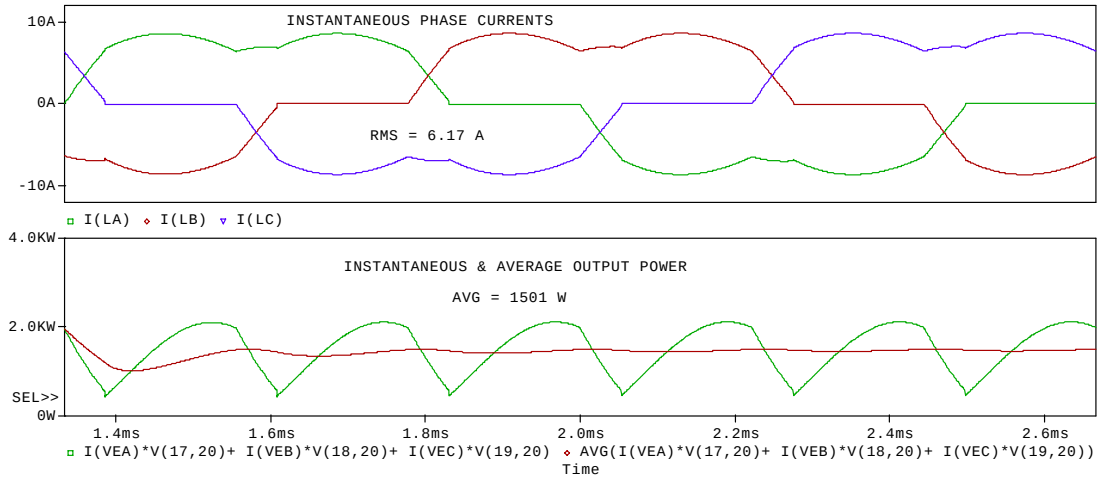
From Fig. 16, we find that

$$\begin{aligned} m_a &= \frac{4}{\pi} \\ I &= 5.65 \text{ A} \\ \delta &= 53.18^{\circ} \\ \theta &= 53.18^{o} \end{aligned} \quad . \tag{76}$$

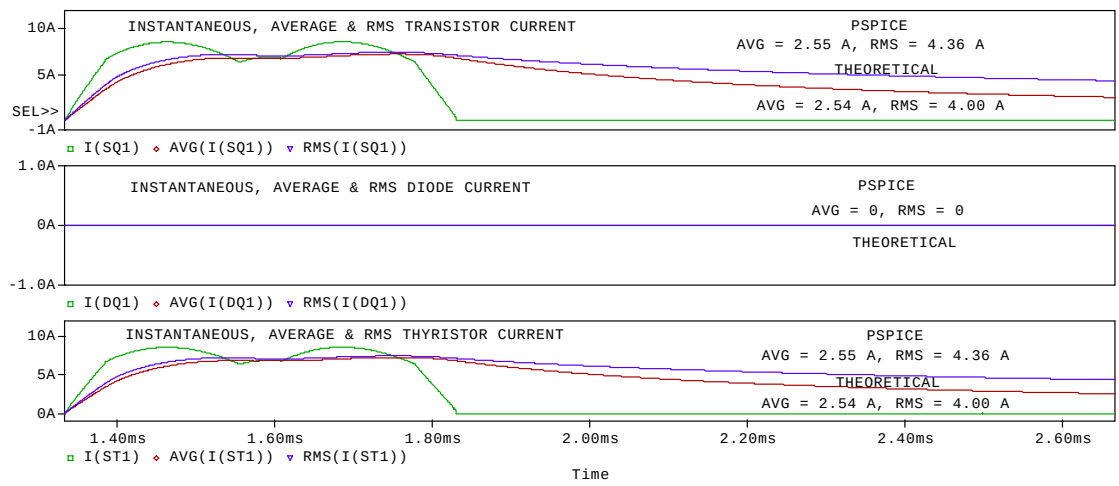
This load condition was simulated using the detailed time-domain DMIC simulator. Simulation results showing phase currents, developed power, and average and rms transistor and bypass diode currents are given in Fig. 17. The device-current magnitudes computed with the fundamental-frequency model formulas are compared below with the values from the simulation

$$\begin{aligned} I &= 5.65 \text{ A (model), } 6.17 \text{ (simulation)} \\ I_{q-avg} &= 2.54 \text{ A (model), } 2.55 \text{ (simulation)} \\ I_{q\text{-}rms} &= 4.00 \text{ A (model), } 4.36 \text{ (simulation)} \\ I_{d-avg} &= 0. \text{ A (model), } 0. \text{ A (simulation)} \\ I_{d-rms} &= 0. \text{ A (model), } 0. \text{ A (simulation)} \\ I_{t-avg} &= 2.54 \text{ A (model), } 2.55 \text{ (simulation)} \\ I_{t\text{-}rms} &= 4.00 \text{ A (model), } 4.36 \text{ (simulation)} \end{aligned} \quad . \tag{77}$$

The fundamental-frequency model predicts the average transistor, diode, and thyristor currents with less than 1% error; however, there is approximately 9% difference between the simplified model and the simulator with respect to the rms transistor and thyristor currents. This is due to the low-frequency harmonics introduced by the six-step switching and by the action of the DMIC inverter at high speed. While this will result in some error in the estimation of the i^2R losses in the transistors and thyristors, the loss of accuracy will be less than 10% of total semiconductor losses assuming that the forward drop losses and body resistance losses are about the same magnitude.



a. Motor currents and power.



b. Transistor, bypass diode, and thyristor currents.

Fig. 17. Time-domain simulation results of the DMIC simulator driving the Motor 1 design at 3000 rpm and 1500 W output with rotational losses included.

The next section considers the calculation of switching losses.

4.2 SWITCHING LOSSES

Figure 18 shows a simplified representation of the dynamics of switch turn-on and turn-off. In the figure, V_{off} and V_{on} are the off-state and on-state voltages respectively, while I_{off} and I_{on} are the off-state and on-state currents. The off-state voltage depends on the dc supply voltage and the on-state current will be dependent on the impedance of the load. The turn-on and turn-off times are denoted as τ_{on} and τ_{off}. The off-state current and on-state voltages have minimal impact on the total energy absorbed by the switch during turn-on and turn-off. Neglecting I_{off} and V_{on}, the energy absorbed during one turn-on and one turn-off operation, as depicted in the idealization of Fig. 18, is given by

$$
\begin{aligned}
E_{sw} &= E_{on} + E_{off} \\
E_{on} &= \frac{V_{off} I_{on}}{6} \cdot \tau_{on} \quad . \\
E_{off} &= \frac{V_{off} I_{on}}{6} \cdot \tau_{off}
\end{aligned}
\tag{78}
$$

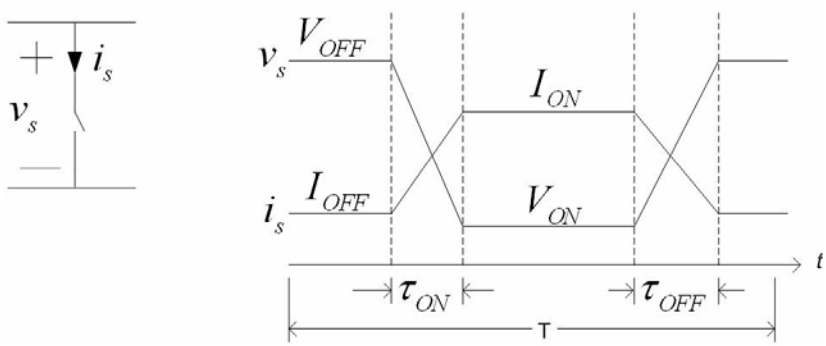


Fig. 18. Simplified description of switching dynamics during turn-on and turn-off.

If there is one turn-on and one turn-off operation each time period, T, then the average switching losses over one period is given by

$$
\begin{aligned}
P_{sw} &= \frac{1}{T}\left(E_{on} + E_{off}\right) \\
&= f\left(E_{on} + E_{off}\right) . \\
&= f\ E_{sw}
\end{aligned}
\tag{79}
$$

The voltage and current dynamics of semiconductors undergoing switching can be much more complicated than the idealization shown in Fig. 18. Generally, device-data sheets will display switching losses versus on-state current for a fixed voltage and one or more device temperatures, such as 25°C and 125°C. Such characteristics can easily be corrected for actual voltage conditions since the switching energy is generally linear in voltage. In this study and evaluation, temperature effects will be incorporated by choosing the characteristics associated at maximum device temperature.

The switching losses described above apply to transistors. The main switching losses of diodes and thyristors are associated with reverse recovery which is described in the next section.

4.3 REVERSE-RECOVERY LOSSES

The reverse-recovery phenomenon is associated with a conducting diode or thyristor undergoing transition from the forward-current conducting state to the reverse-voltage blocking state. The process is dependent on forward current, reverse voltage, and temperature. Idealized voltage and current waveforms are shown in Fig. 19. In the figure, I_{on} is the initial forward current, I_{rr} is the peak reverse-recovery current, V_R is the final reverse voltage, t_a is the time between the current zero crossing and the instant that the peak reverse current is reached, t_b is the time for the reverse current to decay to 10% of the peak-

reverse current, and t_{rr} is the reverse-recovery time which is the sum of t_a and t_b. For most devices, the reverse-recovery time is dominated by the time, t_b. Since the device voltage is approximately zero during the interval denoted as t_a, the energy absorbed during reverse recovery is given by

$$E_{rr} = V_R \frac{I_{rr}}{2} t_b \approx V_R \frac{I_{rr}}{2} t_{rr} = 0.5 V_R Q_{rr}, \tag{80}$$

where Q_{rr} is the peak-recovery charge.

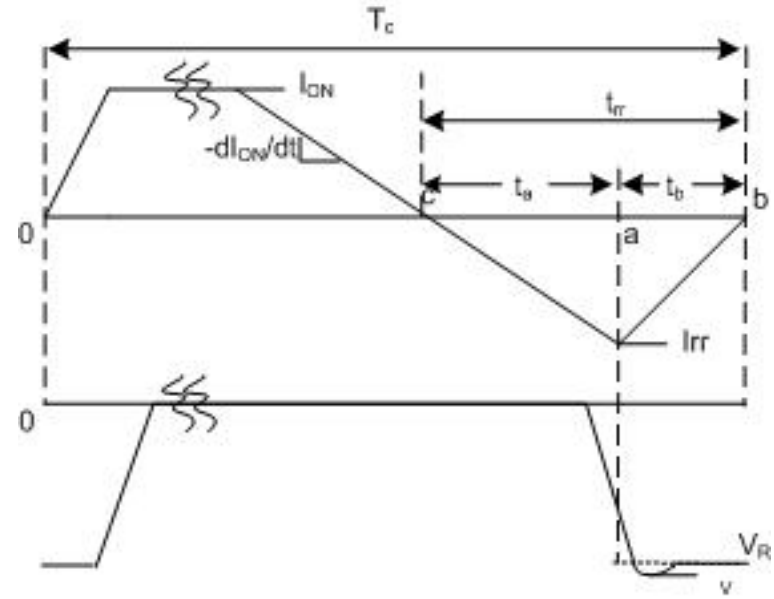


Fig. 19. Reverse-recovery current and voltage.

If there is one reverse recovery during each time period, T, then the average power loss during recovery is

$$P_{rr} = \frac{1}{T} E_{rr} = f\ E_{rr}. \tag{81}$$

A device-data sheet may specify the information needed to determine E_{rr} in various ways. One common method for bypass diodes is to provide plots of reverse-recovery time, t_{rr}, and reverse-recovery current, I_{rr}, versus the forward current through the companion transistor. In the case of CPA and DMIC, the forward current through the companion transistor can be represented as the "average transistor current" as determined in Section 4.1. For thyristors, the reverse-recovery charge, Q_{rr}, may be plotted versus the time rate of change of thyristor current at turn-off for various values of forward current. In the DMIC application, the commutation of thyristors is natural and occurs at the zero crossings of the thyristor current. Thus, it is appropriate to choose the Q_{rr} curve corresponding to the smallest forward current for which data is given. The time rate of change of current can be approximated using the fundamental-current component. Let the instantaneous fundamental current be written as

$$i_1(t) = \sqrt{2} I \sin\left(n\omega_b t + \theta\right). \tag{82}$$

Then the rate of change of this current at its zero crossing is

$$\frac{di}{dt} \to n\omega_b \sqrt{2} I \,. \tag{83}$$

In addition, the voltage blocked by a commutating thyristor at the commutation instant is not necessarily the dc supply voltage as it is for the bypass diodes, but rather the instantaneous phase-to-neutral back-emf. Given the fundamental current as above which is zero at the commutation instant so that $n\omega_b t = -\theta$ and the instantaneous phase-to-neutral back-emf

$$e(t) = n\sqrt{2} E_b \sin\left(n\omega_b t\right), \tag{84}$$

the magnitude of the commutating voltage at the commutation instant is

$$V_R = n\sqrt{2} E_b \sin\left(\theta\right). \tag{85}$$

Thus, the rate of change of thyristor current during reverse recovery and reverse voltage both increase linearly with speed; therefore, the reverse-recovery losses of the thyristor will increase more than linearly with speed.

4.4 INVERTER SEMICONDUCTOR SELECTIONS FOR THE MOTOR 1 AND MOTOR 2 DESIGNS AND LOSS-MODEL PARAMETERS

The evaluation of the Motor 1 and Motor 2 designs will include inverter-loss mechanisms based on "typical" semiconductor parameters obtained from manufacturers' data sheets.

The insulated gate bipolar transistor (IGBT) module used with both motor designs is the Fairchild FMG1G75US60H whose data sheet is given in Appendix A.1. The relevant parameters of the module are given in Table 4. This device has 600 V, 75 A capability and switching rate capability up to 20 kHz. This module was specified by the developers of the prototype PMSM that is under study [9].

Two thyristor modules are used. The first is a EUPEC TT46F08 which is an inverter-grade SCR. Data sheet for the TT46F08 is given in Appendix A.2. The second SCR module is a EUPEC TT61N which is a converter-grade SCR. The data sheet for the TT61N is contained in Appendix A.3. The converter-grade SCR has an average forward-current conduction capability of 61 A which is three times larger than required in the Motor 1, Motor 2 applications, and a voltage blocking capability of 1400 V which is more than required. It is not clear whether or not the converter-grade SCR can sustain operation in the application being considered because the fundamental switching rate is 1.5 kHz at top speed of 6000 rpm. This question would have to be answered by experimentation. The 61 A module was the smallest rating device that was available from the manufacturer's website. This device has significant reverse-recovery charge and consequently high reverse-recovery losses. A lower rating device would likely have smaller reverse-recovery losses since the recovery charge is proportional to volume, which would decrease with reduced current rating. The inverter-grade SCR has an average forward-current rating of 45 A which is more than twice the rating required in the applications under study and a voltage blocking capability of

800 V. The inverter-grade SCR has low reverse-recovery charge and losses. The critical parameters for both the inverter and converter-grade thyristors are given in Table 4.

Table 4. Typical semiconductor parameters

IGBT conduction losses from Appendix A.1.
$E_q = 1.2$ V, $R_q = 0.0125\ \Omega$
$E_d = 1.2$ V, $R_d = 0.0097\ \Omega$
Switching losses
$E_{sw} = 4600\ \mu$J/pulse, test voltage = 300 V
Bypass diode reverse recovery
$I_{rr} = 9$ A, $t_{rr} = 130$ nsec, test voltag = 300 V
Inverter-grade thyristor from Appendix A.2
Conduction losses
$E_{thy} = 0.71$ V, $R_{thy} = 0.0034\ \Omega$
Reverse recovery
$Q_{rr} = 30\ \mu coulombs$
Converter-grade thyristor from Appendix A.3
Conduction losses
$E_{thy} = 0.88$ V, $R_{thy} = 0.0034\ \Omega$
Reverse recovery
$\log(Q_{rr}) = 0.2320 \log\left(\frac{di}{dt}\right) + 1.0703$ $\{di/dt$ in amp/sec, Q_{rr} in μcoulombs$\}$

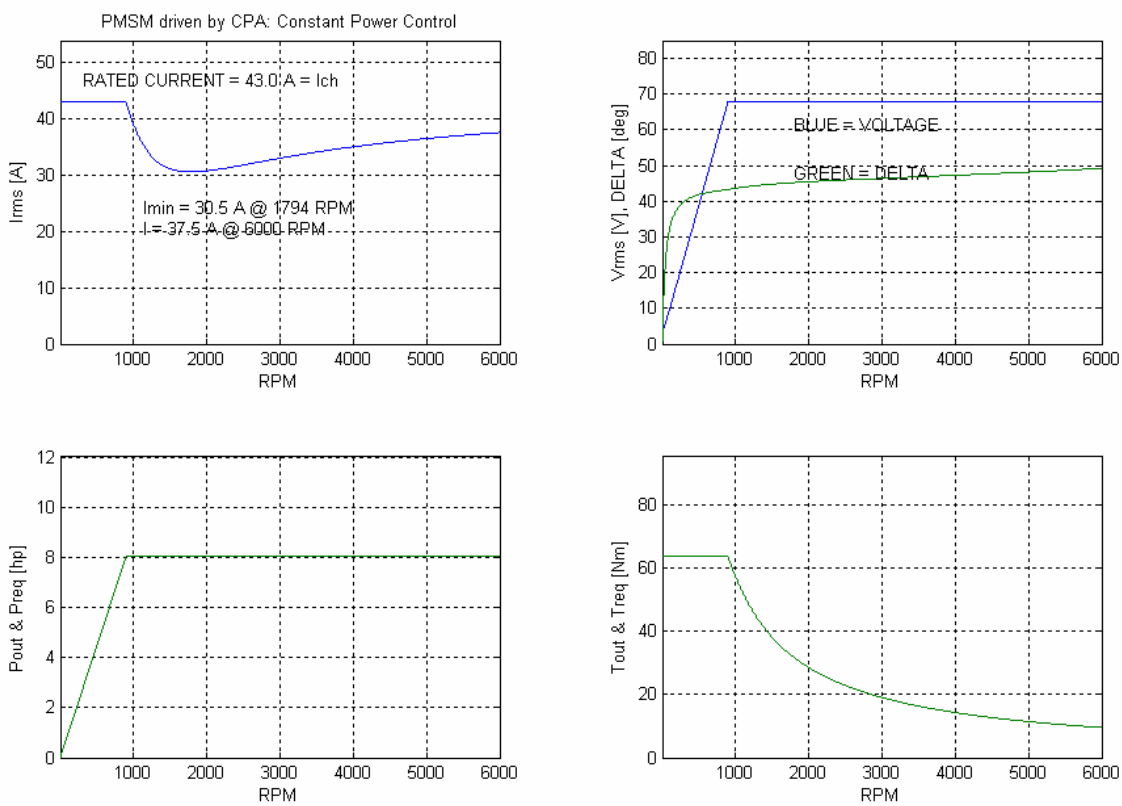
In the next section, the fundamental-frequency model combining motor and inverter losses is used to study the control and performance of Motor 1 when operating at full load and one quarter load over the full speed range. The performance of both the CPA drive and the DMIC case are presented.

4.5 INTEGRATED MOTOR/INVERTER MODEL SIMULATION

Using the motor models developed in Sections 2 and 3 and the inverter model developed above, the performance of Motor 1 was simulated to explore the control over the full speed range when operating at full and at one quarter of rated power. Winding resistance, rotational losses, and inverter losses are included in the simulation. The dc supply voltage is the minimum required to support base-speed condition which is 151 V. For the CPA drive, the IGBT module parameters are those of Table 4. The same IGBT module is used with the DMIC drive and the thyristor parameters are those of the inverter-grade thyristor also given in Table 4.

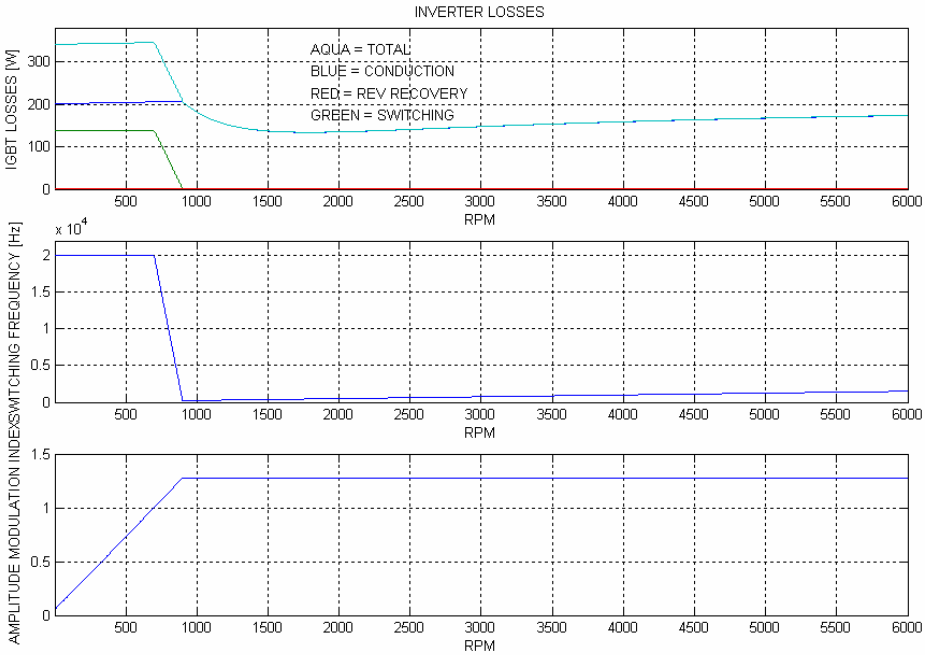
Figure 20 shows the simulation results up to the top speed of 6000 rpm. Figure 20(a) shows the rms motor current, applied fundamental voltage, inverter-lead angle, required and developed power, and required and developed torque versus rpm. Since the motor is being controlled to exactly follow the required torque-speed curve, the required and developed torque curves are identical as are the required and developed power curves. Since the dc supply voltage is the minimum necessary to support rated

power at the specified base speed of 900 rpm, the voltage plot shows that maximum-phase voltage of 68 V is reached at exactly the base speed and is constant for higher speeds. The motor current is the rated current of 43.0 A during the constant-torque zone, drops to a minimum current of 30.5 A during constant-power operation, and is 37.5 A at 6000 rpm. The characteristic current is the same as the rated current of 43.0 A for this motor. Figure 20(b) shows the IGBT losses broken down by conduction loss, switching loss, reverse-recovery loss, and total loss. PWM switching frequency and amplitude-modulation index are also displayed. Note that the switching frequency is at the maximum 20 kHz rate up to that speed where the amplitude-modulation index equals unity and then declines to the fundamental-motor frequency at the base speed of 900 rpm where the amplitude-modulation index reaches the maximum value of $4/\pi$. The IGBT switching losses are approximately 135 W while switching at the 20 kHz and decline to a very low value once the transistor switching becomes the fundamental rate at 900 rpm and above. The conduction losses are approximately 205 W at low speed and the shape of the conduction-loss curves is similar to the rms motor-current curve shown in Fig. 20(a). Figure 20(c) displays motor losses and efficiency, inverter losses and efficiency, output power, total losses, and total drive efficiency versus speed. The efficiency of the motor, inverter, and overall drive are marked at 3000 and 6000 rpm. Note that the motor losses at 6000 rpm are 600 W, which is composed of 300 W of rotational loss (Table 1) and 300 W of copper losses. The total inverter losses are approximately 180 W at 6000 rpm. For comparison, the results of this same case with the DMIC drive are given below.

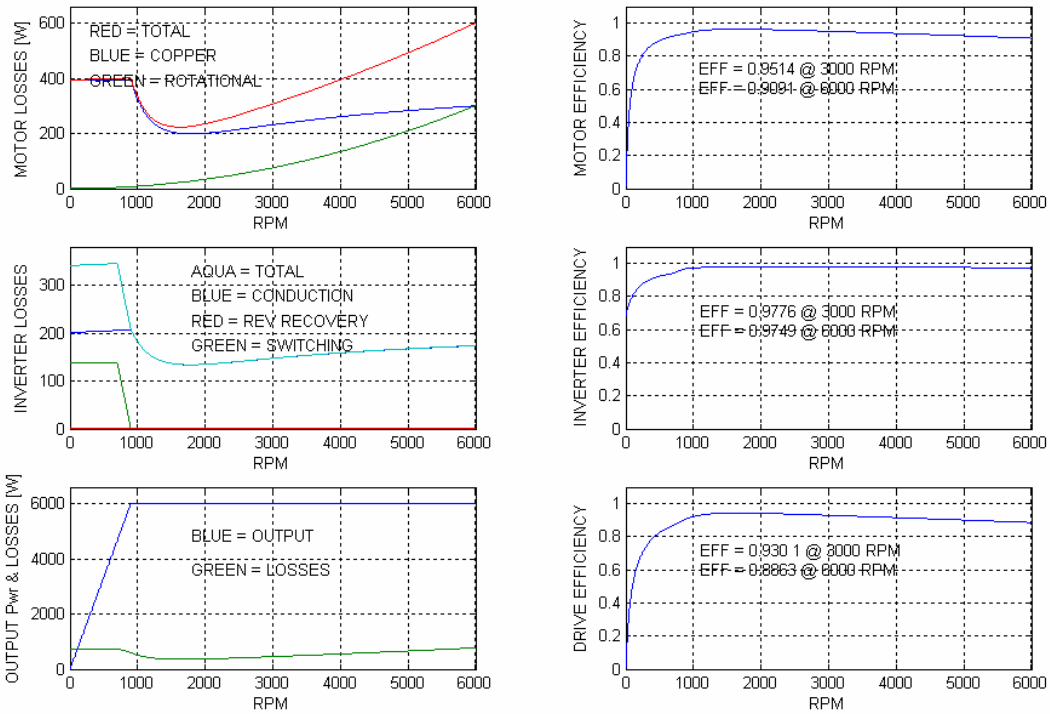


a. RMS current, applied fundamental voltage, lead angle, required and developed power, and required and developed torque vs. rpm.

Fig. 20. Simulation of Motor 1 driven by CPA, operating at full load (6000 W) from a 151 Vdc supply voltage.



b. IGBT losses, PWM switching frequency, and amplitude-modulation index vs. rpm.

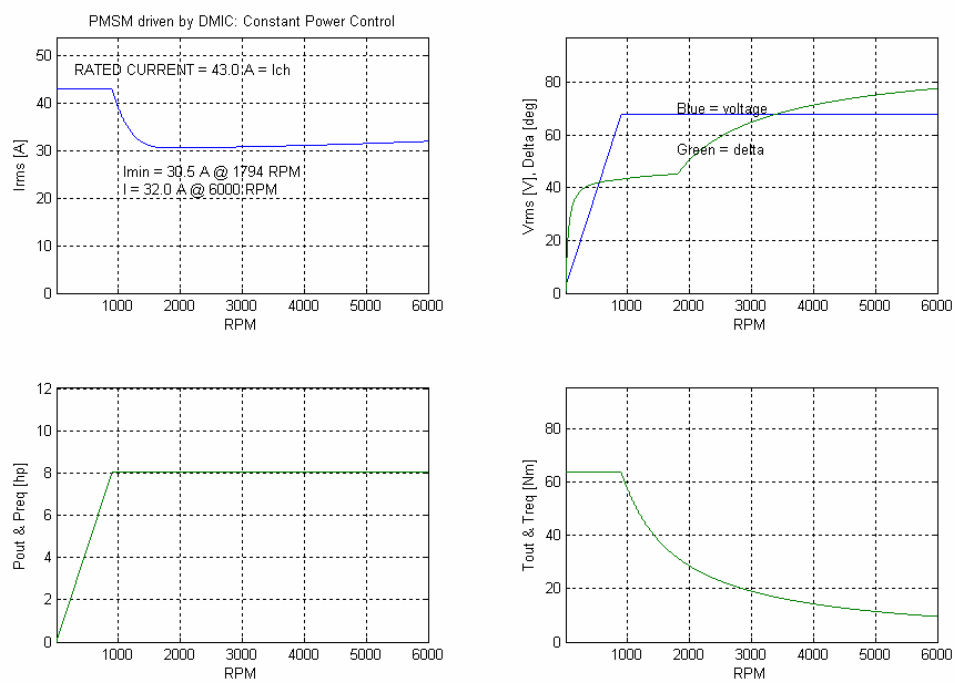


c. Motor losses and efficiency, inverter losses and efficiency, output power, total losses, and overall efficiency vs. rpm.

Fig. 20. Simulation of Motor 1 driven by CPA, operating at full load (6000 W) from a 151 Vdc supply voltage (cont'd).

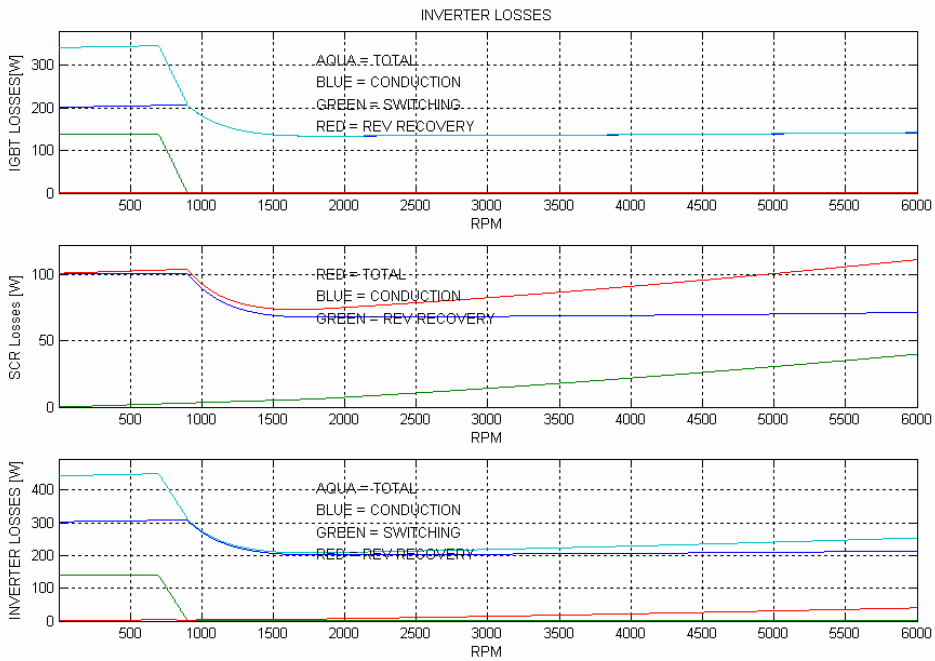
Figure 21 shows the simulation results for Motor 1 at full load over the speed range operating from a 151 Vdc supply when driven by DMIC. Figure 21(a) is completely analogous to Fig. 20(a) which was for the DMIC drive. Note that the rms current from zero speed to 1794 rpm, which is where the minimum current is observed, is the same as for the CPA drive. Beyond 1794 rpm, the DMIC drive current is held nearly at the minimum current but rises slightly due to the increase in motor-rotational losses with speed. The current at 6000 rpm is 32 A as compared to 37.5 A for the CPA case. Figure 21(b) displays the IGBT losses, the thyristor losses, and the total inverter losses versus speed. The low speed (less than 900 rpm) total inverter losses are about 440 W which are composed of 340 W in the IGBTs and 100 W in the thyristors. For the CPA case as shown in Fig. 20(b), the total inverter losses were just the IGBT losses of 340 W. Thus, the DMIC efficiency from zero speed up to at least base speed will be worse than CPA due to the identical motor currents and the added losses in the thyristors.

Figure 21(c) is analogous to that of Fig. 20(c) and displays motor losses and efficiency, inverter losses and efficiency, output power, and total losses and efficiency versus rpm. The motor, inverter, and overall drive efficiencies are indicated on the figure for 3000 and 6000 rpm. Observe that the total efficiency of the DMIC drive at 3000 rpm, 0.9293 is slightly worse than that of the CPA drive, 0.9301. At 6000 rpm, the overall efficiency of the DMIC drive is 0.8875 which is about the same as that of the CPA drive, 0.8863. A comparison based solely on full-load operation does not favor the DMIC drive since its efficiency isn't clearly superior in view of the added cost of the thyristors. At less than full load, the current minimization feature of the DMIC makes its performance much more desirable. This will be shown by rerunning the simulations for one quarter full load across the 6000 rpm speed range.

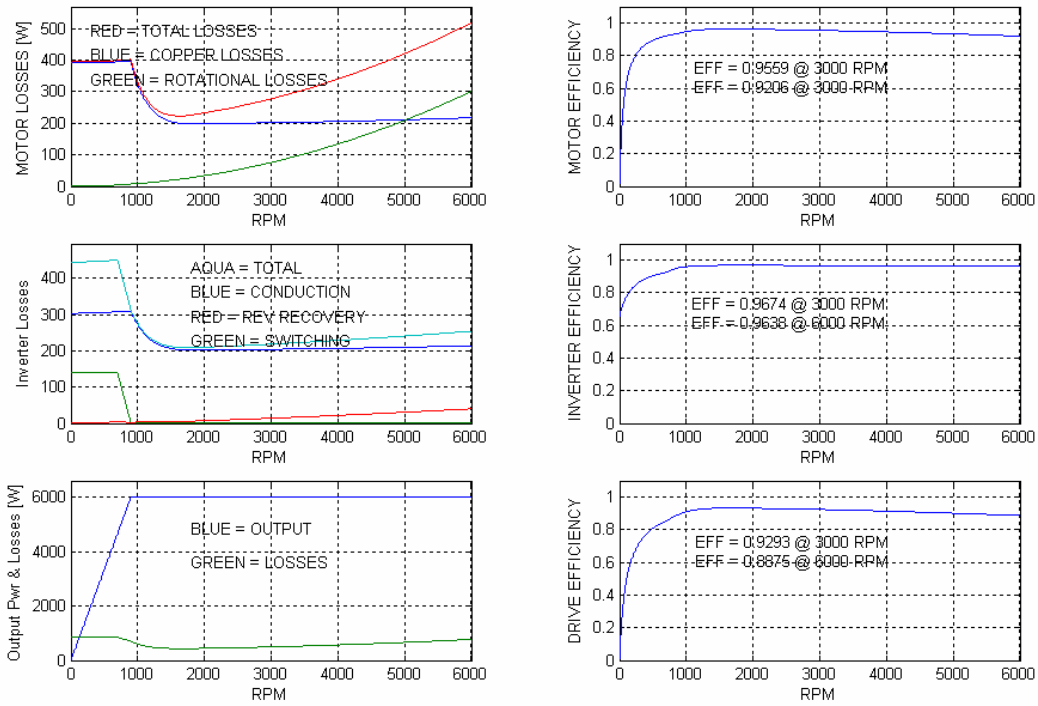


a. RMS current, applied fundamental voltage, lead angle, required and developed power, and required and developed torque vs. rpm.

Fig. 21. Simulation of Motor 1 driven by DMIC, operating at full load (6000 W) from a 151 Vdc supply voltage.



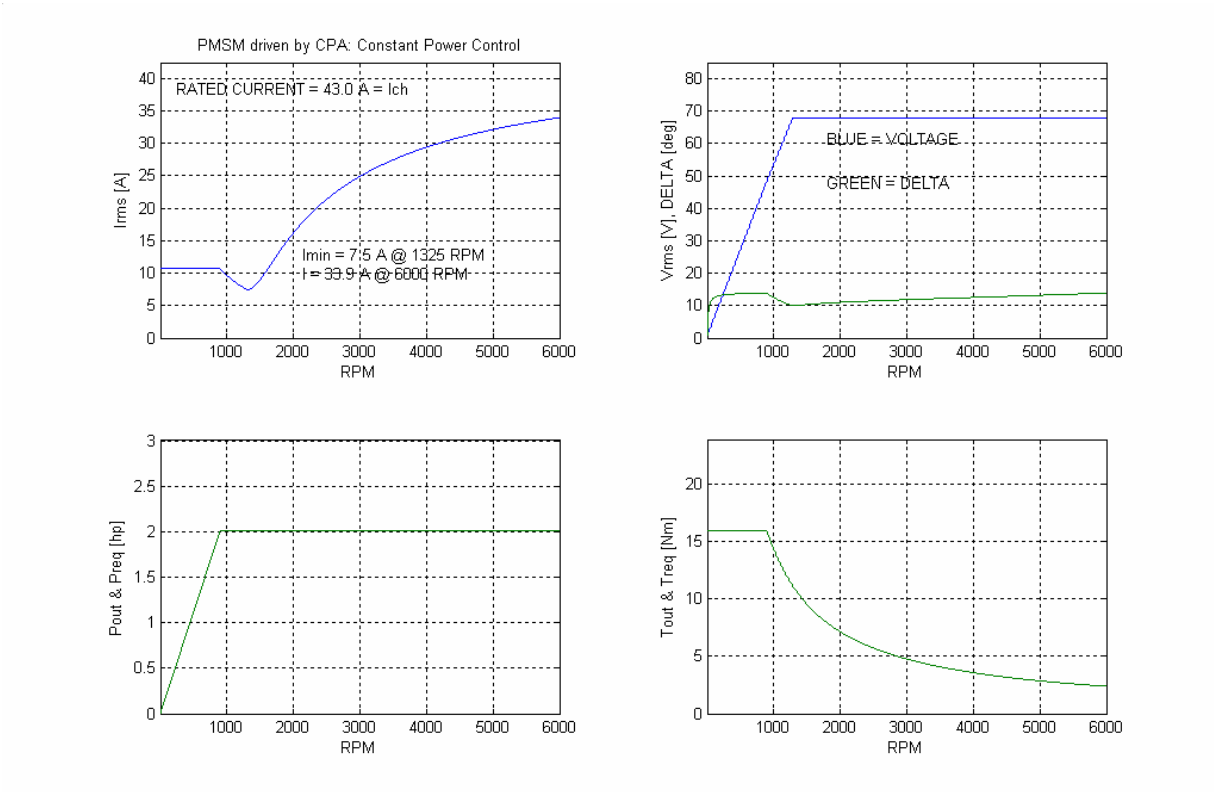
b. IGBT losses, SCR losses, and total inverter losses vs. rpm.



c. Motor losses and efficiency, inverter losses and efficiency, output power, total losses, and overall efficiency vs. rpm.

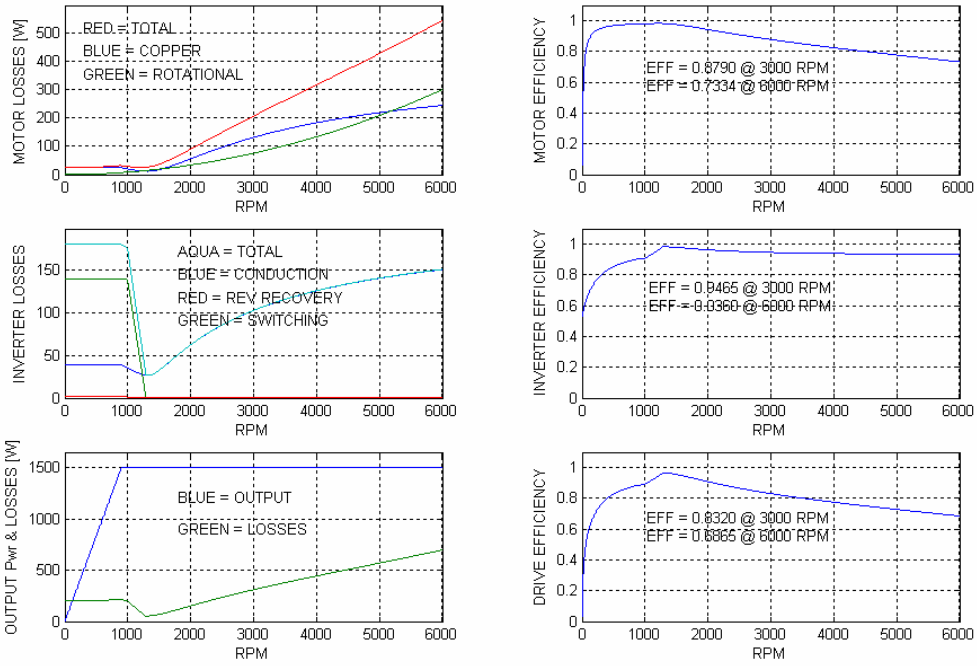
Fig. 21. Simulation of Motor 1 driven by DMIC, operating at full load (6000 W) from a 151 Vdc supply voltage (cont'd).

Figure 22 shows the simulated performance of Motor 1 when operating at one quarter load over the 6000 rpm speed range when driven by CPA. Figure 22(a) displays the rms motor current, applied rms fundamental phase voltage, inverter-lead angle, required and developed power, and required and developed torque. The control was implemented for useful output of exactly one quarter of full load at each speed. Note that the minimum current is 7.5 A at 1325 rpm, but as speed increases the current magnitude approaches the characteristic current (43.0 A) and reaches a value of 33.9 A at 6000 rpm. One should expect that the efficiency at one quarter load will be poor due to the tendency of the motor current towards the characteristic value. Figure 22(b) displays motor losses and efficiency, inverter losses and efficiency, total losses, and overall drive efficiency versus rpm. The motor, inverter, and total drive efficiencies at 3000 and 6000 rpm are indicated on the figure. For comparison, the same load condition was run for the DMIC drive and the results are displayed in Fig. 23.



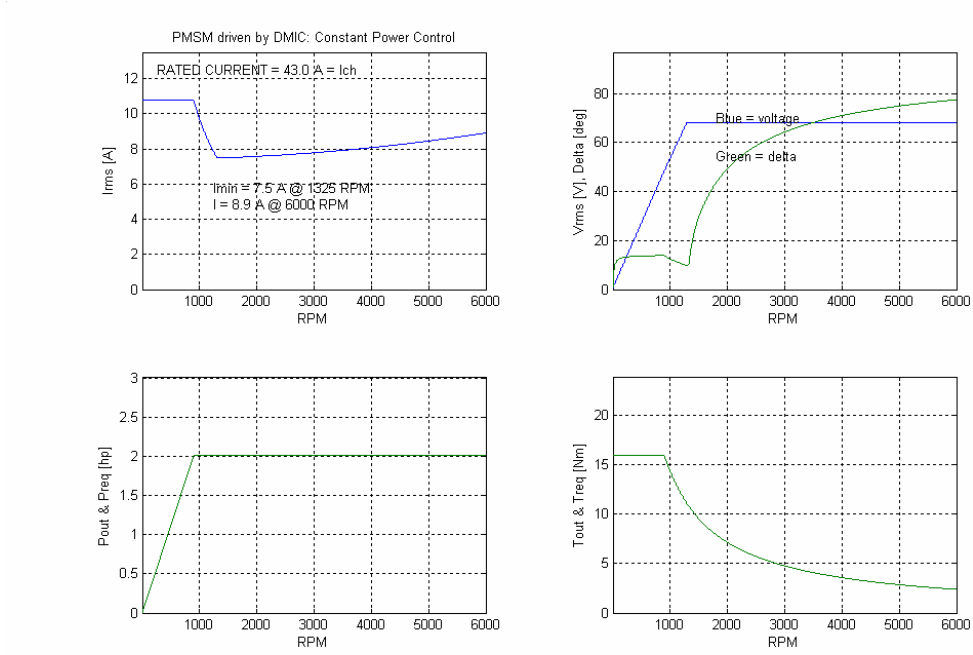
a. RMS current, applied fundamental voltage, lead angle, required and developed power, and required and developed torque vs. rpm.

Fig. 22. Simulation of Motor 1 driven by CPA, operating at quarter of load (1500 W) from a 151 Vdc supply voltage.

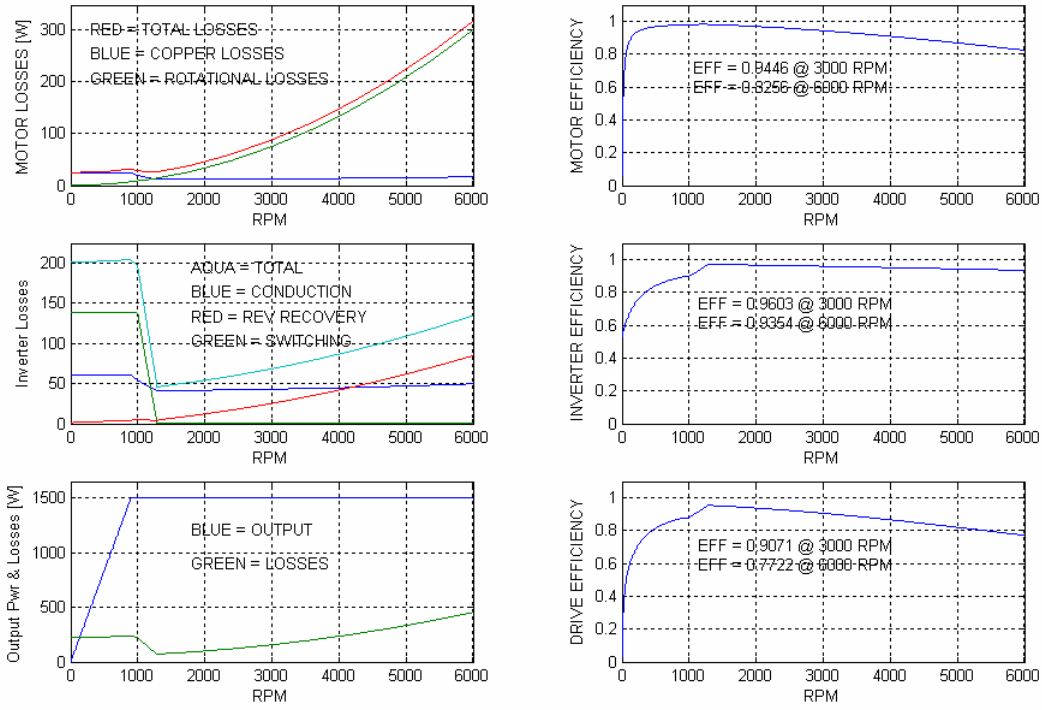


b. Motor losses and efficiency, inverter losses and efficiency, output power, total losses, and overall efficiency vs. rpm.

Fig. 22. Simulation of Motor 1 driven by CPA, operating at quarter of load (1500 W) from a 151 Vdc supply voltage (cont'd).



a. RMS current, applied fundamental voltage, lead angle, required and developed power, and required and developed torque vs. rpm.



b. Motor losses and efficiency, inverter losses and efficiency, output power, total losses and overall efficiency vs. rpm.

Fig. 23. Simulation of Motor 1 driven by DMIC, operating at quarter load (1500 W) from a 151 Vdc supply voltage.

Figure 23(a) shows that the minimum current with DMIC for one quarter load is 7.5 A at 1325 rpm, which is the same as observed with CPA. However, as speed increases above 1325 rpm, the rms motor current with the DMIC remains about the same as the minimum value, but rises slightly to satisfy increased rotational losses in the motor. At 6000 rpm, the current is 8.9 A as compared to 33.9 A for CPA. Figure 23(b) shows the motor, inverter, and overall drive efficiency. Efficiency values at 3000 and 6000 rpm are marked on the figure. The overall efficiency of the DMIC drive is 7.5% percentage points higher at 3000 rpm (0.9071 versus 0.8320) and 8.6% percentage points higher at 6000 rpm (0.7722 versus 0.6865). These improvements are due to the current minimizing capability of the DMIC at high speed. Note that the motor efficiency with the DMIC is 0.8256 at 6000 rpm. While this value seems low, the motor has 300 W of rotational losses at 6000 rpm. These rotational losses are beyond the influence of the motor drive. When developing 1500 W of useful power, the motor efficiency would be 0.8333, assuming no copper losses. Thus, the DMIC value of 0.8256 is quite high considering that the motor efficiency with the CPA drive was 0.7334.

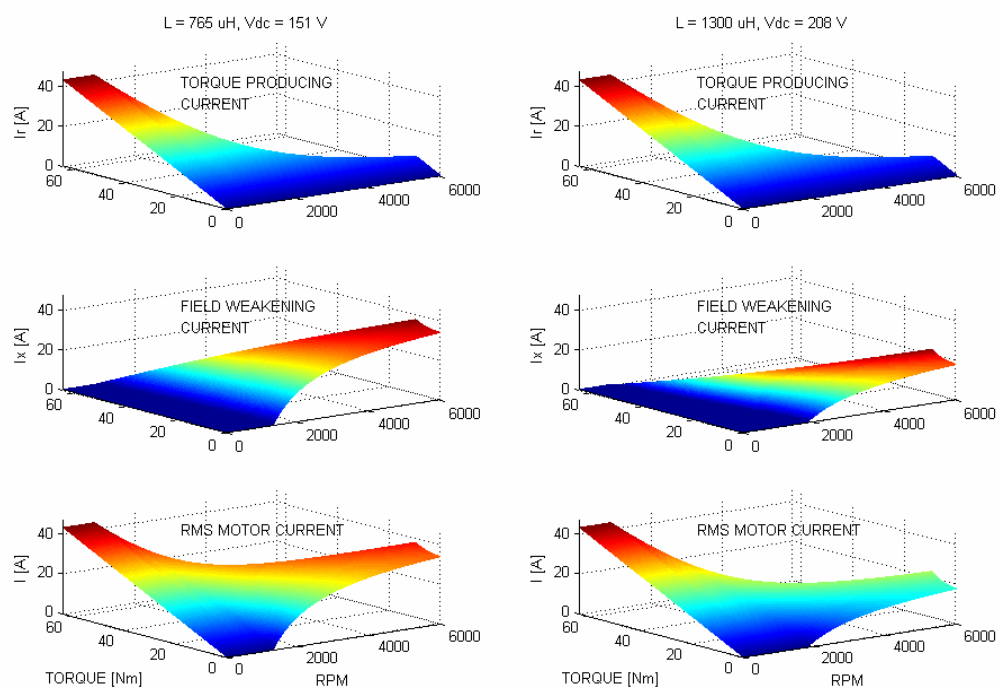
Impact of dc supply voltage, inductance, and drive topology are addressed in the next section using the models developed above.

5. IMPACT OF SUPPLY VOLTAGE, INDUCTANCE, AND INVERTER TOPOLOGY ON DRIVE PERFORMANCE

In this section, the two example motors are used to explore the benefits of having inductance higher than the optimal value, the potential benefit of providing extra dc supply voltage, the potential benefit of DMIC versus CPA, and the impact of thyristor reverse-recovery losses on the performance of DMIC drives.

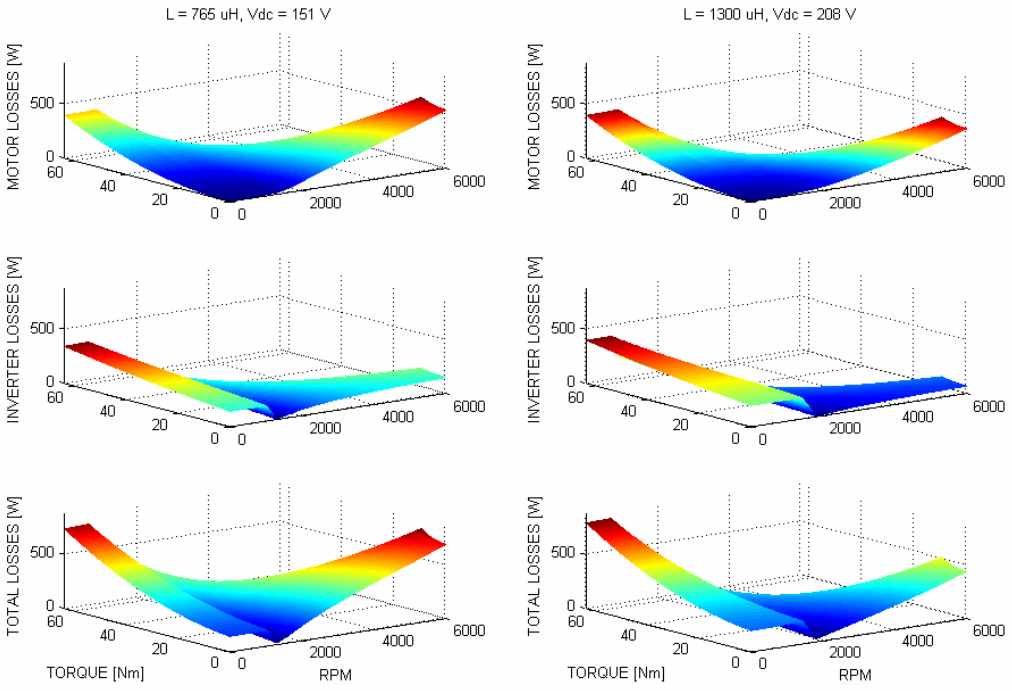
5.1 IMPACT OF MOTOR INDUCTANCE BEING HIGHER THAN "OPTIMAL"

Motor inductance is a critical factor in determining the CPSR of a PMSM when driven by CPA. For the two motors being evaluated in this study, the first has the "optimal" inductance of 765 μH while the second has a much larger value, 1300 μH. In the first section below, the performance of these two motors are compared over the entire torque-speed range using the fundamental-frequency model developed in previous sections. Each motor is supplied by a dc voltage sufficient to achieve rated torque, 63.7 Nm, at the specified base speed. For the low-inductance motor, the supply voltage is 151 V while the higher inductance requires a 208 V supply. Performance was simulated for values of rpm from 20–6000 rpm in steps of 20 rpm and for load levels from full load down to 25/6000 of full load in steps of 25/6000 of full load. Results of the simulations are shown in Fig. 24. The plots in Fig. 24 and in subsequent plots in this section are three-dimensional renderings with shading. The colors used in the shading denote magnitude. The highest values are red; the lowest values are dark blue. The transition from high value to low value is red to yellow to green to aqua to blue. The x axis of each plot is rpm from 0–6000 while the y axis is torque from 0–63.7 Nm. The z axis variable and its scaling depends on the quantity being displayed.

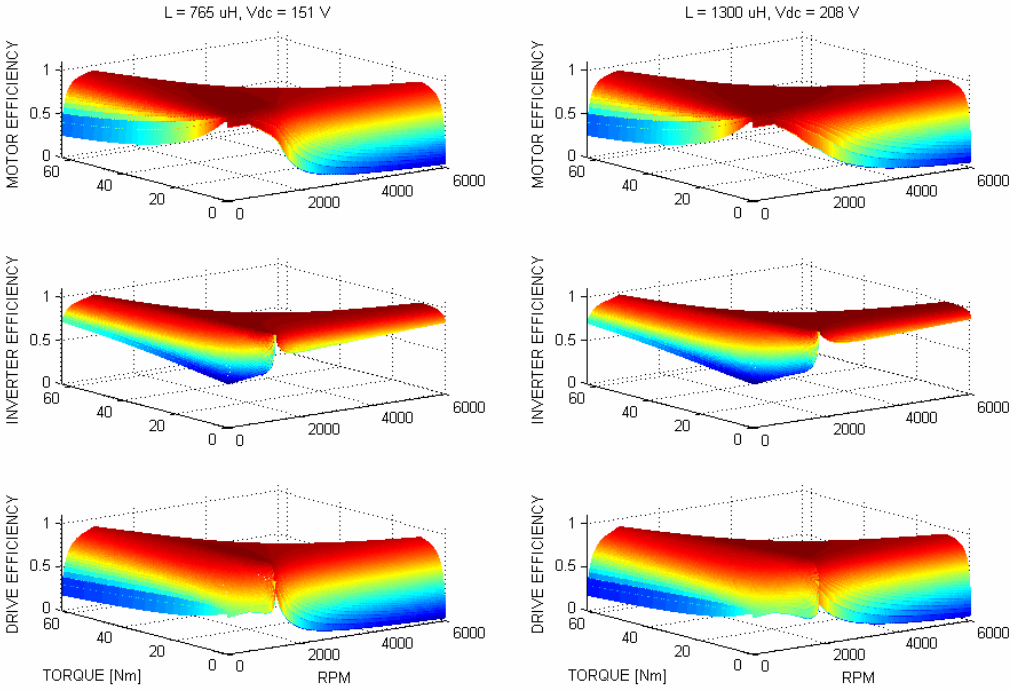


a. Comparison of torque-producing current, field-weakening current, and rms current.

Fig. 24. Performance comparison of Motor 1 (with 151 Vdc supply voltage) and Motor 2 (with 208 Vdc supply voltage) when driven by CPA over the full torque-speed envelope.

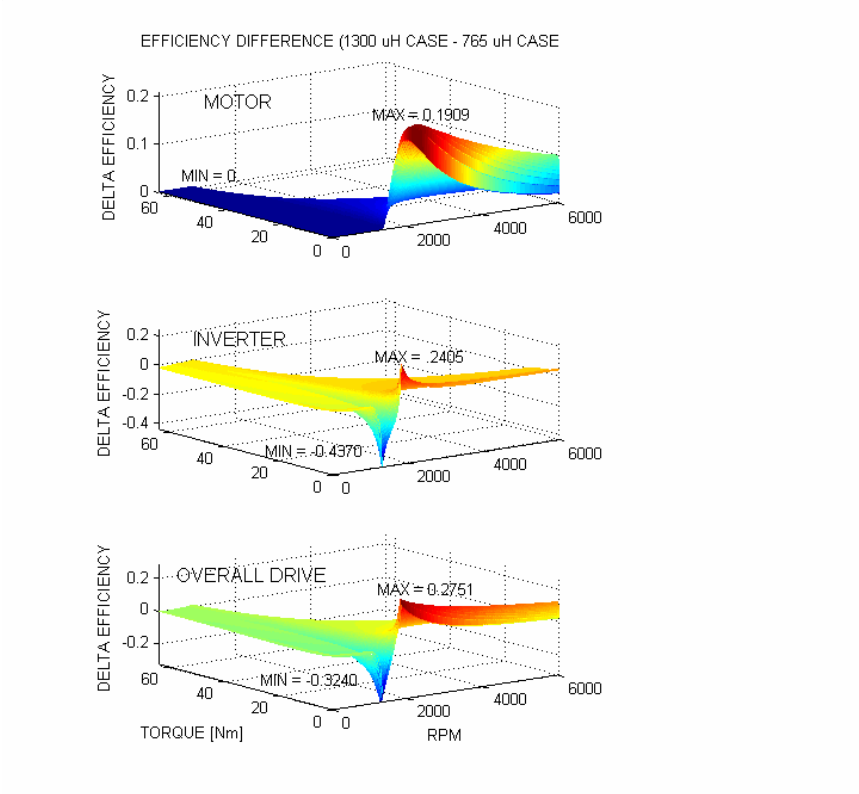


b. Comparison of motor, inverter, and total drive losses.

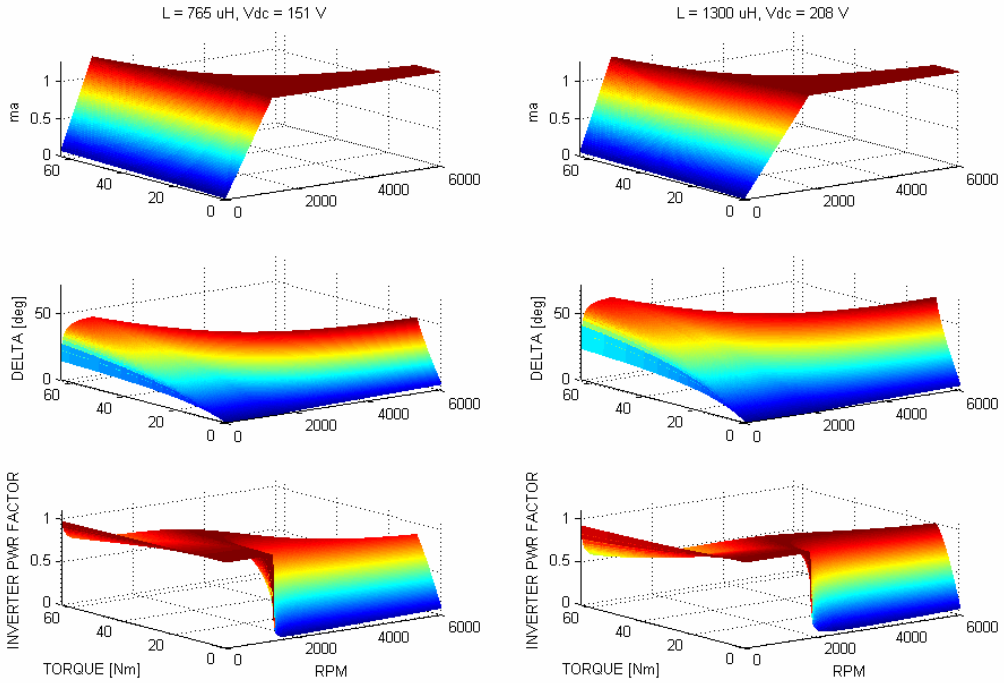


c. Comparison of motor, inverter, and drive efficiency.

Fig. 24. Performance comparison of Motor 1 (with 151 Vdc supply voltage) and Motor 2 (with 208 Vdc supply voltage) when driven by CPA over the full torque-speed envelope (cont'd).



d. Motor, inverter, and overall drive efficiency differences.



e. Comparison of amplitude-modulation index, lead angle, and inverter-power factor.

Fig. 24. Performance comparison of Motor 1 (with 151 Vdc supply voltage) and Motor 2 (with 208 Vdc supply voltage) when driven by CPA over the full torque-speed envelope (cont'd).

Figure 24(a) compares the torque-producing current component, I_r, field-weakening current component, I_x, and rms motor current, I, for the two motors. Since the two motors are controlled to achieve the same torque-speed conditions, the torque-producing current components are identical; however, the field-weakening component is smaller at high-speed conditions for the high-inductance motor. This results in the rms current of the high-inductance motor also being smaller. Figure 24(b) compares the motor losses, inverter losses, and total losses. The motor losses are identical below base speed. Above base speed, the losses of the high-inductance motor are smaller due to its lower current level. The inverter losses of high-inductance motor are slightly larger during operation at and below base speed, 900 rpm. This is due to the fact that the higher inductance motor requires a higher dc voltage supply which increases the switching losses in the IGBTS. During high-speed operation, the switching is at fundamental rate and the dominant loss mechanism in the inverter is the conduction loss. Since the higher inductance motor operates at lower current, the inverter losses are lower at high speed than for the low-inductance machine. Figure 24(c) compares motor, inverter, and overall drive efficiency. Differences between the two motor cases are very difficulty to distinguish due to scaling. Accordingly at each torque-speed condition, the efficiency values for the low-inductance motor were subtracted from the corresponding value for the high-inductance motor. The result is shown in Fig. 24(d). Figure 24(d) shows that, at base speed and below, there are essentially no differences in motor efficiency since, in the constant-torque mode, both motors operate at the same current. However, above base speed the efficiency of Motor 2 is clearly superior being at most 0.1909 larger than that for Motor 1. The inverter efficiency of Motor 2 is less than that of Motor 1 for a small operating region near base speed and encompassing light-load operation. Above base speed, the efficiency of the inverter is higher for Motor 2 and is at most 0.2405 larger than that for Motor 1. The comparison for the overall drive efficiency is similar to that for the inverter. There is a region in the vicinity of base speed and light load where Motor 1 has better over-all efficiency, but for high-speed operating conditions, Motor 2 has greater efficiency by at most 0.2751. Figure 24(e) compares amplitude-modulation index, inverter-lead angle, and inverter-power factor for the two motor cases. The comparison of the modulation index and lead angle shows that the control of these two motors is very similar despite the inductance difference so long as each motor has sufficient dc supply voltage to meet rated torque at base speed. The motor power factors show that, for high-inductance CPA drives, the inverter-power factor is large at high speed when the load is near full load but decreases substantially at low load. This is because the high-speed current is near the characteristic current which is independent of the load.

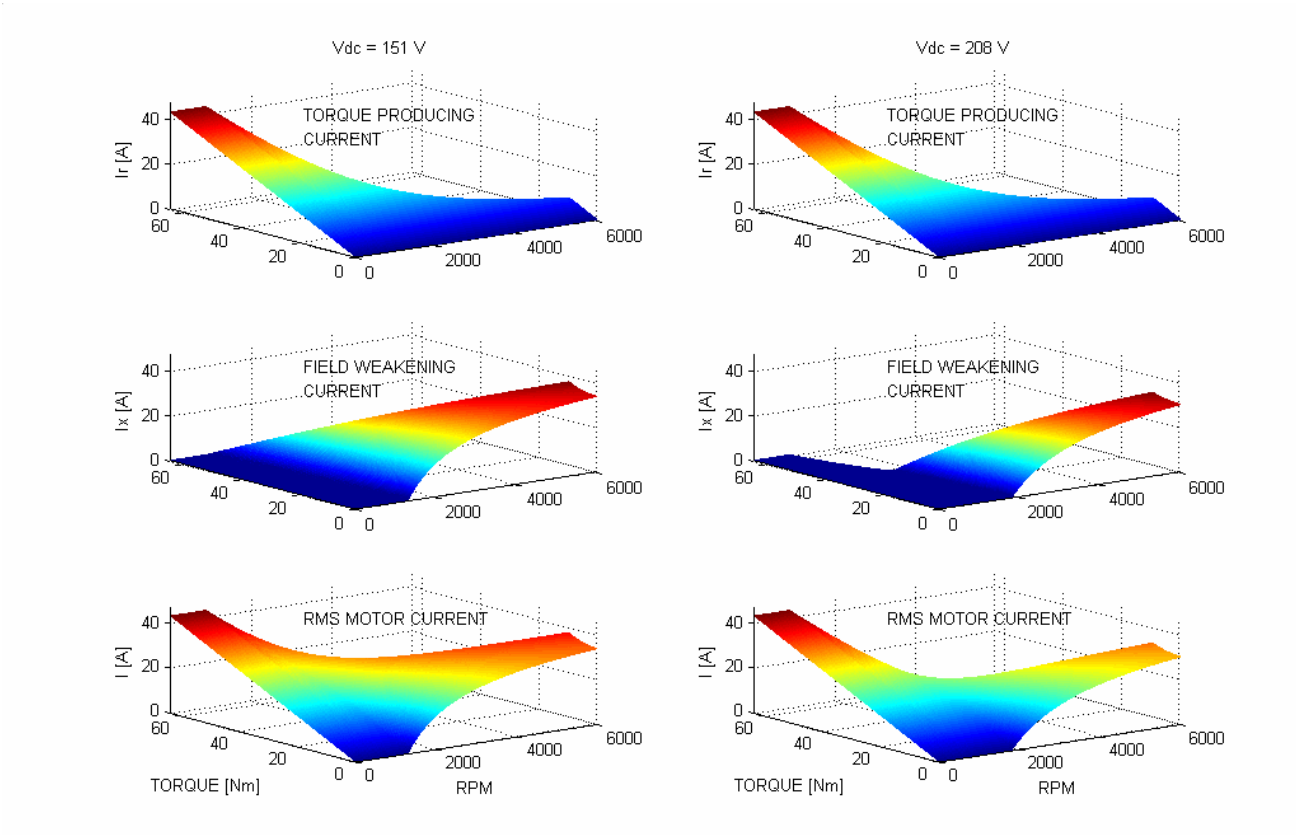
Based on the comparisons in Fig. 24, it is difficult to believe that Motor 1 which has the "optimal inductance" for field weakening is superior to Motor 2 which has 1.7 times as much inductance when both motors are driven by CPA. The characteristic current of Motor 2 is lower than for Motor 1. Since the machine current approaches the characteristic current at high speed, there is a definite advantage for being able to operate at low current. So long as each machine is given sufficient dc supply voltage to support rated torque at base speed, the higher inductance machine will have greater efficiency at high speed. There is a small penalty on the IGBT switching losses at low speed with Motor 2 due to the higher dc supply voltage. The lower inductance Motor 1 would be favored over the higher inductance Motor 2 only in an application where substantial operating time was spent at slow speed conditions.

The next section considers the impact of having a dc supply voltage larger than the minimum required to support rated torque at base speed.

5.2 IMPACT OF DC SUPPLY VOLTAGE GREATER THAN THE MINIMUM

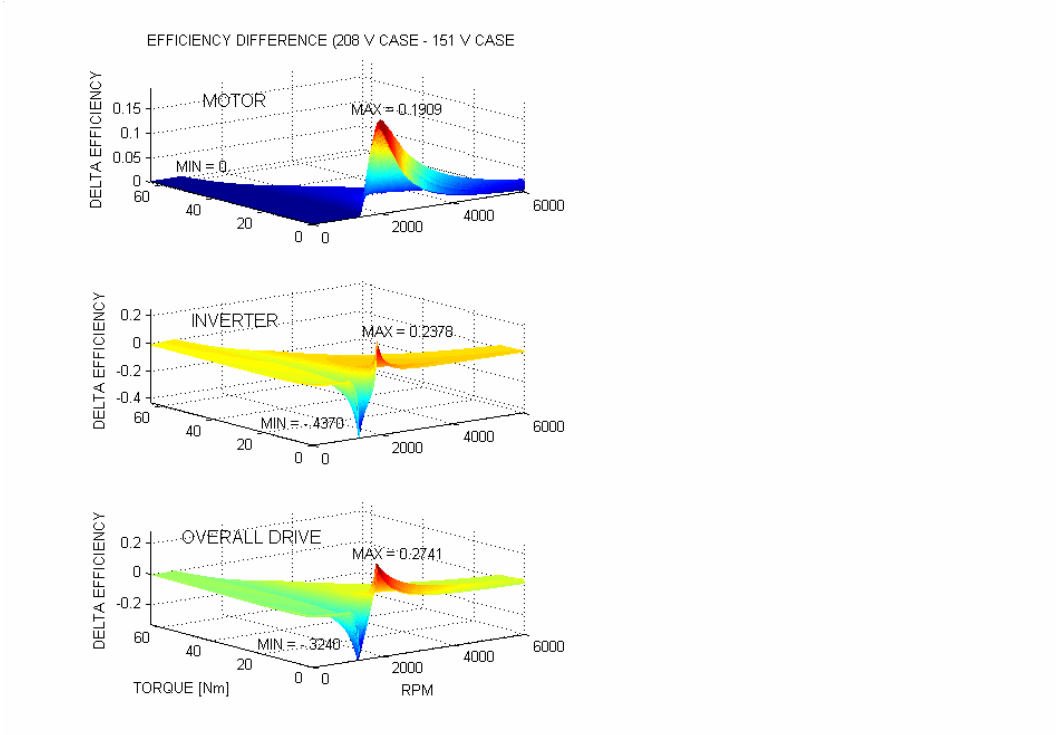
Using a dc supply voltage higher than the minimum necessary to achieve rated torque at base speed can be considered a form of "cheating" to achieve CPSR objectives. Any motor having an inductance higher

than the "optimal" value of L_∞, as given in Eq. (21), has an infinite CPSR. Therefore, any increase in supply voltage above the minimum would not provide improved CPSR but might impact motor current and efficiency. In the previous section, the performance of Motor 1 and Motor 2 were compared with both machines having the minimum dc supply voltage to support rated torque at base speed; which is 151 V for Motor 1 and 208 V for Motor 2. Since the only difference in these two machines is the inductance, it is reasonable to infer that Motor 1 might benefit from the higher voltage that would automatically be provided for Motor 2. The performance of Motor 1 was simulated over the entire torque-speed envelope for these two supply conditions and the results are shown in Fig. 25.

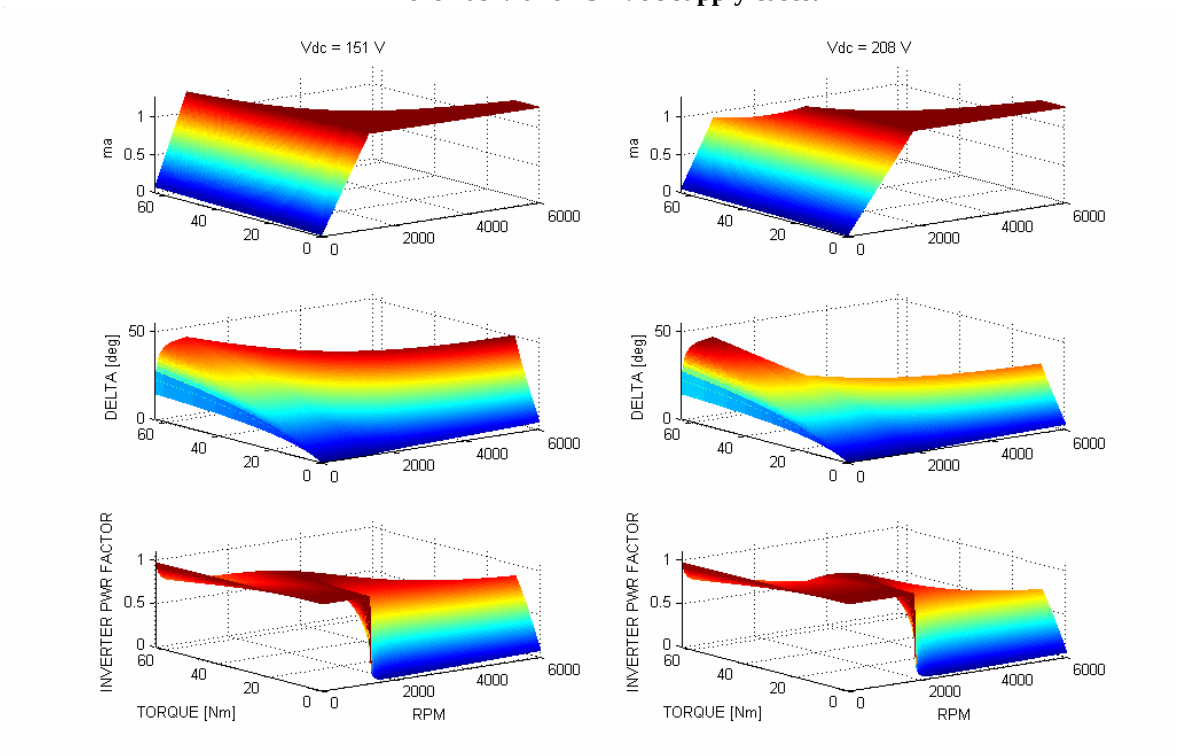


a. Comparison of torque-producing current, field-weakening current, and rms current.

Fig. 25. Comparison of Motor 1 performance when operating from 151 V and 208 Vdc supply voltages when driven by CPA.



b. Motor, inverter, and overall drive efficiency differences between the 208 V and 151 Vdc supply cases.



c. Comparison of amplitude-modulation index, inverter-lead angle, and inverter-power factor.

Fig. 25. Comparison of Motor 1 performance when operating from 151 V and 208 Vdc supply voltages when driven by CPA (cont'd).

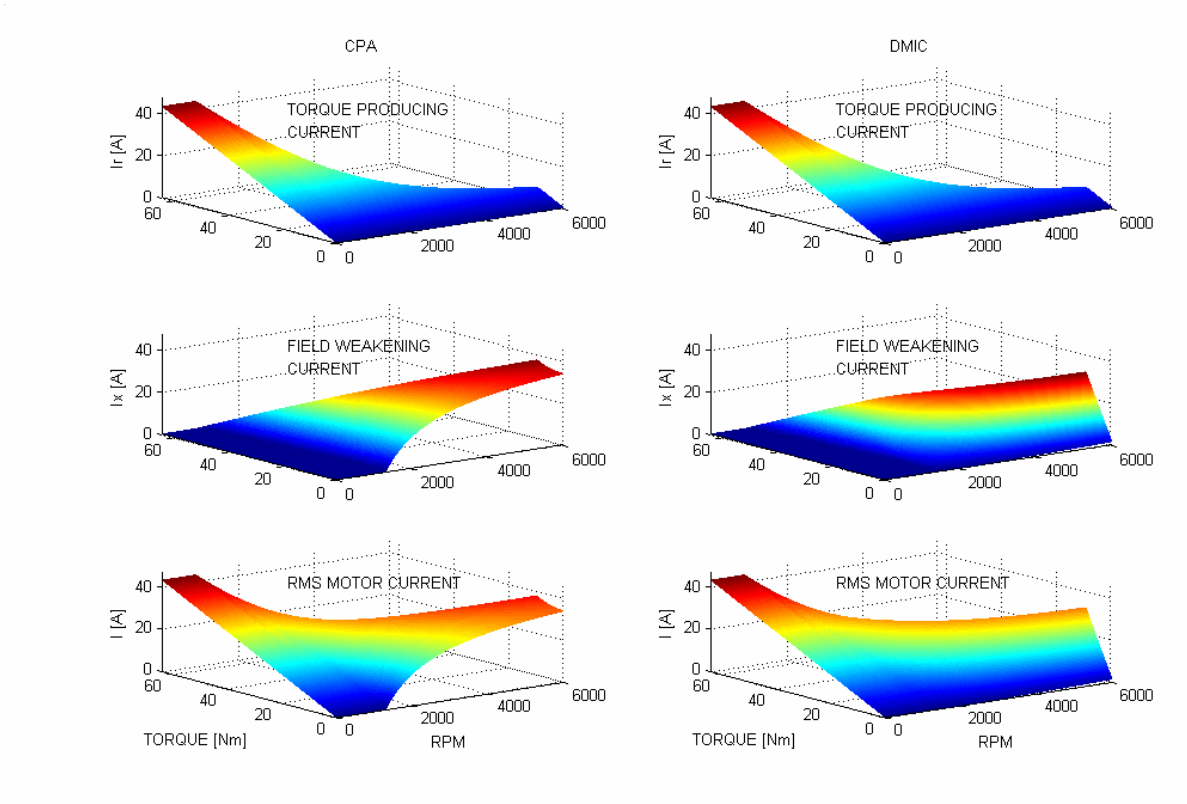
Figure 25(a) shows that the benefit of increased supply voltage is a reduction in field-weakening current. This arises from the fact that the "true base speed" increases from the reduced differential between back-emf and the higher dc supply voltage. Figure 25(b) shows the efficiency of the lower voltage case subtracted from the higher voltage case at each torque-speed operating condition. This is done for the motor, inverter, and overall drive efficiency. The figure shows that there is a substantial benefit to the motor efficiency when operating at high speed. The benefit is the result of the fact that the minimum rms motor current is reduced by the additional supply voltage as given by Eq. (59) when winding resistance is included or Eq. (19) when winding resistance is neglected. The motor efficiency at high speed is increased by as much as 0.1909 during high-speed operating conditions. There is a small region in the vicinity of base speed with low load where the lower voltage results in greater efficiency. But for high-speed operation, the additional dc supply voltage improves efficiency. It should also be noted that the additional supply voltage increases the maximum power-conversion capability although the control in these simulations constrains operation to the specified torque-speed envelope. Figure 25(c) compares the amplitude-modulation index, inverter-lead angle, and inverter-power factor for the two supply voltage cases. The effect of the additional voltage is clearly seen in the amplitude-modulation index. The power-factor curves confirm again that CPA drives have low power factor at high-speed light-load conditions resulting from the current magnitude tending towards the characteristic current.

Based on the simulation results it would appear that additional supply voltage can be beneficial in improving high-speed efficiency. It might be interesting to try and "optimize" the exact amount of additional dc supply voltage by positioning the unity-power condition to a speed at which the drive would commonly operate for a given application. In automotive applications, this could be an rpm corresponding to 45 mph.

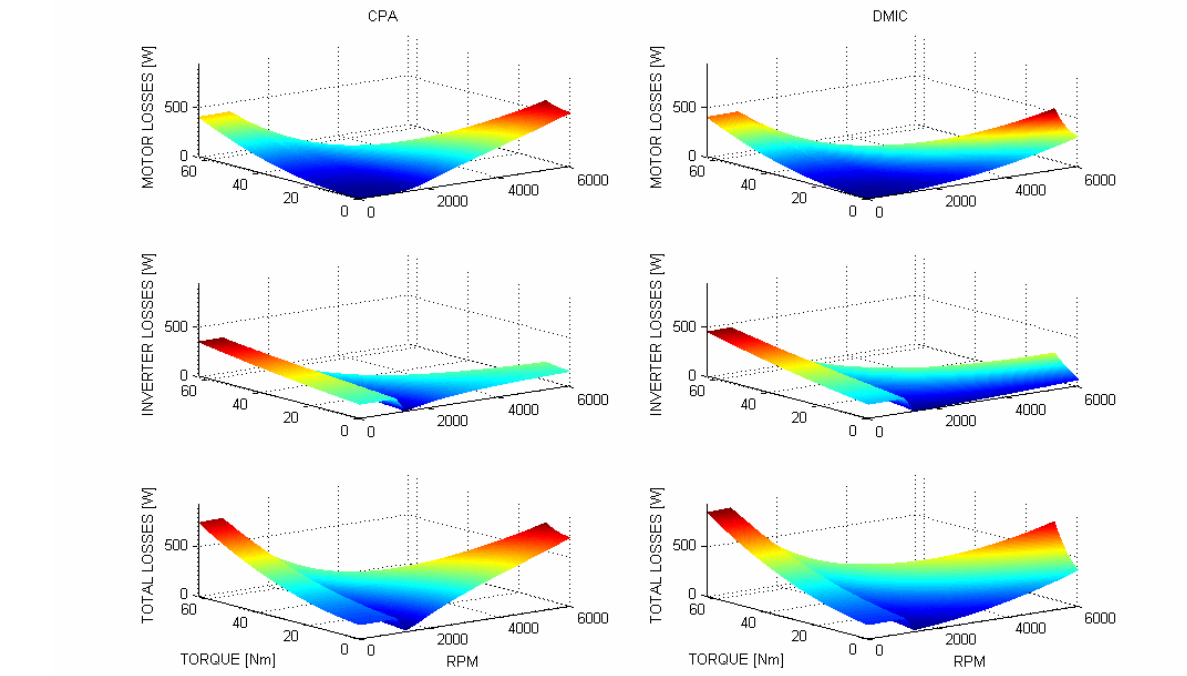
Motor 1 was used to demonstrate the capability of the motor/inverter model for both the CPA and DMIC in Section 4.5. In that earlier comparison, only the full-load and quarter-load conditions were examined. A more thorough assessment from near zero to full load across the full speed range is considered below.

5.3 CPA VERSUS DMIC

Figure 26 contains simulation results over the entire torque-speed envelope for Motor 1 when driven by CPA and by DMIC. In both cases, the dc supply voltage is 151 V which is the minimum necessary to support rated torque at base speed. The thyristor model used with the DMIC case is the "inverter grade" type given in Table 4.

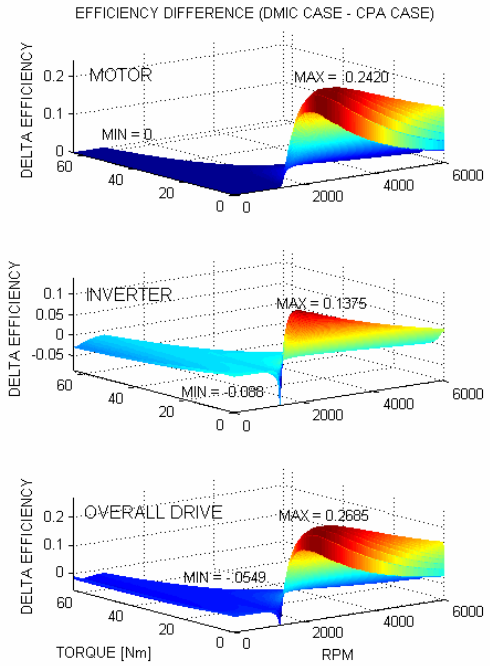


a. Comparison of torque producing, field weakening, and rms current.

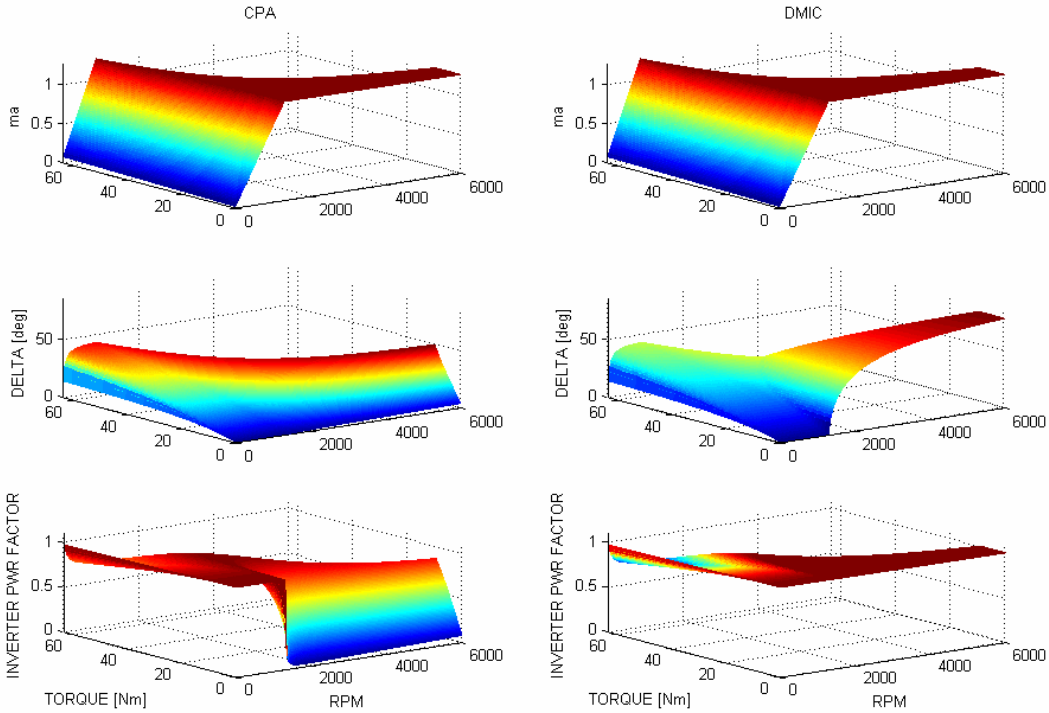


b. Comparison of motor, inverter, and total losses.

Fig. 26. Comparison of Motor 1 driven by CPA and DMIC from a 151 Vdc supply voltage.



c. Motor, inverter, and overall drive efficiency differences between DMIC and CPA.



d. Comparison of amplitude-modulation index, inverter-lead angle, and inverter-power factor.

Fig. 26. Comparison of Motor 1 driven by CPA and DMIC from a 151 Vdc supply voltage (cont'd).

Figure 26(a) shows a key difference in the CPA and DMIC drives. Specifically, the field-weakening component of current in the DMIC drive is proportional to load, as is the rms current. In the CPA drive, the rms current approaches the characteristic current. Since the torque-producing current decreases with speed and is identical for both the CPA and DMIC cases, the field-weakening current tends to the characteristic current at high speed. Because the rms current in the DMIC drive is proportional to load, this drive can maintain high motor efficiency at high speed. This is apparent in Fig. 26(b). At high speed and especially at light load, the motor, inverter, and total losses are lower with the DMIC. At low speed, the conduction losses of the DMIC thyristors result in greater inverter and overall losses. At high speed, the inverter losses of the DMIC are lower, including the thyristors, due to the high-speed current minimization of the DMIC. These effects are also seen in Fig. 26(c) in which the motor, inverter, and overall efficiency of the CPA case is subtracted from the corresponding DMIC case over all torque-speed conditions. The motor is the main beneficiary of the DMIC due to the lower current at high speed; the motor efficiency is higher by as much as 0.2420. The inverter efficiency is lower at and below speed due to the added thyristor conduction losses, but the inverter efficiency is higher during high-speed operation by as much as 0.1375. In the overall efficiency, the DMIC may be as much as 0.0549 lower than the CPA during low-speed operation or as much as 0.2685 higher during the constant-power mode. If the drive spends most of its operating time at or above base speed, then the efficiency of the DMIC may be significantly better than CPA when inverter-grade thyristors are used in the DMIC drive. Figure 26(d) shows that the DMIC maintains unity inverter-power factor during high-speed operation under all load conditions.

The final comparison considered here is the DMIC drive with converter-grade thyristors versus the inverter-grade thyristors. The parameters of both types are given in Table 4.

5.4 INVERTER VERSUS CONVERTER-GRADE THYRISTORS IN THE DMIC

The impact of converter versus inverter-grade thyristors in the DMIC drive is mainly on the inverter losses and efficiency and on the total losses and efficiency. For Motor 1 with 151 Vdc supply, the difference in inverter efficiency and total efficiency is shown in Fig. 27. Below base speed the two cases are nearly identical. Above base speed the reverse-recovery losses of the converter-grade thyristor are larger than those of the inverter grade. Figure 27 shows that the inverter grade may have an efficiency that is at most 0.0768 larger than for the converter grade. The figure also shows that the total efficiency with inverter-grade thyristors is as much as 0.0428 larger than for converter grade. These differences occur at 6000 rpm where the fundamental frequency is 1.5 kHz. Although the thyristor commutation in the DMIC occurs at natural current zeros crossings, it is not clear whether converter-grade thyristors are even capable of such switching rate. The authors have done testing with converter-grade thyristors in a DMIC drive operating at 300 Hz and performance was satisfactory. The motors under investigation have 30 poles, which is the cause of the high fundamental rate. At this point, it is not known whether converter-grade thrysistors would work for high-pole count PMSMs, but their use will result in decreased efficiency.

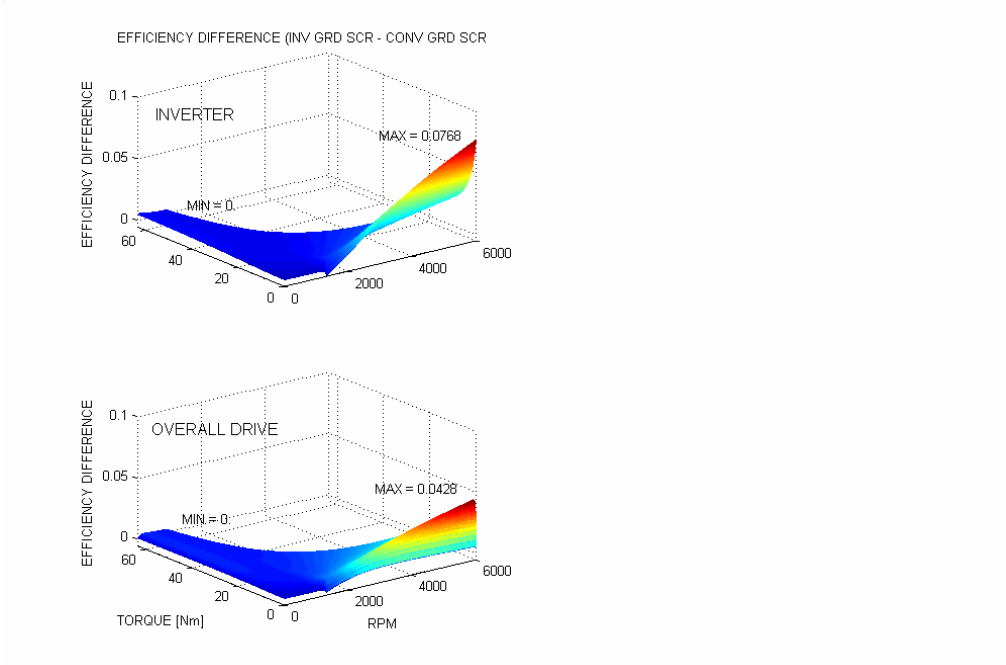


Fig. 27. Efficiency difference between inverter and converter-grade SCRs with Motor 1 driven by DMIC with a 151 Vdc supply voltage.

6. CONCLUSIONS

Regarding control of PMSMs based on this study:

- More inductance and more voltage are better.
- Even with the benefit of both characteristic inductance and high voltage, CPA suffers from low efficiency.
- DMIC solves this problem by assuring that the current used is proportional to load.
- Automobiles spend most of their time at half speed, which is quarter load.
- As gas prices soar and efficiency becomes more important to the consumer, DMIC has the potential to provide the highest efficiency possible.

Regarding validation of methodology used in this study:

- Expressions for the modulation index, m_a, and inverter-lead angle, δ, which were derived based on an algebraic fundamental-frequency model, have been found to be very accurate when used in a detailed time-domain simulation that includes PWM switching.
- Expressions for average and rms currents in diodes, transistors, and thyristors were compared with detailed time-domain simulations above and below base speed.
  - Below base speed where simulations for CPA and DMIC control are the same simulated losses at carrier frequencies of 8505 and 2025 Hz, agreed with theoretical model losses with 1%.
  - Above base speed where separate simulations were necessary for CPA and DMIC
    - Simulated losses for CPA control were within 2.5% of the theoretical model for transistor average, rms current, and diode average currents. Simulated loss of the diode rms current, which was not quite as good, was within 8% of the theoretical model.
    - Simulated losses for DMIC control were within 1% of the theoretical model for the average transistor, by-pass diode, and thyristor currents. Simulated loss of the transistor and thyristor rms currents, which were not quite as good, were within 9% of the theoretical model.
- Since diode losses are generally 1/2 transistor losses and conduction losses of diodes are weighted more by forward voltage drop and average current than by diode resistance (rms current losses), the simplified theoretical model is sufficiently accurate for this study.

Regarding operation of PMSMs under CPA control:

- Characteristic motor current, which permits operation at high CPSR, depends solely on machine parameters E_b, Ω_b, and L and is independent of motor load and dc supply voltage. This lowers its efficiency at partial load conditions. Providing voltage higher than necessary to support rated torque at base speed cannot reduce the current at high speed.
- It is advantageous to have the inductance higher than "optimal" because it enables the motor to develop the required power with lower current and attendant efficiency increase.
- Even more voltage than the minimum required for injecting rated current at base speed can be beneficial because of lower current and attendant efficiency increase.
- The speed at which minimum current, n_{min}, occurs depends linearly on developed power and inversely on the maximum fundamental-inverter voltage. n_{min}, is a unique speed which varies with voltage leaving room for optimization. If a motor spends a substantial amount of time at half speed, it could be desirable to choose a dc supply voltage which causes the minimum current at half speed. This would involve using a dc supply larger than the minimum and using control to restrain the torque envelope.

- Control of the voltage-lead angle at high speeds allows a PMSM to operate at constant power, but it doesn't assure operation within rated current. Inductance is the critical factor that assures operation within rated current.
- The limiting current at high speed is mostly for field weakening and, therefore, produces little torque.
- At full load, Motor 1 behaves as well with CPA control as with DMIC control.

Regarding operation of PMSMs under DMIC control:

- Higher inductance results in reduced current at only one speed and power level under CPA control, whereas DMIC control minimizes current at all power levels and speeds, $n > 2$.
- DMIC motor current is proportional to load at high speed, which leads to decreased current and attendant increased efficiency at partial load.
- Although originally for motors with low inductance, DMIC has potential for significant loss reduction for PMSMs with large inductance.
- DMIC control maintains an inverter-power factor of 1 for all speeds greater than n_{min}, the speed at which minimum current occurs. Under CPA control, n_{min} is a single speed at which a PMSM operates at an inverter-power factor of 1. At all speeds above $n_{min,}$ the CPA power-factor leads.
- With DMIC high speed, current is inversely proportional to supply voltage so that extra supply voltage can lead to improved efficiency.
- Depending on the application, particularly the speed/loss profile, loss reduction may more than compensate for the losses introduced by the addition of the SCRs required by DMIC.
- At half speed (quarter load), Motor 1 under DMIC delivers 7.5% percentage points more power at 3000 rpm and 8.6% more power at 6000 rpm than Motor 1 under CPA control.

Regarding the grade of SCR that should be used:

- Increasing reverse-recovery losses of thyristors, which increases with speed, is a problem that can be reduced with inverter-grade components at increased cost; however, cost and losses may be offset by efficiency enhancement.
- The question about converter-grade SCRs being able to sustain operation in the FreedomCAR and Vehicle Technologies application at a fundamental switching rate of 1.5 kHz at top speed of 6000 rpm must be answered in the laboratory by experimentation.

7. REFERENCES

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2. A. K. Adnanes, "Torque Analysis of Permanent Magnet Synchronous Motors," pp. 695–701 in the *23rd Annual IEEE Power Electronics Specialists Conference Record*, June 29–July 3, 1992.
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6. A. M. El-Refaie and T. M. Jahns, "Optimal Flux Weakening in Surface PM Machines Using Concentrated Windings," pp. 1038–1047 in *Conference Recl IEEE Industry Applications Society Annual Meeting,* **2**, Seattle, Washington, October 2004.
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8. J. S. Lawler, J. M. Bailey, and J. McKeever, "Minimum Current Magnitude Control of Surface PM Synchronous Machines during Constant Power Operation," pp. 53–56 in *IEEE Power Electronics Letters*, **3**(2), June 2005.
9. A. M. El-Refaie, T. M. Jahns, P. J. McCleer, and J. W. McKeever, "Experimental Verification of Optimal Flux Weakening in Surface PM Machines Using Concentrated Windings," *Conf. Rec. IEEE Industry Applications Society Annual Meeting*, Hong Kong, October 2–6, 2005.
10. B. Ozpineci, "System Impact of Silicon Carbide Power Electronics on Hybrid Electric Vehicle Applications," Ph. D. dissertation, University of Tennessee, Knoxville, Tennessee, August 2002.
11. M. H. Bierhoff and F. W. Fuchs, "Semiconductor Losses in Voltage-Source and Current Source IGBT Converters Based on Analytical Derivation," pp. 2836–2842 in *Proceedings of IEEE 35th Power Electronics Specialist Conference*, **4**, Aachen, Germany, June 2004.

APPENDIX A.1: 600 V, 75 A, IGBT MODULE – FAIRCHILE FMG1G75US60H

FAIRCHILD SEMICONDUCTOR®

IGBT

FMG1G75US60H

FMG1G75US60H

Molding Type Module

General Description

Fairchild's Insulated Gate Bipolar Transistor (IGBT) power modules provide low conduction and switching losses as well as short circuit ruggedness. They are designed for applications such as motor control, uninterrupted power supplies (UPS) and general inverters where short circuit ruggedness is a required feature.

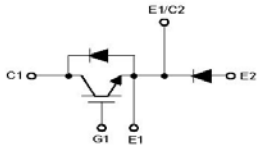
Features

- UL Certified No. E209204
- Short Circuit rated 10us @ T_C = 100°C, V_{GE} = 15V
- High Speed Switching
- Low Saturation Voltage : $V_{CE(sat)}$ = 2.2 V @ I_C = 75A
- High Input Impedance
- Fast & Soft Anti-Parallel FWD

Application

- AC & DC Motor Controls
- General Purpose Inverters
- Robotics
- Servo Controls
- UPS

Package Code : 7PM-GA



Internal Circuit Diagram

Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Description		FMG1G75US60H	Units
V_{CES}	Collector-Emitter Voltage		600	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Curent	@ T_C = 25°C	75	A
$I_{CM\ (1)}$	Pulsed Collector Current		150	A
I_F	Diode Continuous Forward Current	@ T_C = 100°C	75	A
I_{FM}	Diode Maximum Forward Current		150	A
T_{SC}	Short Circuit Withstand Time	@ T_C = 100°C	10	us
P_D	Maximum Power Dissipation	@ T_C = 25°C	310	W
T_J	Operating Junction Temperature		-40 to +150	°C
T_{stg}	Storage Temperature Range		-40 to +125	°C
V_{iso}	Isolation Voltage	@ AC 1minute	2500	V
Mounting Torque	Power Terminals Screw : M5		2.0	N.m
	Mounting Screw : M5		2.0	N.m

Notes :
(1) Repetitive rating : Pulse width limited by max. junction temperature

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FMG1G75US60H Rev. A

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EcoSPARK™	I²C™	PowerTrench ®	SuperSOT™-6	
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EnSigna™	LittleFET™	QS™	SyncFET™	
FACT™	MicroFET™	QT Optoelectronics™	TinyLogic™	
FACT Quiet Series™	MicroPak™	Quiet Series™	TruTranslation™	

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As used herein:

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. H5

Electrical Characteristics of IGBT T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{CES}	Collector-Emitter Breakdown Voltage	V_{GE} = 0V, I_C = 250uA	600	--	--	V
$\Delta B_{VCES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	V_{GE} = 0V, I_C = 1mA	--	0.6	--	V/°C
I_{CES}	Collector Cut-Off Current	$V_{CE} = V_{CES}$, V_{GE} = 0V	--	--	250	uA
I_{GES}	G-E Leakage Current	$V_{GE} = V_{GES}$, V_{CE} = 0V	--	--	±100	nA
On Characteristics						
$V_{GE(th)}$	G-E Threshold Voltage	V_{GE} = 0V, I_C = 75mA	5.0	6.0	8.5	V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage	I_C = 75A, V_{GE} = 15V	--	2.2	2.8	V
Dynamic Characteristics						
C_{ies}	Input Capacitance	V_{CE} = 30V, V_{GE} = 0V, f = 1MHz	--	7056	--	pF
C_{oes}	Output Capacitance		--	672	--	pF
C_{res}	Reverse Transfer Capacitance		--	180	--	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 300 V, I_C = 75A, R_G = 3.3Ω, V_{GE} = 15V Inductive Load, T_C = 25°C	--	20	--	ns
t_r	Rise Time		--	40	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	--	ns
t_f	Fall Time		--	110	200	ns
E_{on}	Turn-On Switching Loss		--	1.4	--	mJ
E_{off}	Turn-Off Switching Loss		--	1.7	--	mJ
E_{ts}	Total Switching Loss		--	3.1	--	mJ
$t_{d(on)}$	Turn-On Delay Time	V_{CC} = 300 V, I_C = 75A, R_G = 3.3Ω, V_{GE} = 15V Inductive Load, T_C = 125°C	--	20	--	ns
t_r	Rise Time		--	50	--	ns
$t_{d(off)}$	Turn-Off Delay Time		--	80	--	ns
t_f	Fall Time		--	250	--	ns
E_{on}	Turn-On Switching Loss		--	1.6	--	mJ
E_{off}	Turn-Off Switching Loss		--	3.0	--	mJ
E_{ts}	Total Switching Loss		--	4.6	--	mJ
T_{sc}	Short Circuit Withstand Time	V_{CC} = 300 V, V_{GE} = 15V @ T_C = 100°C	10	--	--	us
Q_g	Total Gate Charge	V_{CE} = 300 V, I_C = 75A, V_{GE} = 15V	--	310	350	nC
Q_{ge}	Gate-Emitter Charge		--	62	--	nC
Q_{gc}	Gate-Collector Charge		--	130	--	nC

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Electrical Characteristics of DIODE T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
V_{FM}	Diode Forward Voltage	I_F = 75A	T_C = 25°C	--	1.9	2.8	V
			T_C = 100°C	--	1.8	--	
t_{rr}	Diode Reverse Recovery Time	I_F = 75A di / dt = 150 A/us	T_C = 25°C	--	90	130	ns
			T_C = 100°C	--	130	--	
I_{rr}	Diode Peak Reverse Recovery Current		T_C = 25°C	--	7	9	A
			T_C = 100°C	--	10	--	
Q_{rr}	Diode Reverse Recovery Charge		T_C = 25°C	--	315	590	nC
			T_C = 100°C	--	650	--	

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case (IGBT Part, per 1/2 Module)	--	0.4	°C/W
$R_{\theta JC}$	Junction-to-Case (DIODE Part, per 1/2 Module)	--	0.9	°C/W
$R_{\theta CS}$	Case-to-Sink (Conductive grease applied)	0.05	--	°C/W
Weight	Weight of Module	--	190	g

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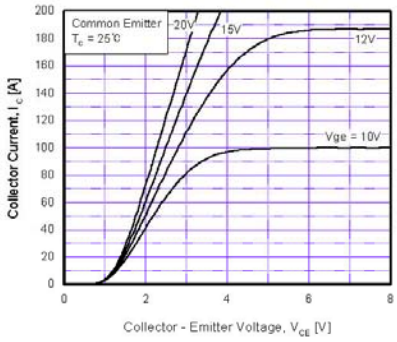

Fig 1. Typical Output Characteristics

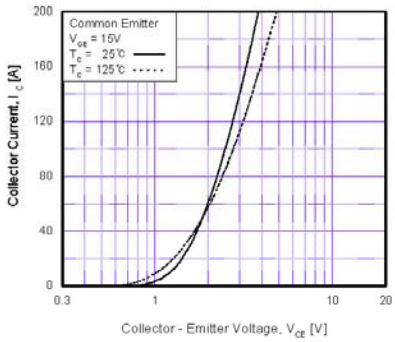

Fig 2. Typical Saturation Voltage Characteristics

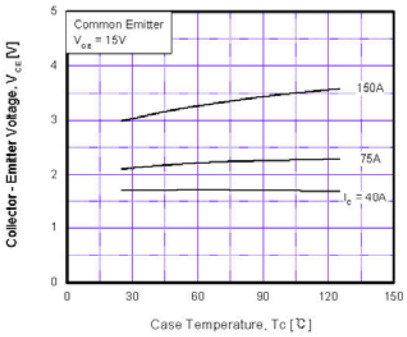

Fig 3. Saturation Voltage vs. Case Temperature at Variant Current Level

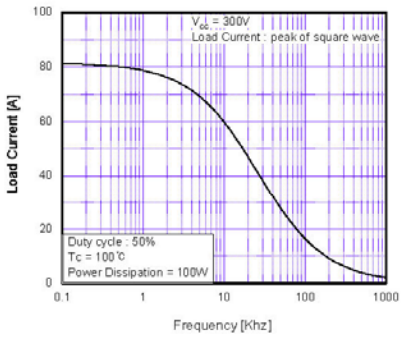

Fig 4. Load Current vs. Frequency

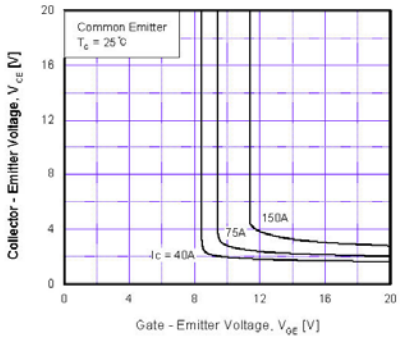

Fig 5. Saturation Voltage vs. V_{GE}

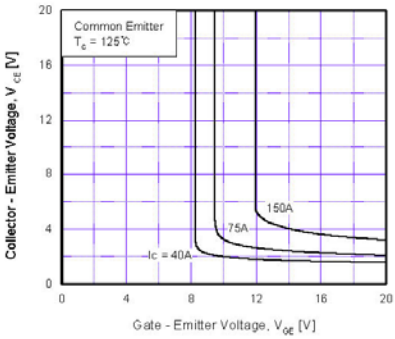

Fig 6. Saturation Voltage vs. V_{GE}

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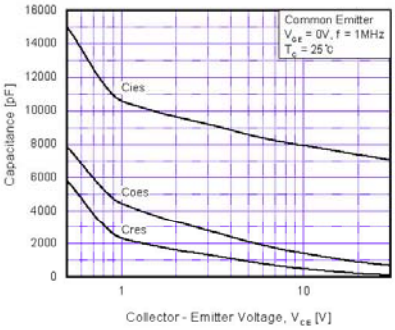

Fig 7. Capacitance Characteristics

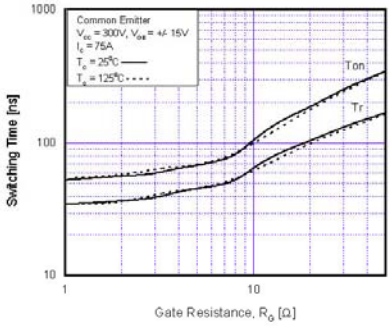

Fig 8. Turn-On Characteristics vs. Gate Resistance

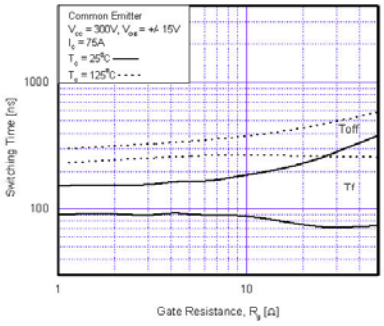

Fig 9. Turn-Off Characteristics vs. Gate Resistance

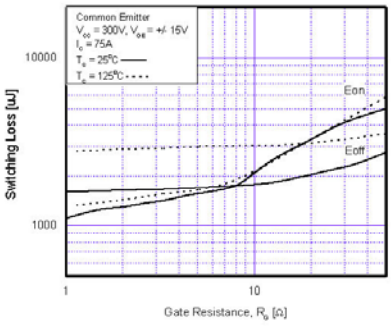

Fig 10. Switching Loss vs. Gate Resistance

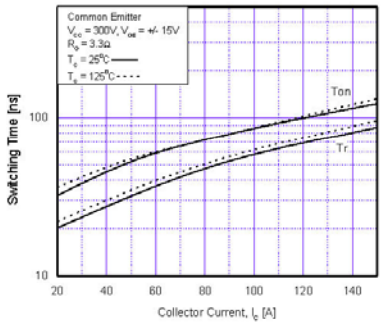

Fig 11. Turn-On Characteristics vs. Collector Current

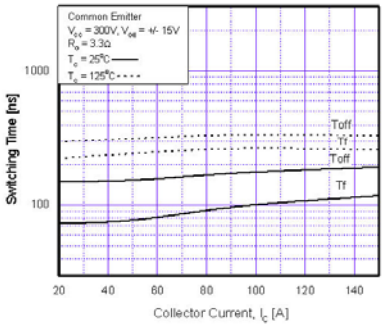

Fig 12. Turn-Off Characteristics vs. Collector Current

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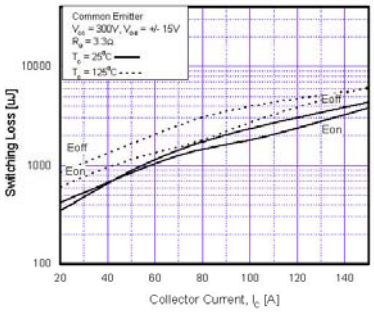

Fig 13. Switching Loss vs. Collector Current

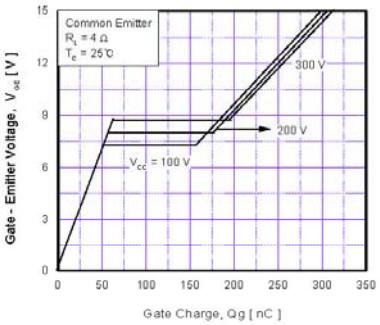

Fig 14. Gate Charge Characteristics

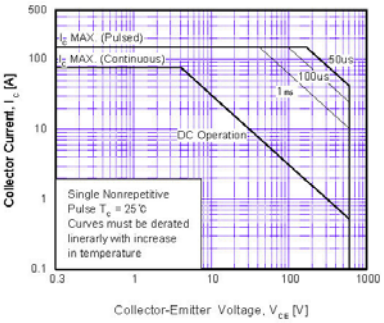

Fig 15. SOA Characteristics

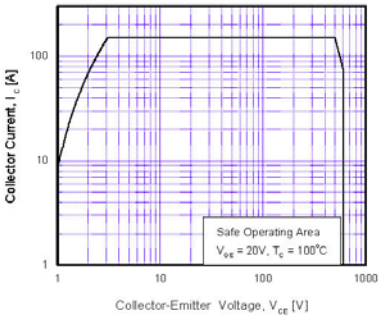

Fig 16. Turn-Off SOA Characteristics

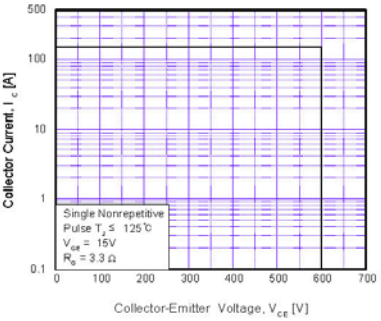

Fig 17. RBSOA Characteristics

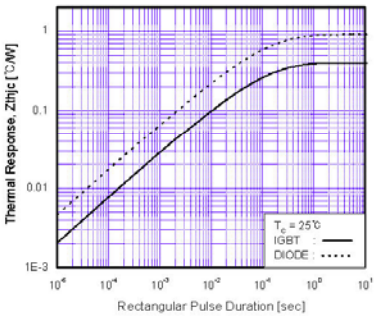

Fig 18. Transient Thermal Impedance

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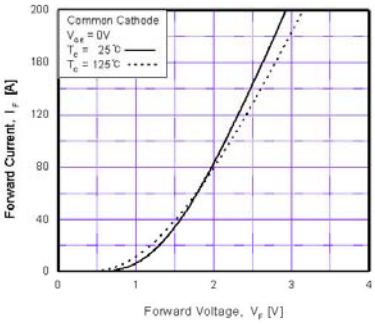

Fig 19. Forward Characteristics

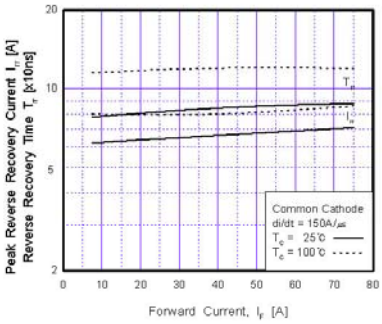

Fig 20. Reverse Recovery Characteristics

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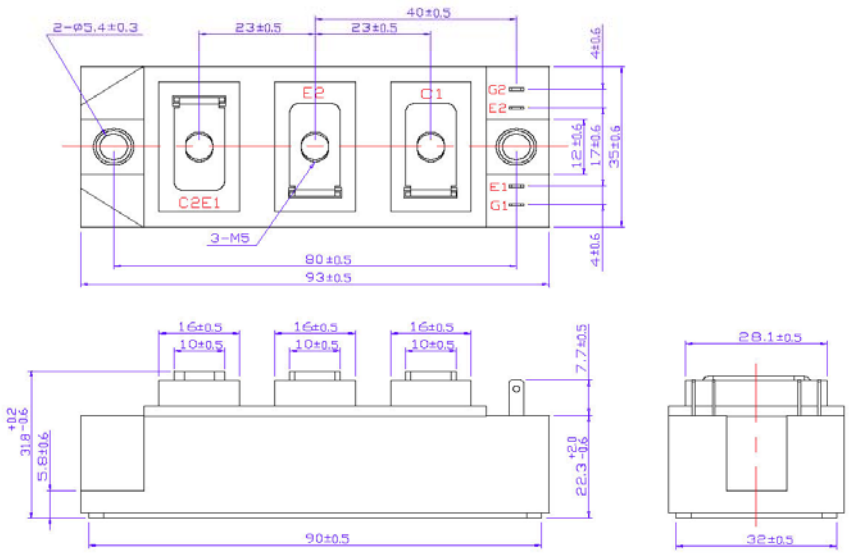
Package Dimension

7PM-GA



Dimensions in Millimeters

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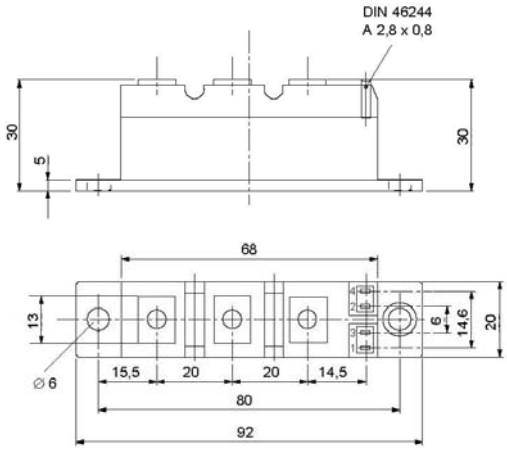
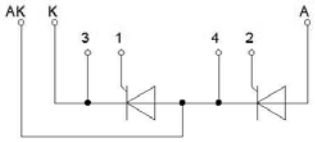
APPENDIX A.2: 800 V, 45 A, INVERTER-GRADE THYRISTOR MODULE – EUPEC TT46F08

eupec

European Power-
Semiconductor and
Electronics Company

Marketing Information
TT 46 F 08...13





MA2-BE, 24. May 1994

TT 46 F 08...13

Elektrische Eigenschaften	Electrical properties					
Höchstzulässige Werte	*Maximum rated values*					
Periodische Vorwärts- und Rückwärts-Spitzensperrspann.	repetitive peak forward off-state and reverse voltages	$t_{vj} = - t_{c\,op}$ ...$t_{vj\,max}$	V_{DRM}, V_{RRM}	800, 1000, 1100 1200, 1300		V [1]
Vorwärts-Stoßspitzensperrspannung	non-repetitive peak forward off-state voltage	$t_{vj} = - t_{c\,op}$ ...$t_{vj\,max}$	V_{DSM}	800, 1000, 1100 1200, 1300		V
Rückwärts-Stoßspitzensperrspannung	non-repetitive peak reverse voltage	t_{vj} = +25°C...$t_{vj\,max}$	V_{RSM}	900, 1100, 1200 1300, 1400		V
Durchlaßstrom-Grenzeffektivwert	RMS on-state current		I_{TRMSM}		120	A
Dauergrenzstrom	average on-state current	t_c = 85°C	I_{TAVM}		45	A
		t_c = 48°C			76	A
Stoßstrom-Grenzwert	surge current	t_{vj} = 25°C, t_p = 10 ms	I_{TSM}		1300	A
		$t_{vj} = t_{vj\,max}$, t_p = 10 ms			1150	A
Grenzlastintegral	I^2t-value	t_{vj} = 25°C, t_p = 10 ms	I^2t		8450	A^2s
		$t_{vj} = t_{vj\,max}$, t_p = 10 ms			6600	A^2s
Kritische Stromsteilheit	critical rate of rise of on-state current	DIN IEC 747-6, f = 50 Hz, v_L = 10 V i_{GM} = 0,75 A, di_G/dt = 0,75 A/µs	$(di_T/dt)_{cr}$		120	A/µs
Kritische Spannungssteilheit	critical rate of rise of off-state voltage	$t_{vj} = t_{vj\,max}$, v_D = 0,67 V_{DRM}	$(dv_D/dt)_{cr}$	2)	3)	V/µs
		6.Kennbuchstabe/6th letter B		50	50	
		6.Kennbuchstabe/6th letter C		500	500	V/µs
		6.Kennbuchstabe/6th letter L		500	50	V/µs
		6.Kennbuchstabe/6th letter M		1000	500	V/µs
Charakteristische Werte	*Characteristic values*					
Durchlaßspannung	on-state voltage	$t_{vj} = t_{vj\,max}$, i_T = 230 A	v_T		max. 2,20	V
Schleusenspannung	threshold voltage	$t_{vj} = t_{vj\,max}$	$V_{T(TO)}$		1,30	V
Ersatzwiderstand	slope resistance	$t_{vj} = t_{vj\,max}$	r_T		3,4	mΩ
Zündstrom	gate trigger current	t_{vj} = 25 °C, v_D = 12 V	I_{GT}		max. 150	mA
Zündspannung	gate trigger voltage	t_{vj} = 25 °C, v_D = 12 V	V_{GT}		max. 1,4	V
Nicht zündender Steuerstrom	gate non-trigger current	$t_{vj} = t_{vj\,max}$, v_D = 12 V	I_{GD}		max. 5	mA
		$t_{vj} = t_{vj\,max}$, v_D = 0,5 V_{DRM}			max. 2,5	mA
Nicht zündende Steuerspann.	gate non-trigger voltage	$t_{vj} = t_{vj\,max}$, v_D = 0,5 V_{DRM}	V_{GD}		max. 0,2	V
Haltestrom	holding current	t_{vj} = 25 °C, v_D = 12 V, R_A = 5 Ω	I_H		max. 250	mA
Einraststrom	latching current	t_{vj} = 25 °C,v_D = 12 V, R_{GK} > = 20 Ω i_{GM} = 0,75 A, di_G/dt = 0,75 A/µs, t_g = 20	I_L		max. 1000	mA
Vorwärts- und Rückwärts-Sperrstrom	forward off-state and reverse currents	$t_{vj} = t_{vj\,max}$ $v_D = V_{DRM}$, $v_R = V_{RRM}$	i_D, i_R		max. 25	mA
Zündverzug	gate controlled delay time	DIN IEC 747-6, t_{vj} = 25°C i_{GM} = 0,75 A, di_G/dt = 0,75 A/µs	t_{gd}		max. 1,4	µs
Freiwerdezeit	circuit commutated turn-off time	$t_{vj} = t_{vj\,max}$, $i_{TM} = I_{TAVM}$ v_{RM} = 100 V, v_{DM} = 0,67 V_{DRM} $-di_T/dt$ = 20 A/µs	t_q			
		5.Kennbuchstabe/5th letter C			max. 12	µs
		5.Kennbuchstabe/5th letter D			max. 15	µs
		5.Kennbuchstabe/5th letter E			max. 20	µs
		5.Kennbuchstabe/5th letter F			max. 25	µs
Isolations-Prüfspannung	insulation test voltage	RMS, f = 50 Hz, 1 min.	V_{ISOL}		2,5	kV
Thermische Eigenschaften	Thermal properties					
Innerer Wärmewiderstand	thermal resistance, junction to case	pro Modul/per module,Θ =180° sin	R_{thJC}		max. 0,26	°C/W
		pro Zweig/per arm,Θ =180° sin			max. 0,52	°C/W
		pro Modul/per module, DC			max. 0,25	°C/W
		pro Zweig/per arm, DC			max. 0,50	°C/W
Übergangs-Wärmewiderstand	thermal resistance, case to heatsink	pro Modul/per module	R_{thCK}		max. 0,08	°C/W
		pro Zweig/per arm			max. 0,16	°C/W
Höchstzul.Sperrschichttemp.	max. junction temperature		$t_{vj\,max}$		125	°C
Betriebstemperatur	operating temperature		$t_{c\,op}$		-40...+125	°C
Lagertemperatur	storage temperature		t_{stg}		-40...+130	°C
Mechanische Eigenschaften	Mechanical properties					
Innere Isolation	internal insulation				AlN	
Anzugsdrehmoment für mech. Befestigung	mounting torque	Toleranz/tolerance +/- 15%	M1		4	Nm
Anzugsdrehmoment für elektrische Anschlüsse	terminal connection torque	Toleranz/tolerance +5%/-10%	M2		4	Nm
Gewicht	weight		G		typ. 180	g
Kriechstrecke	creepage distance				12,5	mm
Schwingfestigkeit	vibration resistance	f = 50 Hz			50	m/s²

[1] 1300V auf Anfrage / 1300V on demand
[2] Werte nach DIN IEC 747-6 (ohne vorrausgehende Kommutierung). / Values to DIN IEC 747-6 (without prior commutation)
[3] Unmittelbar nach der Freiwerdezeit, vgl. Meßbedingungen für t_q. / Immediatly after circuit commutated turn-off time, see parameters t_q.

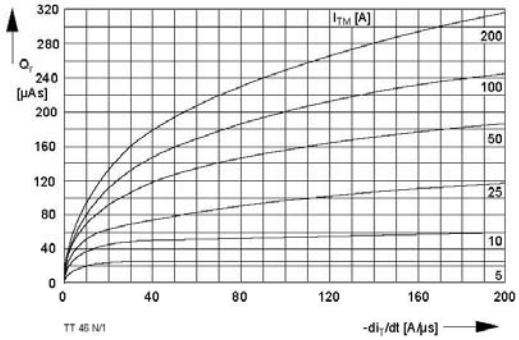


Bild / Fig. 1
Sperrverzögerungsladung / Recovered Charge Qr = f(di/dt)
$t_{vj} = t_{vj\,max}$, $v_R = 0{,}5\ V_{RRM}$, $v_{RM} = 0{,}8\ V_{RRM}$
Parameter: Durchlaßstrom / on-state current I_{TM}

Analytische Elemente des transienten Wärmewiderstandes Z_{thJC} pro Zweig für DC
Analytical elements of transient thermal impedance Z_{thJC} per arm for DC

Pos. n	1	2	3	4	5	6	7
R_{thn} [°C/W]	0,0218	0,0426	0,1886	0,247			
τ_n [s]	0,000945	0,01	0,31	1,762			

Analytische Funktion / Analytical function:

$$Z_{thJC} = \sum_{n=1}^{n_{max}} R_{thn}\,(1-e^{-\frac{t}{\tau_n}})$$

APPENDIX A.3: 1400 V, 61 A, CONVERTER-GRADE THRISTOR MODULE – EUPEC TT61N

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	

TT61N	TD61N	DT61N
TT61N...-K	TD61N...-A	DT61N...-K

Elektrische Eigenschaften / Electrical properties

Höchstzulässige Werte / Maximum rated values

Periodische Vorwärts- und Rückwärts-Spitzensperrspannung repetitive peak forward off-state and reverse voltages	T_{vj} = -40°C... $T_{vj\,max}$	V_{DRM},V_{RRM}	1200 1600	1400	V V
Vorwärts-Stoßspitzensperrspannung non-repetitive peak forward off-state voltage	T_{vj} = -40°C... $T_{vj\,max}$	V_{DSM}	1200 1600	1400	V V
Rückwärts-Stoßspitzensperrspannung non-repetitive peak reverse voltage	T_{vj} = +25°C... $T_{vj\,max}$	V_{RSM}	1300 1700	1500	V V
Durchlaßstrom-Grenzeffektivwert maximum RMS on-state current		I_{TRMSM}		120	A
Dauergrenzstrom average on-state current	T_C = 85°C T_C = 76°c	I_{TAVM}		60 76	A A
Stoßstrom-Grenzwert surge current	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I_{TSM}		1550 1400	A A
Grenzlastintegral I^2t-value	T_{vj} = 25 °C, t_P = 10 ms T_{vj} = $T_{vj\,max}$, t_P = 10 ms	I^2t		12000 9800	A^2s A^2s
Kritische Stromsteilheit critical rate of rise of on-state current	DIN IEC 747-6 f = 50 Hz, i_{GM} = 1 A, di_G/dt = 1 A/µs	$(di_T/dt)_{cr}$		150	A/µs
Kritische Spannungssteilheit critical rate of rise of off-state voltage	T_{vj} = $T_{vj\,max}$, v_D = 0,67 V_{DRM} 6.Kennbuchstabe / 6th letter F	$(dv_D/dt)_{cr}$		1000	V/µs

Charakteristische Werte / Characteristic values

Durchlaßspannung on-state voltage	T_{vj} = $T_{vj\,max}$, i_T = 300 A	v_T	max.	1,9	V
Schleusenspannung threshold voltage	T_{vj} = $T_{vj\,max}$	$V_{(TO)}$		0,8	V
Ersatzwiderstand slope resistance	T_{vj} = $T_{vj\,max}$	r_T		3,4	mΩ
Zündstrom gate trigger current	T_{vj} = 25°C, v_D = 6 V	I_{GT}	max.	120	mA
Zündspannung gate trigger voltage	T_{vj} = 25°C, v_D = 6 V	V_{GT}	max.	1,4	V
Nicht zündender Steuerstrom gate non-trigger current	T_{vj} = $T_{vj\,max}$, v_D = 6 V T_{vj} = $T_{vj\,max}$, v_D = 0,5 V_{DRM}	I_{GD}	max. max.	5,0 2,5	mA mA
Nicht zündende Steuerspannung gate non-trigger voltage	T_{vj} = $T_{vj\,max}$, v_D = 0,5 V_{DRM}	V_{GD}	max.	0,2	V
Haltestrom holding current	T_{vj} = 25°C, v_D = 6 V, R_A = 5 Ω	I_H	max.	200	mA
Einraststrom latching current	T_{vj} = 25°C, v_D = 6 V, R_{GK} ≥ 10 Ω i_{GM} = 1 A, di_G/dt = 1 A/µs, t_g = 20 µs	I_L	max.	620	mA
Vorwärts- und Rückwärts-Sperrstrom forward off-state and reverse current	T_{vj} = $T_{vj\,max}$ v_D = V_{DRM}, v_R = V_{RRM}	i_D, i_R	max.	20	mA
Zündverzug gate controlled delay time	DIN IEC 747-6 T_{vj} = 25 °C,i_{GM} = 1 A, di_G/dt = 1 A/µs	t_{gd}	max.	3	µs

prepared by:	C.Drilling		date of publication:	09.07.02
approved by:	J. Novotny		revision:	3

BIP AC/ 16.05.2002; Drilling	A 05/02	Seite/page	1/2

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	

Elektrische Eigenschaften / Electrical properties
Charakteristische Werte / Characteristic values

Freiwerdezeit circuit commutated turn-off time	$T_{vj} = T_{vj\,max}$, $i_{TM} = I_{TAVM}$ v_{RM} = 100 V, v_{DM} = 0,67 V_{DRM} dv_D/dt = 20 V/µs, $-di_T/dt$ = 10 A/µs 5.Kennbuchstabe / 5th letter O	t_q	typ.	120	µs
Isolations-Prüfspannung insulation test voltage	RMS, f = 50 Hz, t = 1 min RMS, f = 50 Hz, t = 1 sec	V_{ISOL}		2,5 3,0	kV kV

Thermische Eigenschaften / Thermal properties

Innerer Wärmewiderstand thermal resistance, junction to case	pro Modul / per Module, Θ = 180° sin pro Zweig / per arm, Θ = 180° sin pro Modul / per Module, DC pro Zweig / per arm, DC	R_{thJC}	max. max. max. max.	0,26 0,52 0,25 0,50	°C/W °C/W °C/W °C/W
Übergangs-Wärmewiderstand thermal resistance, case to heatsink	pro Modul / per Module pro Zweig / per arm	R_{thCH}	max. max.	0,08 0,16	°C/W °C/W
Höchstzulässige Sperrschichttemperatur maximum junction temperature		$T_{vj\,max}$		125	°C
Betriebstemperatur operating temperature		$T_{c\,op}$		-40...+125	°C
Lagertemperatur storage temperature		T_{stg}		-40...+130	°C

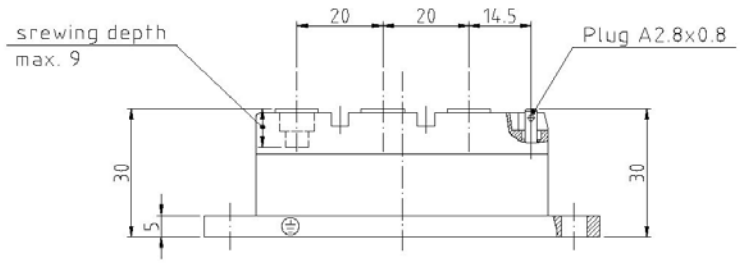
Mechanische Eigenschaften / Mechanical properties

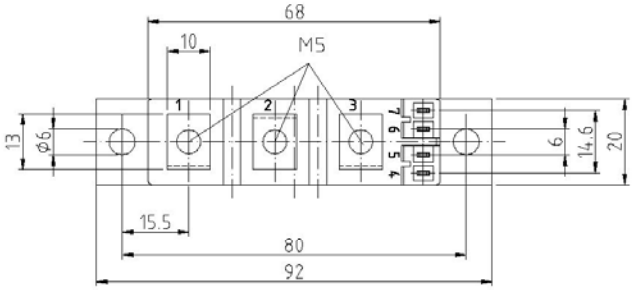
Gehäuse, siehe Anlage case, see annex				Seite 3 page 3	
Si-Element mit Druckkontakt Si-pellet with pressure contact					
Innere Isolation internal insulation				AlN	
Anzugsdrehmoment für mechanische Anschlüsse mounting torque	Toleranz / Tolerance ± 15%	M1		4	Nm
Anzugsdrehmoment für elektrische Anschlüsse terminal connection torque	Toleranz / Tolerance ± 10%	M2		4	Nm
Steueranschlüsse control terminals	DIN 46 244			A 2,8 x 0,8	
Gewicht weight		G	typ.	160	g
Kriechstrecke creepage distance				12,5	mm
Schwingfestigkeit vibration resistance	f = 50 Hz			50	m/s²
UL-gelistet UL listed	file-No.			E 83336	

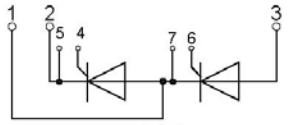
Mit diesem Datenblatt werden Halbleiterbauelemente spezifiziert, jedoch keine Eigenschaften zugesichert. Es gilt in Verbindung mit den zugehörigen technischen Erläuterungen.

This data sheet specifies semiconductor devices, but promises no characteristics. It is valid in combination with the belonging technical notes.

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	







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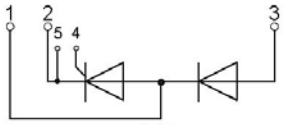

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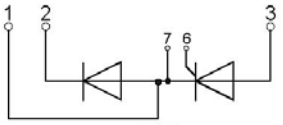

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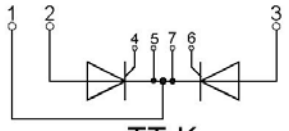

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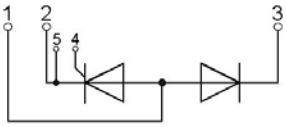

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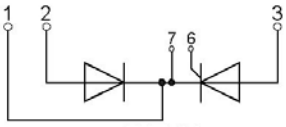


DT-K

BIP AC/ 16.05.2002; Drilling	A 05/02	Seite/page	3/2

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	

Analytische Elemente des transienten Wärmewiderstandes Z_{thJC} für DC
Analytical elements of transient thermal impedance Z_{thJC} for DC

Pos. n	1	2	3	4	5	6	7
R_{thn} [°C/W]	0,0218	0,0426	0,1886	0,2470			
τ_n [s]	0,000945	0,01	0,31	1,762			

Analytische Funktion / Analytical function: $$Z_{thJC} = \sum_{n=1}^{n_{max}} R_{thn} \left(1 - e^{\frac{-t}{\tau_n}}\right)$$

Natürliche Kühlung / Natural cooling
3 Module pro Kühler / 3 modules per heatsink
Kühler / Heatsink type: KM14 (50W)

Analytische Elemente des transienten Wärmewiderstandes Z_{thCA}
Analytical elements of transient thermal impedance Z_{thCA}

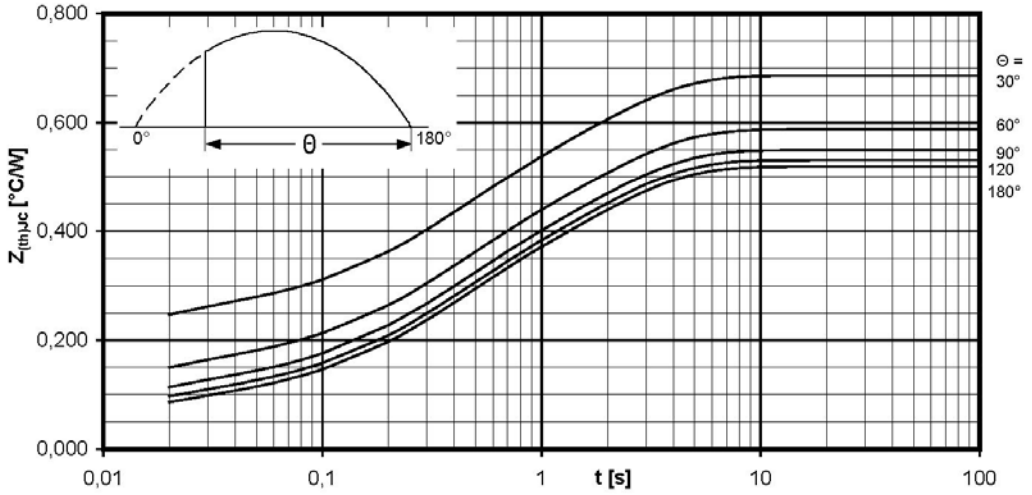
Pos. n	1	2	3	4	5	6	7
R_{thn} [°C/W]	0,007	0,191	0,142	2,12			
τ_n [s]	0,858	6,07	47,7	917			

Verstärkte Kühlung / Forced cooling
3 Module pro Kühler / 3 modules per heatsink
Kühler / Heatsink type: KM14 (Papst 4650N)

Analytische Elemente des transienten Wärmewiderstandes Z_{thCA}
Analytical elements of transient thermal impedance Z_{thCA}

Pos. n	1	2	3	4	5	6	7
R_{thn} [°C/W]	0,007	0,191	0,142	0,570			
τ_n [s]	0,858	6,07	47,7	247			

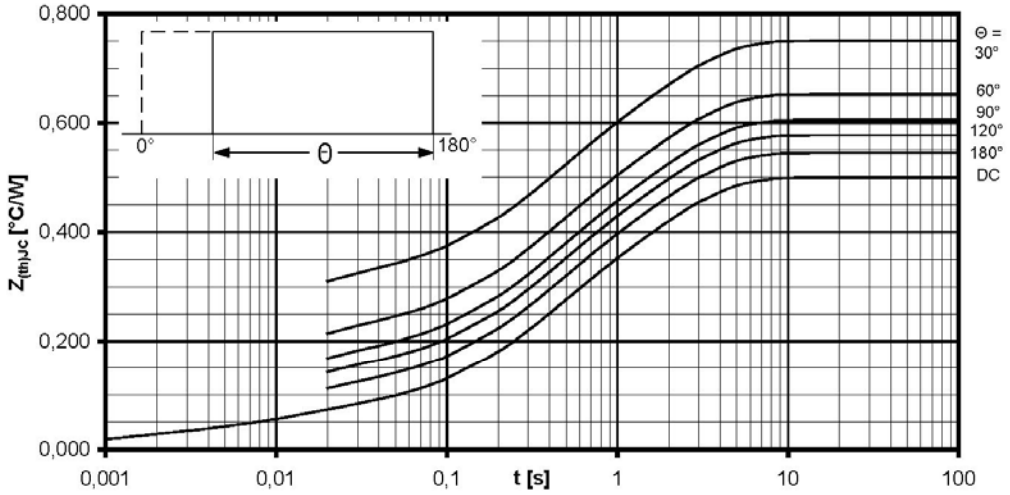
Analytische Funktion / Analytical function: $$Z_{thCA} = \sum_{n=1}^{n_{max}} R_{thn} \left(1 - e^{\frac{-t}{\tau_n}}\right)$$



Transienter innerer Wärmewiderstand je Zweig / Transient thermal impedance per arm Z_{thJC} = f(t)

Sinusförmiger Strom / Sinusoidal current

Parameter: Stromflußwinkel Θ / Current conduction angle Θ

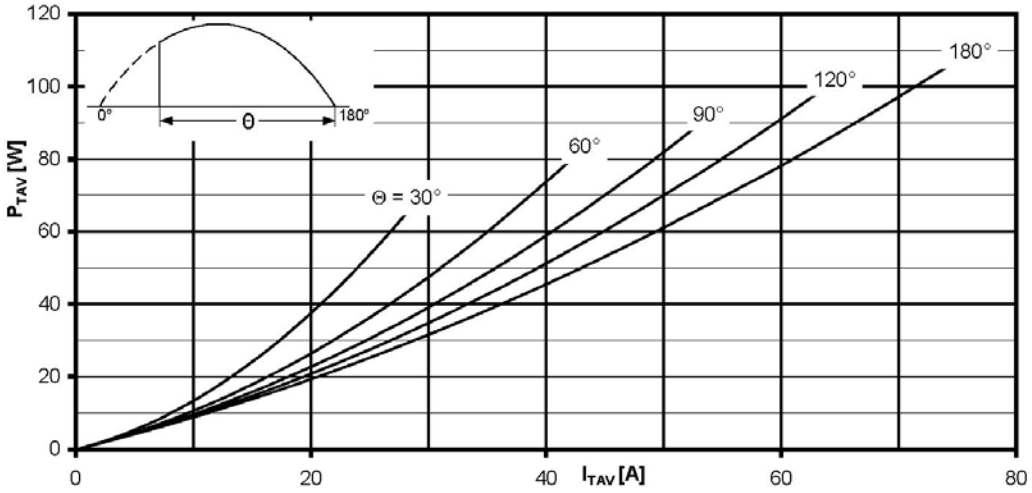


Transienter innerer Wärmewiderstand je Zweig / Transient thermal impedance per arm Z_{thJC} = f(t)

Rechteckförmiger Strom / Rectangular current

Parameter: Stromflußwinkel Θ / Current conduction angle Θ

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	

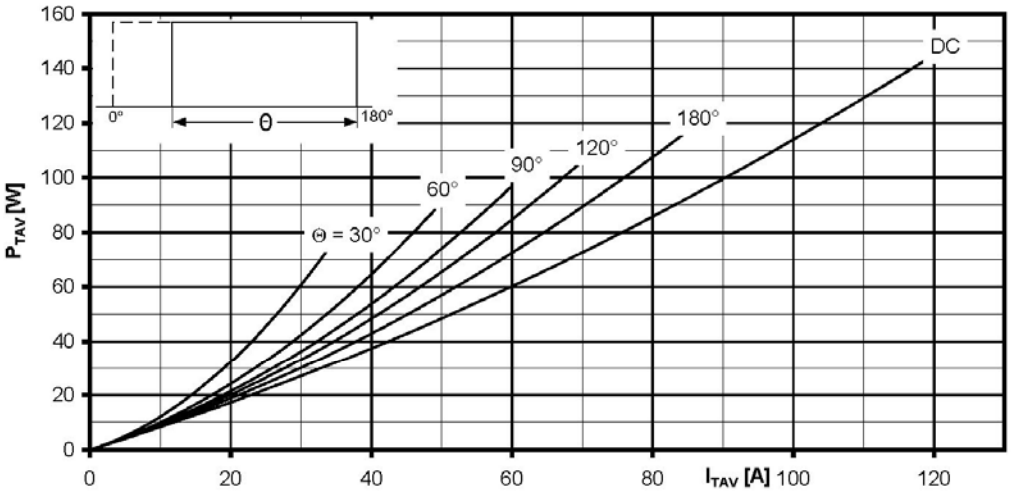


Durchlassverlustleistung je Zweig / On-state power loss per arm $P_{TAV} = f(I_{TAV})$

Sinusförmiger Strom / Sinusoidal current Strombelastung je Zweig / Current load per arm

Berechnungsgrundlage P_{TAV} (Schaltverluste gesondert berücksichtigen)
Calculation base P_{TAV} (switching losses should be considered separately)

Parameter: Stromflußwinkel / Current conduction angle Θ

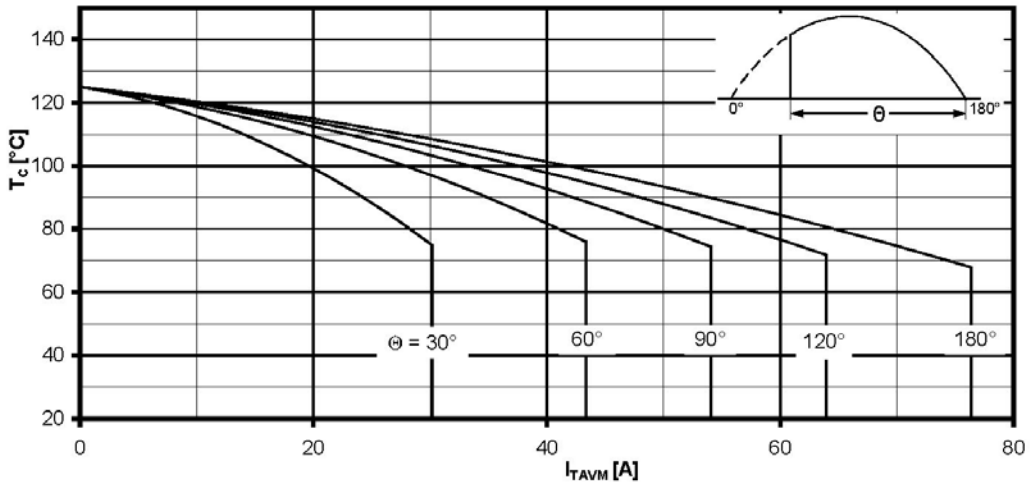


Durchlassverlustleistung je Zweig / On-state power loss per arm $P_{TAV} = f(I_{TAV})$

Rechteckförmiger Strom / Rectangular current Strombelastung je Zweig / Current load per arm

Berechnungsgrundlage P_{TAV} (Schaltverluste gesondert berücksichtigen)
Calculation base P_{TAV} (switching losses should be considered separately)

Parameter: Stromflußwinkel / Current conduction angle Θ

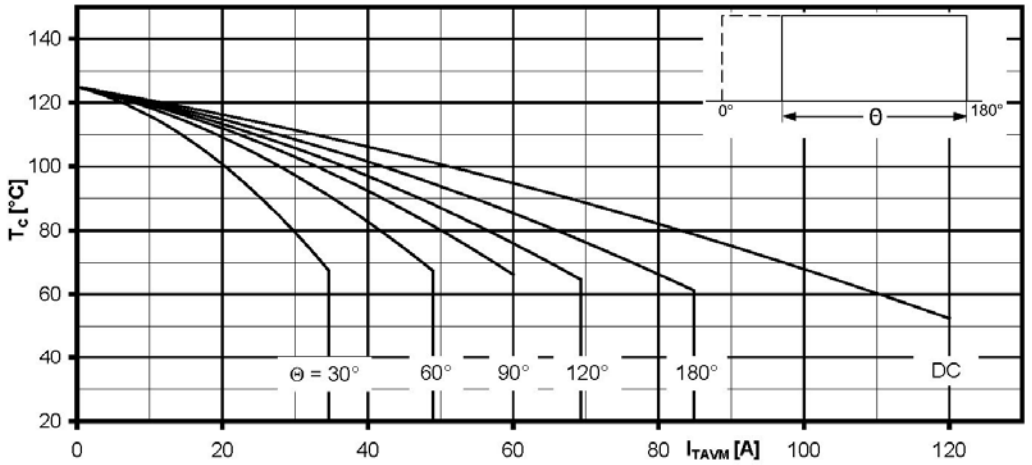


Höchstzulässige Gehäusetemperatur / Maximum allowable case temperature $T_C = f(I_{TAVM})$

Sinusförmiger Strom / Sinusoidal current Strombelastung je Zweig / Current load per arm

Berechnungsgrundlage P_{TAV} (Schaltverluste gesondert berücksichtigen)
Calculation base P_{TAV} (switching losses should be considered separately)

Parameter: Stromflußwinkel Θ / Current conduction angle Θ



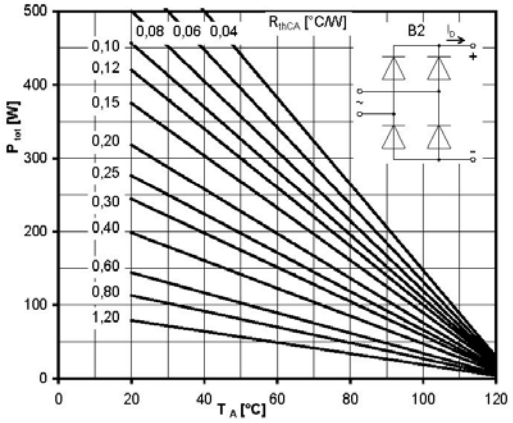
Höchstzulässige Gehäusetemperatur / Maximum allowable case temperature $T_C = f(I_{TAVM})$

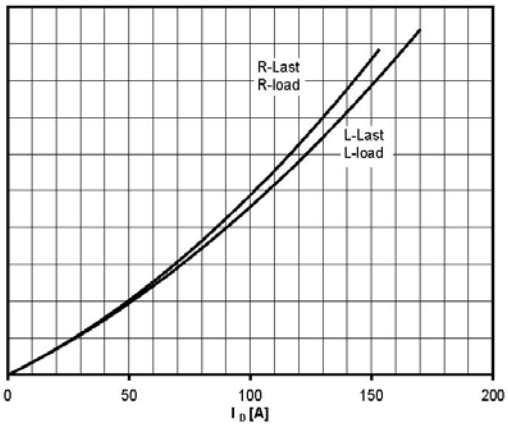
Rechteckförmiger Strom / Rectangular current Strombelastung je Zweig / Current load per arm

Berechnungsgrundlage P_{TAV} (Schaltverluste gesondert berücksichtigen)
Calculation base P_{TAV} (switching losses should be considered separately)

Parameter: Stromflußwinkel Θ / Current conduction angle Θ

N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	



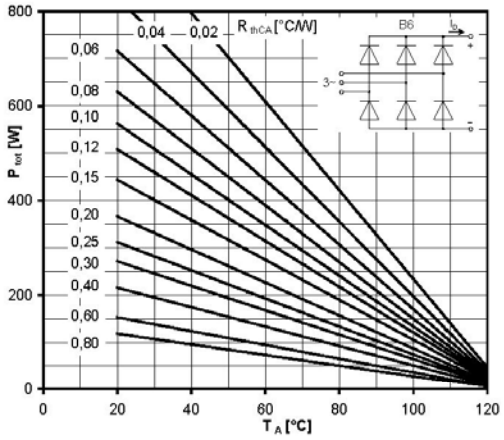


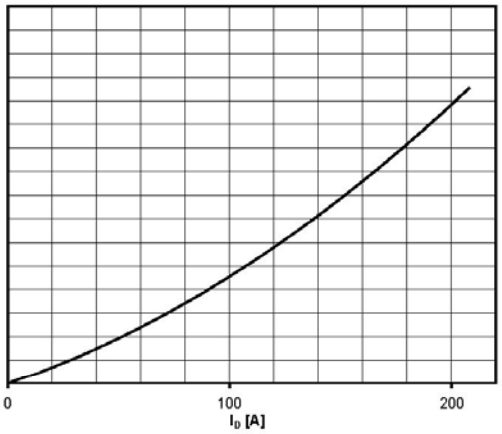
Höchstzulässiger Ausgangsstrom / Maximum rated output current I_D

B2- Zweipuls-Brückenschaltung / Two-pulse bridge circuit

Gesamtverlustleistung der Schaltung / Total power dissipation at circuit P_{tot}

Parameter:
Wärmewiderstand zwischen den Gehäusen und Umgebung / Thermal resistance cases to ambient R_{thCA}



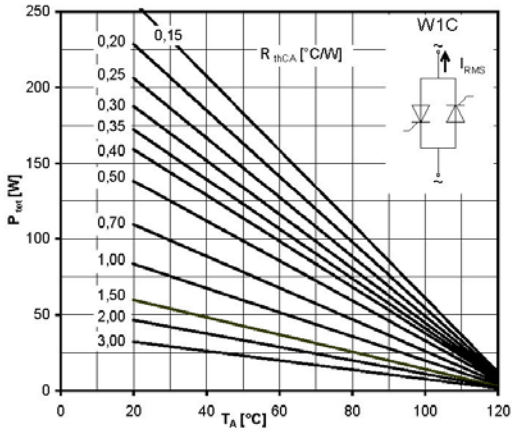


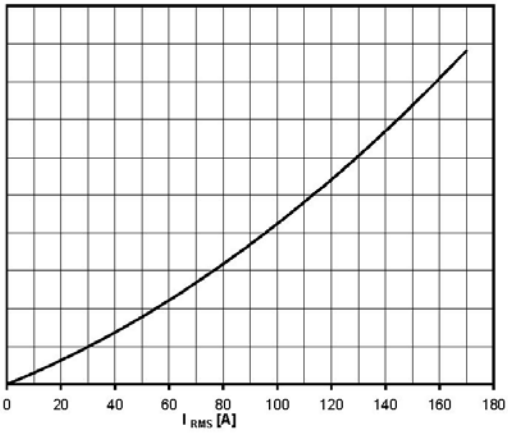
Höchstzulässiger Ausgangsstrom / Maximum rated output current I_D

B6- Sechspuls-Brückenschaltung / Six-pulse bridge circuit

Gesamtverlustleistung der Schaltung / Total power dissipation at circuit P_{tot}

Parameter:
Wärmewiderstand zwischen den Gehäusen und Umgebung / Thermal resistance cases to ambient R_{thCA}



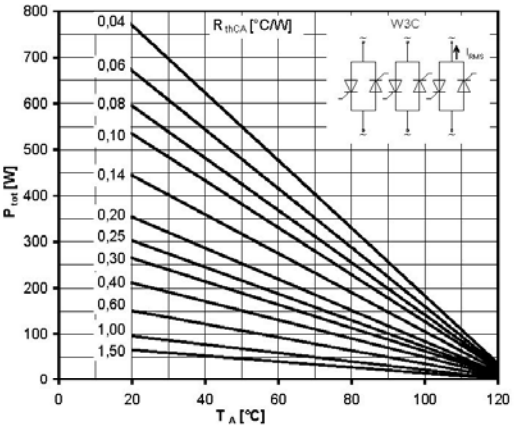


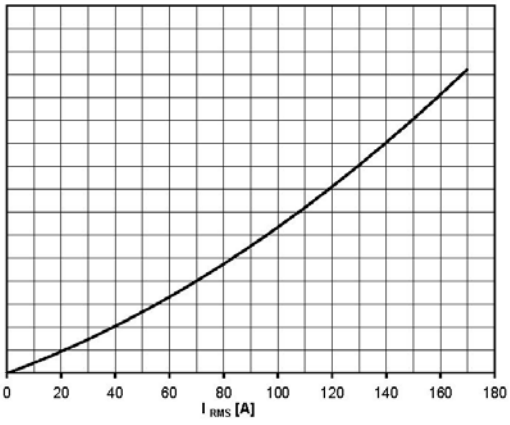
Höchstzulässiger Effektivstrom / Maximum rated RMS current I_{RMS}

W1C - Einphasen-Wechselwegschaltung / Single-phase inverse parallel circuit

Gesamtverlustleistung der Schaltung / Total power dissipation at circuit P_{tot}

Parameter:
Wärmewiderstand zwischen den Gehäuse und Umgebung / Thermal resistance case to ambient R_{thCA}





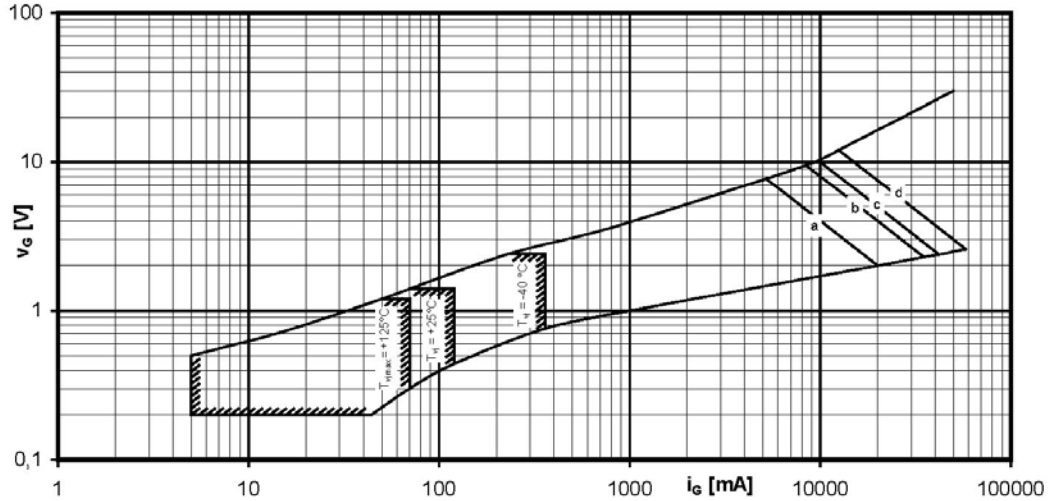
Höchstzulässiger Effektivstrom / Maximum rated RMS current I_{RMS}

W3C - Dreiphasen-Wechselwegschaltung / Three-phase inverse parallel circuit

Gesamtverlustleistung der Schaltung / Total power dissipation at circuit P_{tot}

Parameter:
Wärmewiderstand zwischen den Gehäusen und Umgebung / Thermal resistance cases to ambient R_{thCA}

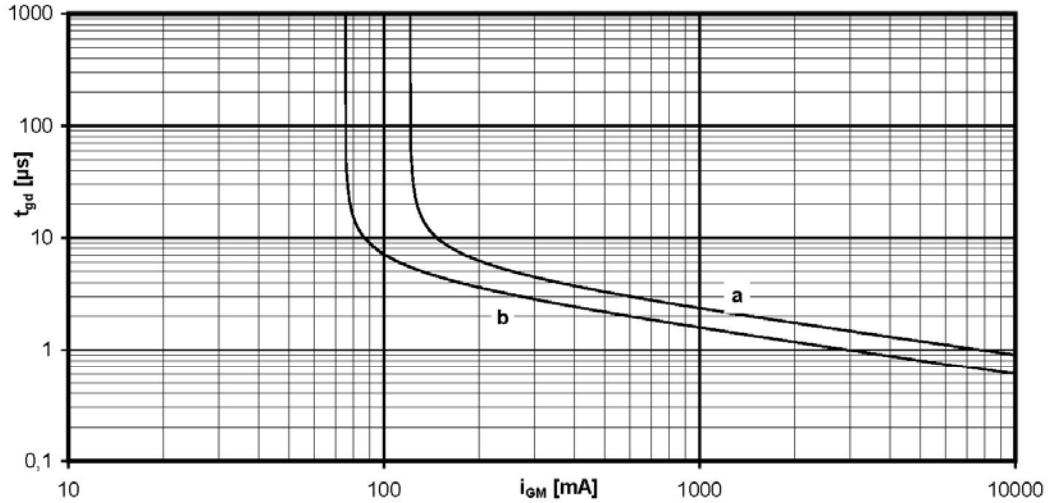
N	Datenblatt / Data sheet	power electronics in motion eupec
Netz-Thyristor-Modul Phase Control Thyristor Module	**TT61N**	



Steuercharakteristik $v_G = f(i_G)$ mit Zündbereichen für $V_D = 6$ V
Gate characteristic $v_G = f(i_G)$ with triggering area for $V_D = 6$ V

Höchstzulässige Spitzensteuerverlustleistung / Maximum rated peak gate power dissipation $P_{GM} = f(t_g)$:

a - 40 W/10ms b - 80 W/1ms c - 100 W/0,5ms d – 150W/0,1ms

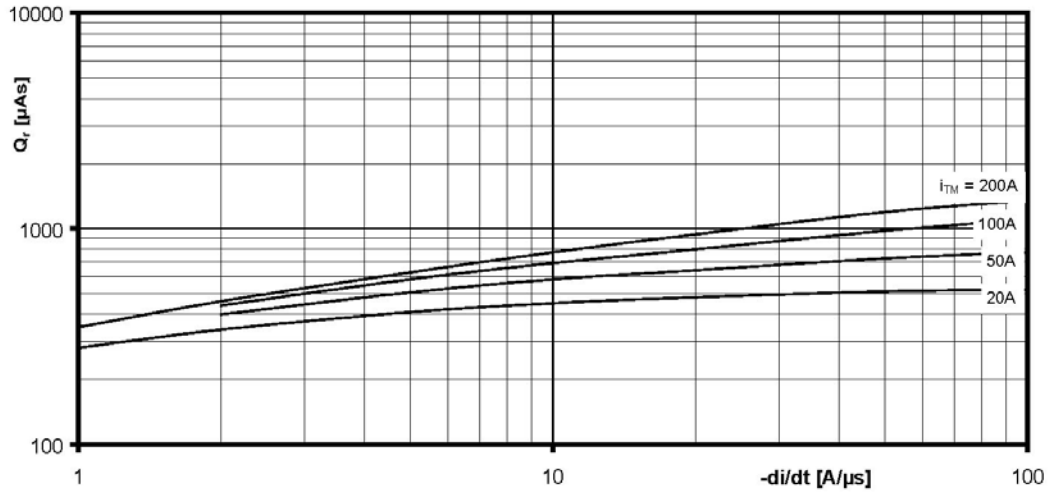


Zündverzug / Gate controlled delay time $t_{gd} = f(i_G)$

$T_{vj} = 25°C$, $di_G/dt = i_{GM}/1\mu s$

a - maximaler Verlauf / Limiting characteristic

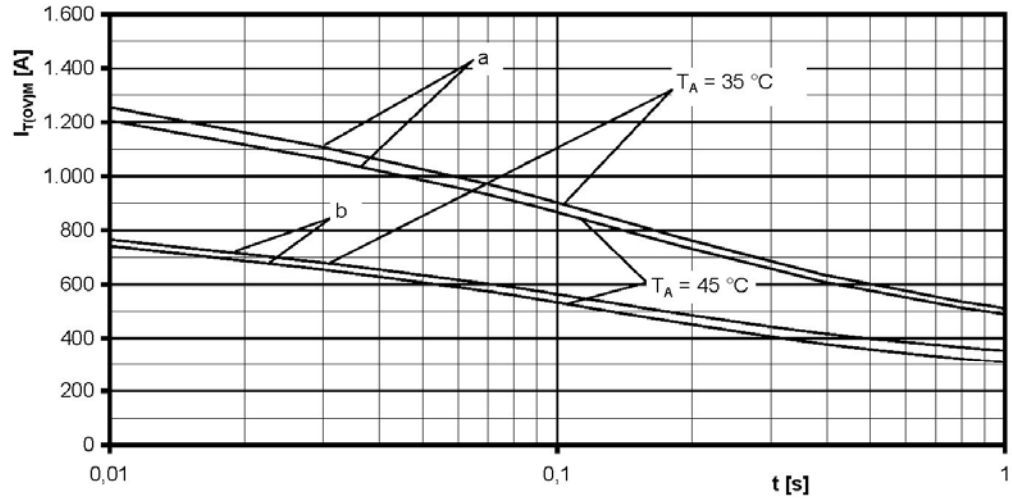
b - typischer Verlauf / Typical characteristic



Sperrverzögerungsladung / Recovered charge Q_r = f(-di/dt)

$T_{vj} = T_{vjmax}$, $v_R \leq 0{,}5\ V_{RRM}$, $v_{RM} = 0{,}8\ V_{RRM}$

Parameter: Durchlaßstrom / On-state current i_{TM}

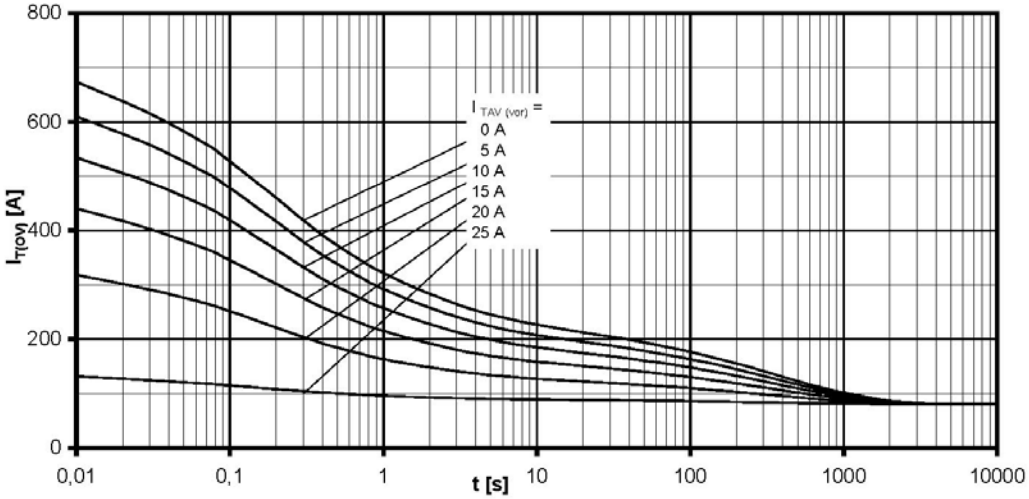


Grenzstrom / Maximum overload on-state current $I_{T(OV)M}$ = f(t), v_{RM} = 0,8 V_{RRM}

Leerlauf / No-load conditions

a: T_A = 35°C, verstärkte Luftkühlung / Forced air cooling

b: T_A = 45°C, natürliche Luftkühlung / Natural air cooling

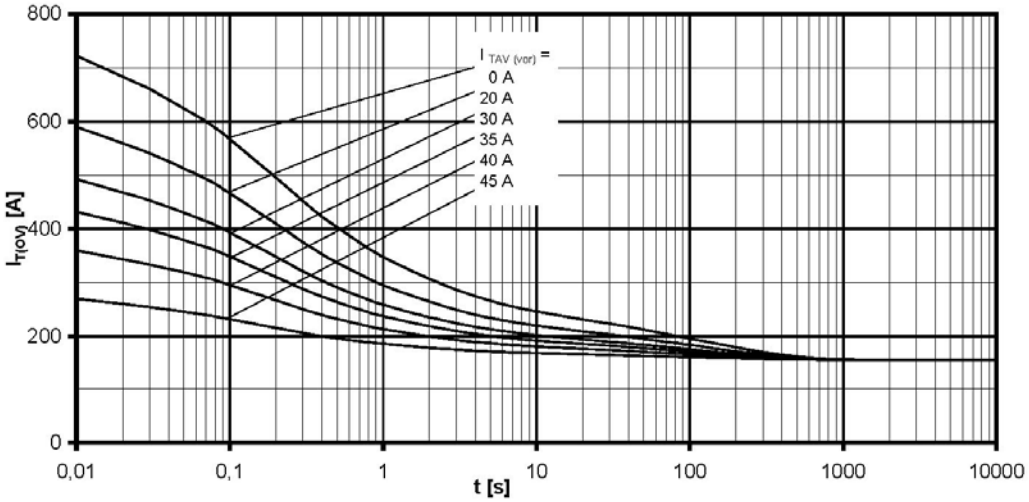


Überstrom je Zweig / Overload on-state current $I_{F(OV)}$

B6- Sechspuls-Brückenschaltung, 120° Rechteck / Six-pulse bridge circuit, 120° rectangular

Kühlkörper / Heatsink type KM14 (50W) Natürliche Kühlung bei / Natural cooling at T_A = 45°C

Parameter: Vorlaststrom je Zweig / Pre-load current per arm $I_{FAV(vor)}$



Überstrom je Zweig / Overload on-state current $I_{F(OV)}$

B6- Sechspuls-Brückenschaltung, 120° Rechteck / Six-pulse bridge circuit, 120° rectangular

Kühlkörper / Heatsink type KM14 (Papst 4650N) Verstärkte Kühlung bei / Forced cooling at T_A = 35°C

Parameter: Vorlaststrom je Zweig / Pre-load current per arm $I_{FAV(vor)}$

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