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CONDUCTED SUSCEPTIBILITY TESTS ON AN ARTIFACT USING IEC AND MIL-STD TEST METHODS

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Kofi Korsah

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Kofi Korsah, Mike Moore, P. D. Ewing, and R. T. Wood

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ABSTRACT

This document presents the results of tests conducted on interconnecting signal lines on an artifact using both the Department of Defense (DoD) (MIL-STD) and European Committee for Electrotechnical Standardization (CENELEC) test criteria. Oak Ridge National Laboratory (ORNL) has been engaged in assisting the U.S. Nuclear Regulatory Commission Office of Nuclear Regulatory Research in developing the technical basis for regulatory guidance on electromagnetic interference (EMI) and radio frequency interference (RFI) and power surge withstand capability (SWC). The current study focuses on the susceptibility of instrumentation and control (I&C) systems to conducted EMI/RFI along interconnecting signal lines. Coverage of signal line susceptibility was identified as an open issue in previous research on establishing the technical basis for EMI/RFI and SWC in safety-related I&C systems.

The artifact used for the tests was developed at ORNL and consisted of an analog-to-digital converter (ADC) and a random access memory (RAM) interfaced to a laptop computer through optoisolators. The optoisolators were used for all analog and digital input output (I/O) data lines as well as the control and address lines. This ensured that high level perturbations due to test signal injection in the data lines would not propagate into the computer.

The military standards used were CS101, CS114, CS115, and CS116. The European standards used were IEC 61000-4-4, IEC 61000-4-5, IEC 61000-4-6, and IEC 61000-4-12. These tests were performed to compare U.S. and European conducted susceptibility standards. In particular, the test results were analyzed with the objective of answering the following questions: (1) are the test methodologies comparable, (2) are the test limits comparable, and (3) for the test standards which are comparable, did the results show failure at comparable levels?

Significant findings resulting from this study are as follows:

1) MIL-STD-461 tries to control the delivered current to the EUT, while IEC 61000-4 focuses on controlling the source voltage (and sometimes power).

2) The operating envelopes of MIL-STD-461 use units of amps, while IEC 61000-4 uses units of volts.

3) MIL-STD-461 uses injection probes (inductive), while IEC 61000-4 uses capacitive coupling (except for IEC 61000-4-6).

4) MIL-STD-461 typically calls for adjusting the test generator output to maintain a given level of current injection with the EUT in the circuit; while IEC 61000-4 series does not typically adjust for the impedance realities of the EUT.

5) MIL-STD-461 typically calls for probe to EUT distances of about 5 cm, whereas IEC 61000-4 allows for up to 1 m. This can affect test results above 30 MHz ($\lambda < 10$ m) since the cable length becomes a significant portion of a wavelength. When the insertion distance becomes a significant portion of a wavelength, the looking-in impedance of the EUT, translated to the injection point, can be greatly affected.

CS114 and IEC 61000-4-6 are the closest equivalents in that they address RF interference, use injection probes, and use fairly similar frequency ranges. Almost all thresholds were a few dB for the two tests. Since the test methods are similar and both use injection probes for coupling, the similarity of these tests is expected. The differences in modulation types and sweep rates were the likely causes for the slight deviations in the test results.

CS116 and IEC 61000-4-12 are similar in that they both apply the damped sine wave with approximately the same power. CS116 and IEC 61000-6-12 both apply the damped sine waveform. However, IEC 61000-4-12 also calls for a Ring Wave test. In the artifact test of IEC 61000-4-12, only the ring wave waveform was used. Therefore, any comparison would be suspect, especially since the threshold of energy necessary to cause errors were not reached in the IEC 61000-4-12 tests. Further investigation is needed to complete the comparison of these tests.

CS101 only addresses power lines and is not comparable with any of the IEC standards used in the tests.

CS115 is the only one of the test methods dedicated to exciting natural resonances.

IEC 71000-4-4 and IEC 61000-4-5 are similar, but the first is aimed at applying EFT voltages and the second is aimed at applying surge voltages, such as those caused by lightning. Therefore, IEC 61000-4-4 uses a much higher coupling impedance (lower capacitance) than does IEC 61000-4-5. The tests produced very dissimilar results. Further investigation is needed to determine why the results differed so much.

1. ARTIFACT DESIGN

1.1 SYSTEM-LEVEL DESCRIPTION OF ARTIFACT

The following objectives were observed in the design of the Artifact:

a. The use of a minimal set of components in order to reduce the number and type of errors that could be encountered and observed at the chip level.

b. Isolation of Artifact from the control/monitoring equipment so that observed errors could be directly attributable to the application of the EMI/RFI testing signal to the Artifact itself, and not as a result of propagation of effects from the control/monitoring equipment.

To achieve objective (a), only two components (one RAM and one ADC) were used as discussed. Design methodologies used to achieve objective (b) (use of optocouplers) are discussed in section 1.2.2.

The artifact was developed at ORNL and consisted of an analog-to-digital converter (ADC) and a random access memory (RAM) interfaced to a laptop computer through optoisolators. The latter were used for all analog and digital input/ output (I/O) data lines as well as the control and address lines. This ensured that high level perturbations due to test signal injection in the data lines would not propagate into the computer.

The artifact actually consists of two separate modules; an Artifact Module (AM) and an Interface Module (IM), each housed in a separate chassis. Figure 1.1 shows a block diagram of the AM and how it interfaces to the Personal computer (PC) through the IM.

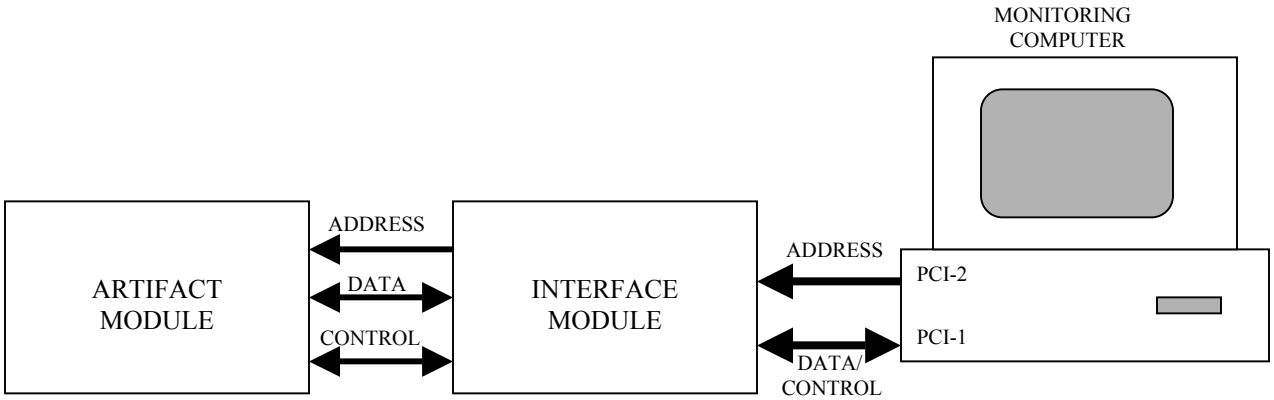


Fig. 1.1. ORNL Artifact System interconnections to a personal computer

Fig. 1.2 shows a system-level schematic of the same configuration. Figure 1.3 shows a detailed circuit diagram of the Artifact Module while Fig. 1.4 shows a circuit diagram of the Interface Module. The AM consists of a single printed circuit board (PCB) containing the ADC and the RAM. The IM also consists

of a single PCB containing all the optoisolators used for interfacing the data, address, and control lines of from the AM.

1.2 ARTIFACT AND INTERFACE MODULE SCHEMATICS

1.2.1 Artifact Module

The PCB in the AM chassis consists of one 8-bit CMOS successive approximation ADC (model ADC0802, (U1), and one 128K x 8 Static RAM (model CYC1009, (U3). A DC power source supplies +15V, and -15V to the board. In addition, two voltage regulators U5 and U4 respectively supply +5V to the circuits on board, and $V_{ref}/2$ (in this case, 2.5V) to the ADC.

An internal clock is generated by the ADC for internal timing purposes. This clock is connected via buffer U2 output CLOCK_READ to the input of ISO29 (Fig. 4), and may be read by the computer for diagnostics or other purposes.

1.2.2 Interface Module

The PCB in the IM chassis consists of 32, 20 Mbd high common-mode rejection logic optocouplers. The model HCPL-2430 optocouplers are interfaced to the 16 RAM address lines (A0_A through A16_A), and the control lines BAR_RD_C(A), BAR_WR_C(A), BAR_CS_C(A), BAR_CE1_C(A), BAR_WE_C(A), BAR_OE_C(A), OPTOTRI (OPTO_WRITE_1, OPTO_WRITE_2, and OPTOTRI_IN). Note that the optocouplers work in such a way that when the cathode of the input diode goes LO, it turns the associated NAND gate ON and its corresponding output goes LO. For example, when OPTOTRI goes LO, both PTO_WRITE_1 and OPTOTRI_2 go LO, and OPTOTRI_IN goes HI, since its input OPTOTRI is inverted through U6A.

The HCPL-2430 is also used to interface an external clock from the computer to the ADC in the artifact through CLOCK_OUT_A. Note that although this provision has been made, the artifact currently does not use an external clock; rather, as has already been explained, an internal clock is generated by the ADC in the artifact, which is connected to the input of ISO29 via CLOCK_READ_A.

The 8-bit data bus from the computer go through 8 pairs of optoisolators (model HCPL-2400). Each pair is connected back-to-back such that the 8 pairs form an 8-bit, bi-directional data bus. For example in Fig. 1.4, consider the optoisolator pair connected to any of the data lines DATA_IN_IOX. When the tristate input OPTOTRI of ISO25 is LO, the output of the same chip (OPTO_WRITE_1) is LO and the associated output (OPTOTRI_IN) from U6A is HI. The reverse is true when OPTOTRI is HI. OPTO_WRITE_1 is connected to the tristate input of one half of the optoisolator pair, and OPTOTRI_IN is connected to the tristate input of the other half. When this tristate input is LO, the associated optoisolator is enabled and when it is HI, the associated optoisolator is disabled (high impedance state). Thus, when the control signal OPTOTRI from the computer is LO (OPTO_WRITE_1 is LO and OPTOTRI_IN is HI), data from the computer side (DATA_IN_IOX) is available on the Artifact side (DATA_OUT_IOX), i.e., data is *written* by the computer to the Artifact. On the other hand, when the control signal OPTOTRI from the computer is HI (OPTO_WRITE_1 is HI and OPTOTRI_IN is LO), data from the Artifact side (DATA_OUT_IOX) is available on the computer side (DATA_IN_IOX), i.e., data is *read* by the computer from the Artifact.

The analog signal from the computer connects to the Artifact through a high linearity analog optocoupler HCNR201.

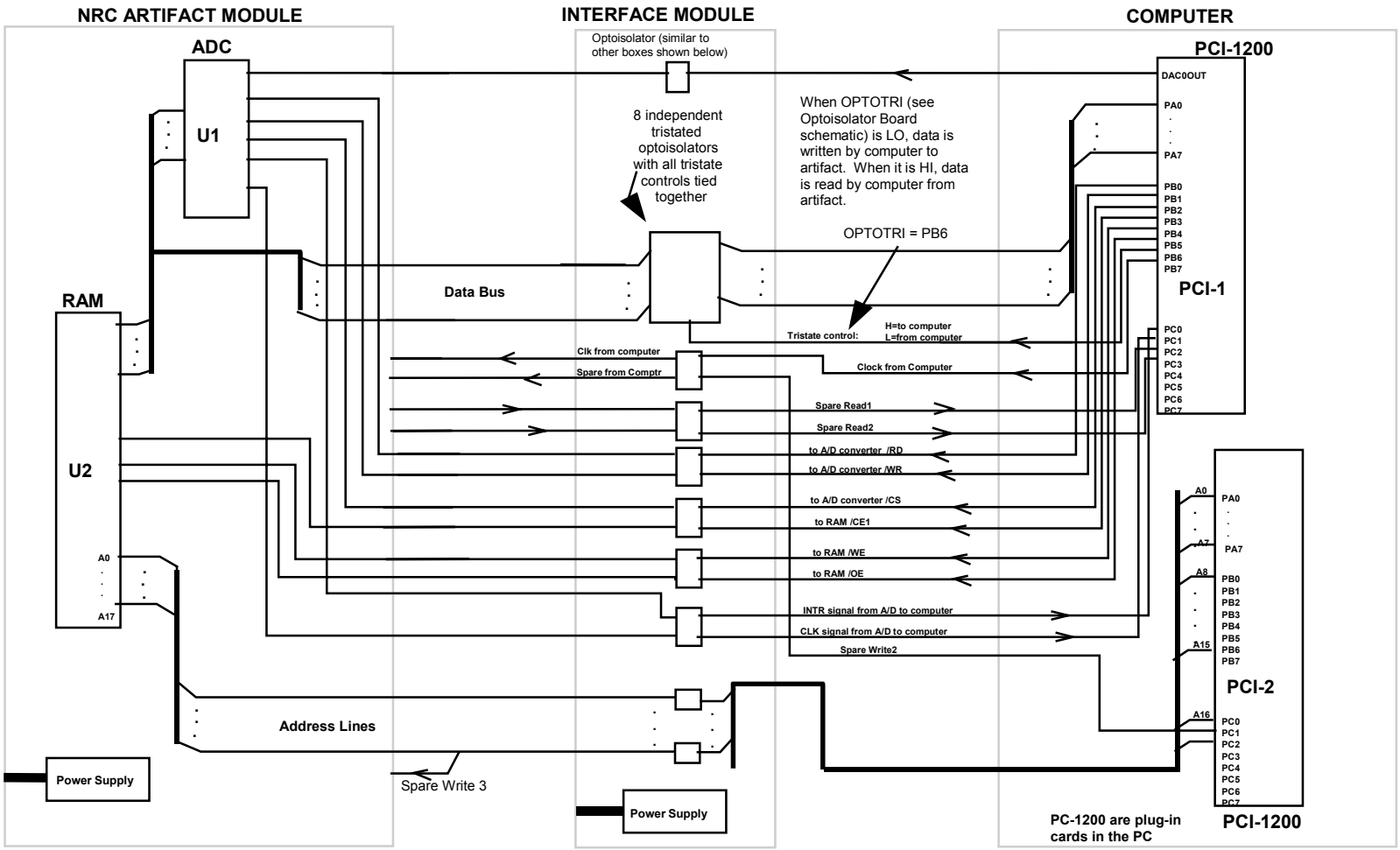


Fig. 1.2. Block diagram of artifact and interface modules showing interconnections to computer

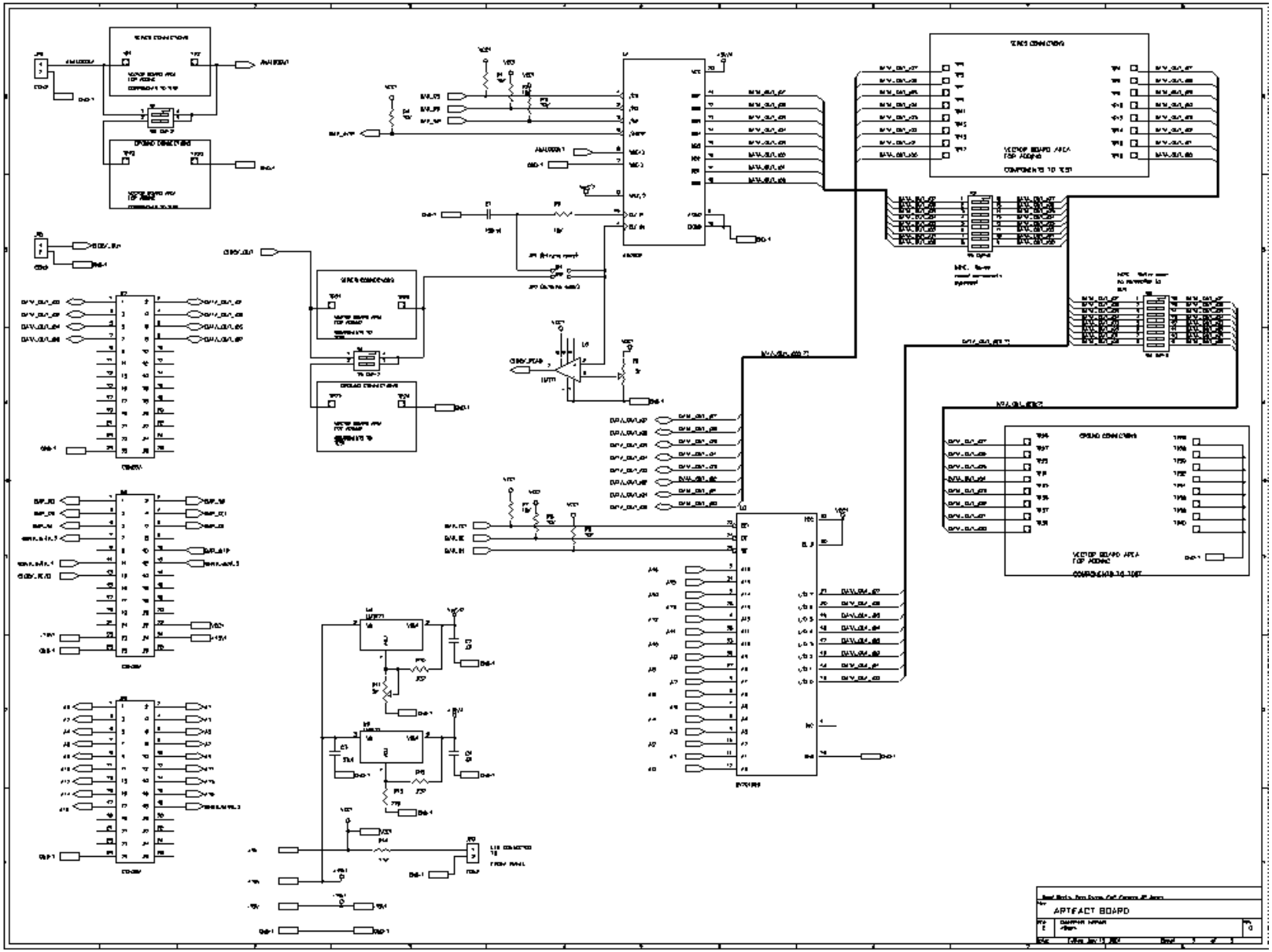


Fig. 1.3. Schematic of artifact module.

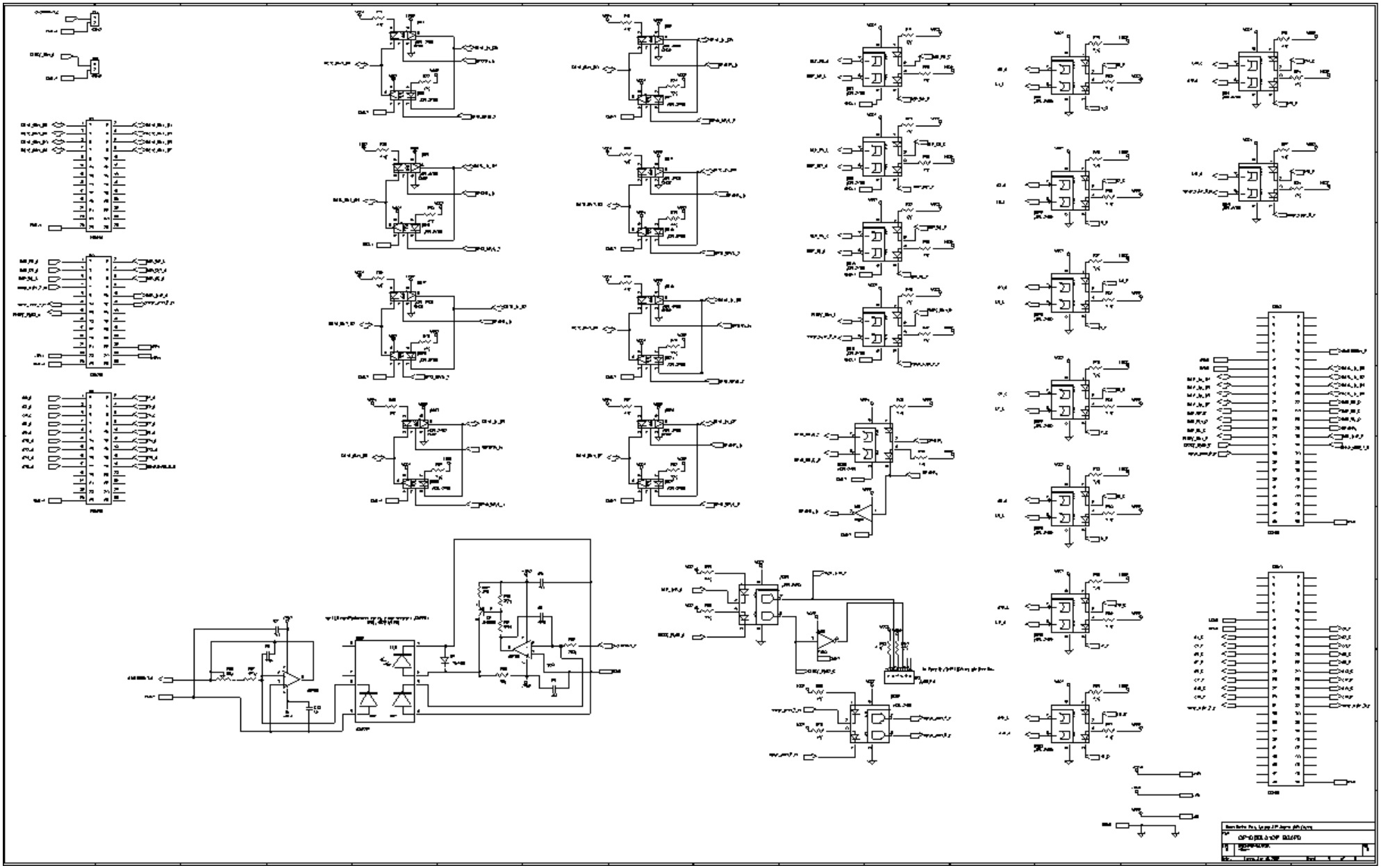


Fig. 1.4. Schematic of interface module.

1.2.3 Multi-Function Boards: PCI-1200 I/O Cards

The IM connects to the PC through two identical Multifunction I/O Boards the PCI-1200. The PCI-1200 has 8 single-ended, 4 differential, software selectable analog input (via analog-to-digital converter (ADC)) channels; 2 analog output (via digital-to-analog converter (DAC)) channels; and 24 digital I/O lines. These I/O lines are configured as three 8-bit ports (PA, PB, and PC). There are 3 programmable modes of operation for the digital ports—Mode 0, Mode 1, and Mode 2. Each of these modes determine how individual ports are configured (input, output, or bi-directional). These modes can be changed at any time within a program via a control register CR. The three ports in each of the PCI-1200 cards (PCI-1 and PCI-2 in Fig. 1.1) are configured as follows:

Ports in PCI-1
Port A is used as the data bus. It is used to input data from either the Analog-to-Digital Converter (U1) or the RAM (U2). It is also used to output data to the RAM. Thus, port A is used both as input and output (I/O) port.

Port B is used only as an output port. The bits of this port are used to control the ADC and the RAM.

Port C is used as input port. (Only the lower nibble is used in this design).
Mode 0 is used as the programmable mode for this configuration. The control word (in the CR register) necessary for this configuration is shown in Table 1.1. The Number column corresponds to the number chosen out of the 16 possible configurations in Mode 0:

Table 1.1 Control word content for PCI-1 ports configuration (Mode 0)

	Control Word	**Group A**		**Group B**	
Number	**Bit 76543210**	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
5	10001001 (89H)	Output	Input	Output	Input
13	10011001 (99H)	Input	Input	Output	Input

[1]Upper nibble of Port C
[2]Lower nibble of Port C

The bit designations for the ports during each configuration in Mode 0 are illustrated below:

input	input	input	input	input	input	input	input
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Mode 0; CR=99H

output	output	output	output	output	output	output	output
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Mode 0; CR=99H

input	input	input	input	input	input	input	input
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Mode 0; CR=99H

output	output	output	output	output	output	output	output
PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0

Mode 0; CR=89H

output	output	output	output	output	output	output	output
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0

Mode 0; CR=89H

input	input	input	input	input	input	input	input
PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Mode 0; CR=89H

Ports in PCI-2

Most of the digital bits in PCI-2 are used as address lines (there are 17 address lines in all) for the RAM (U2). Only two other bits are needed as outputs (i.e., the total number of bits needed as outputs = 19). Thus, for convenience, ports A, B, and C are all configured as output ports. This configuration corresponds to Mode 0 with a CR value of 80H as shown in Table 1.2.

Table 1.2. Control word content for PCI-2 ports configuration (Mode 0)

	Control Word	**Group A**		**Group B**	
Number	**Bit 76543210**	**Port A**	**Port C[1]**	**Port B**	**Port C[2]**
0	10000000 (80H)	Output	Output	Output	Output

[1]Upper nibble of Port C
[2]Lower nibble of Port C

1.3 SYSTEM SOFTWARE

1.3.1 System Algorithm

Assumptions:

a). The control inputs to the ADC in the artifact from computer are Read, (BAR_RD (the BAR designation signifies a LO TRUE signal)), Write, (BAR_WR), and Chip Select , (BAR_CS). In addition, there is one control output from the ADC to the computer; the Interrupt, or BAR_INTR

b). The control inputs to the RAM in the Artifact from the computer are Chip Enable One (BAR_CE1), Write Enable, (BAR_WE) and Output Enable (BAR_OE).

Algorithm:

1. Computer generates, via the digital-to-analog converter (DAC), the analog equivalent of the digital data XXH and sends it to the ADC in the Artifact. Valid values of XXH are from 00H - FFH, corresponding to 8 bits of ADC resolution.

2. Computer selects ADC in the Artifact by setting BAR_CS LO. Note that the RAM need not be selected at this time (i.e., BAR_CE1remains HIGH. BAR_WE and BAR_OE are also placed HI at this time). (Note that the other control input of the RAM, CE2 (pin 30), is tied to Vcc permanently. Note that BAR_WR and BAR_RD of the ADC remain HI at this time.

3. Computer commands ADC in the Artifact to convert analog data by setting pulsing BAR_WR LO (i.e., setting BAR_WR LO), and then back to HI. (Note that according to the data sheet, conversion will start from 1 to 8 clock periods after at least one of the inputs BAR_CS or BAR_WR makes a LO-to-HI transition.)

4. Computer waits for 10 ms (data conversion will be completed long before this time), then commands the A/D in the artifact to put the converted data on the output bus. It does this by setting BAR_RD LO (the combination of BAR_CS and BAR_RD LO will reset the BAR_INTR line HI. This line went LO when conversion was complete, and could have been used by the computer to detect Conversion Complete. The ***n***INTR will indeed be monitored by the computer, but will be used only for diagnostics purposes. If the computer depends on BAR_INTR to proceed, the computer will be in an infinite loop (i.e., will not continue further tests) if the ADC malfunctions.

5. The computer reads the digital data from the ADC and compares it with the XXH value it put out during step 1. These values should match. Note that BAR_RD is set back to HI after the data has been read by the computer. This puts the ADC output in the high impedance state.

The RAM now needs to be checked with the same digital value it used for the A/D. The problem is, to which RAM location do we write this data? We can solve this problem simply by using the digital ***data*** *generated in step 1 (XXH) also as an* ***address*** *for the RAM.*

6. Computer outputs the value XXH onto the address bus.

7. Computer commands RAM to write data into location XXH. It does this by pulling BAR_CE1 and BAR_WE LO. This will put the data into the RAM.

8. Computer reads back data from RAM. It does this by first pulling BAR_WE HI, then BAR_OE LO. (BAR_CE1 remains LO). Both the written data and the read data should match. After the data has

been read, BAR_CE1, BAR_WE, and BAR_OE are all pulled back up HI. This deselects the RAM and puts the output in the high impedance state, ready for the next iteration.

9. Loop is repeated for the next digital value (XXH + 1).

1.3.2 Types of Errors Encountered

The following list gives the types of errors in the Artifact that the monitoring system was designed to log:

1. ADC Data Mismatches:
This type of error occurred whenever there was a difference between the value of analog data sent to the ADC by the monitoring computer (MC), and the value reported back from the ADC to the MC. An example of an actual entry in the error file is as follows:

12:31:50 PM ADC Mismatch (3) Analog in = 5.000 V Analog out = 4.784 V

The first column is a time stamp, showing the time that the error occurred. The second column shows the time of day (AM or PM). The fourth column [(n)], gives the number of times the particular error (in this case, ADC Mismatch) has occurred during the particular test run. For the error entry under consideration, a total of 3 ADC mismatches has occurred since the beginning of the test run. The fifth column gives the value of the analog voltage as sent to the ADC from the MC. Finally, the sixth column gives the voltage value sent back to the MC from the ADC.*
The software was designed to allow the ADC to cycle from 0V through 5.0V in approximately 20mV increments.**

2. RAM Data Mismatches:
This type of error occurred whenever there was a difference between the byte of data sent to the RAM by the MC, and the digital byte reported back from the RAM to the MC. An example of an actual entry in the error file is as follows:

1:43:55 PM RAM Mismatch (1) Digital in = 255 Digital out = 129

This entry is similar to entry type (1), and is self-explanatory.

1.3.3 Software Implementation

The software was implemented in LabVIEW, a graphical programming language well suited to data acquisition and instrumentation and control applications. Figure 1.5 shows the front panel of the artifact control software.

* During the tests, the system was set up to log ADC mismatches that were greater than 100mV.
** For an 8-bit ADC, this is equivalent to 1-bit change.

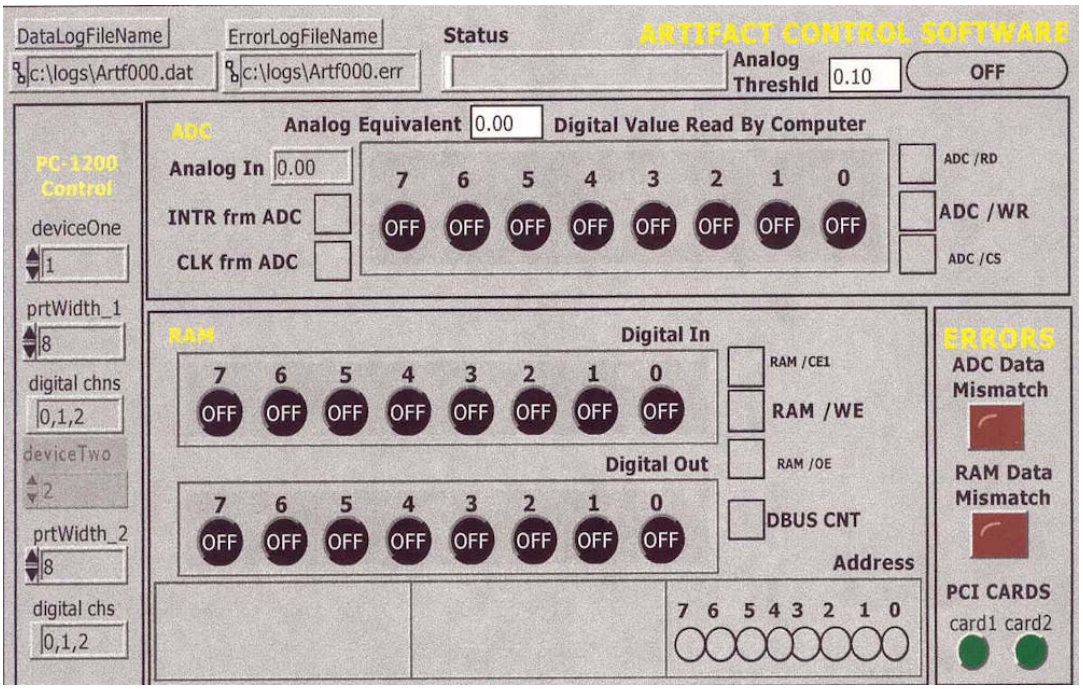


Fig. 1.5. Front panel of the artifact control software.

2 CONDUCTED SUSCEPTIBILITY TESTS

2.1 GENERAL TEST PROCEDURE

The objective of the EMI/RFI tests was to make the artifact malfunction (if possible) without permanent damage. Thus, the general procedure followed for all the tests was the following:

a. Increase the test signal by a predetermined amount from its current setting and wait for 30 seconds.
b. If there are no errors repeat step (a).
c. If there are errors, verify their repeatability by reducing the current test signal setting, then increasing it back up again.
d. Log any errors on file dynamically during the testing.

NOTE: To ensure that the equipment was functioning properly, baseline data was obtained for at least 5 min. prior to each test.

The system configuration during an actual test run is shown in Figs. 2.1 and 2.2. (Fig. 2.1 shows the monitoring computer and Interface module, while Fig. 2.2 shows the Artifact system under test).

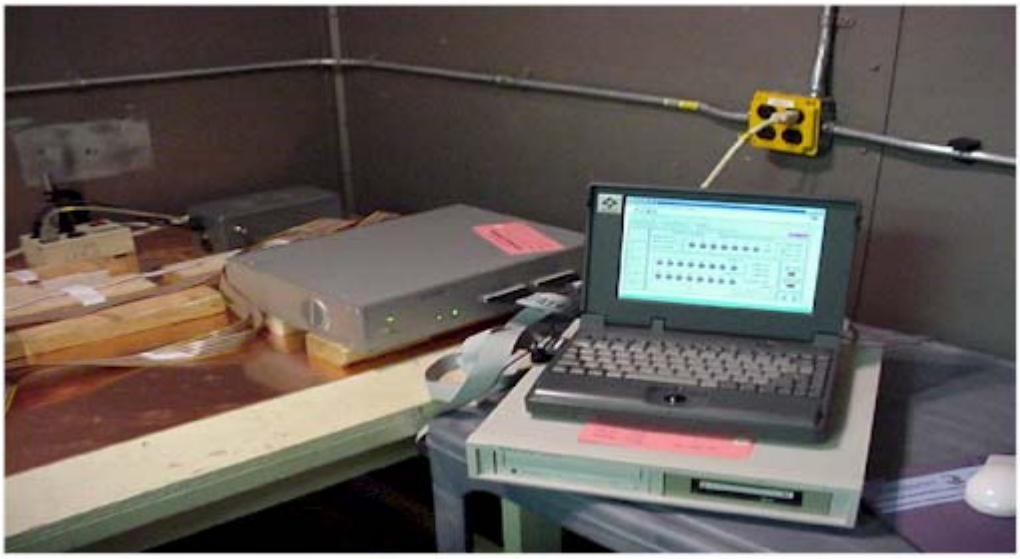


Fig. 2.1 Monitoring computer and interface module.

Fig. 2.2 Artifact system under test.

2.2 CS101 (CONDUCTED SUSCEPTIBILITY, 30 Hz to 50 kHz): TEST SUMMARY

The CS101 test ensures that equipment and subsystems are not susceptible to voltage distortions present on the power leads in the frequency range 30 Hz to 50 kHz. The test is applicable to AC and DC power leads, not including grounds and neutrals. If the Equipment-Under-Test (EUT) is DC operated this test is applicable over the frequency range 30 Hz to 50 kHz. If the EUT is AC operated, this test is applicable starting from the second harmonic of the power frequency and extending to 50 kHz.

The EUT should not exhibit any malfunction or degradation of performance beyond specified operational tolerances when subjected to electromagnetic energy injected unto its power leads at the levels and frequencies given in Fig. 2.3.

Prior to the CS101 tests, initial generator settings are determined using a calibrated load as shown in Fig. 2.4. During the EUT testing, the power and voltage are both monitored. Adjustments are made, as necessary, to maintain either voltage and/or power limits given, without going over the power setting determined during calibration.

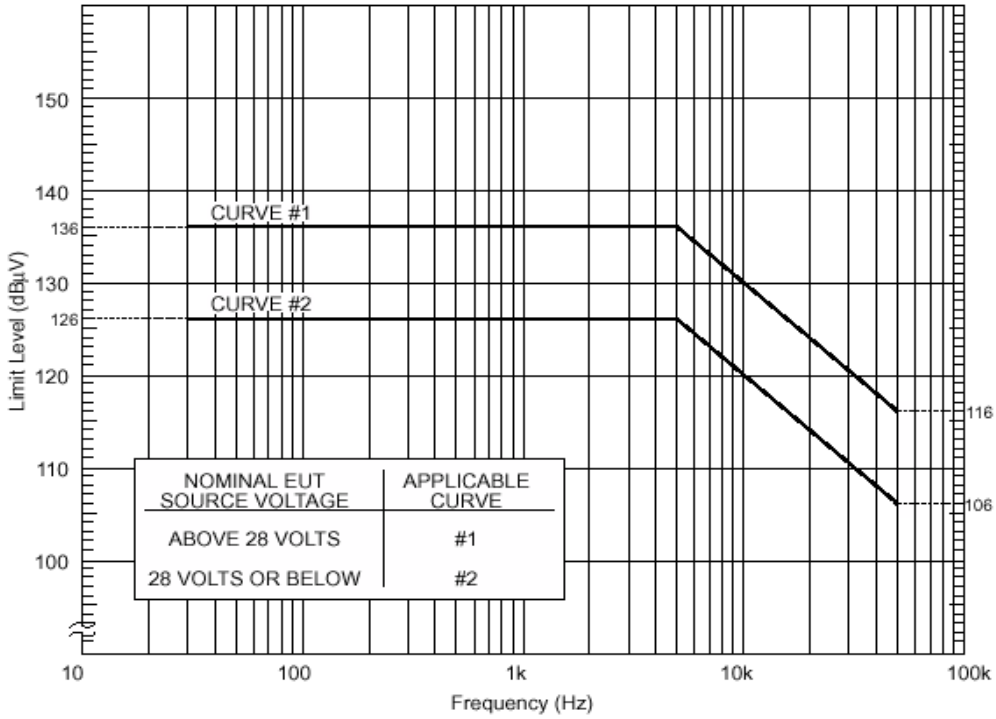


Fig. 2.3. CS101 Limit [EUT power leads, AC and DC for all applications (MIL-STD-461D)]

2.2.1 Artifact Test Procedure for CS101

The signal generator was first calibrated in accordance with MIL-STD-462D (1993) (see Fig. 2.4) to determine the signal source setting needed to maintain the required power level. Actual testing of the Artifact was performed in accordance with MIL-STD-462D (1993) (see Fig 2.5). In particular, the following test procedure was followed:

1. The signal generator was set to the lowest test frequency, then increased until the required voltage or power level was reached.
2. While maintaining the required signal level, the required frequency (e.g., 30Hz – 100Hz, 1kHz – 10 kHz) range was scanned at a rate specified in the standard.
3. If errors were recorded, the test was repeated at his frequency range to verify that the error(s) was repeatable.
4. Errors were recorded as shown in Table 2.1.

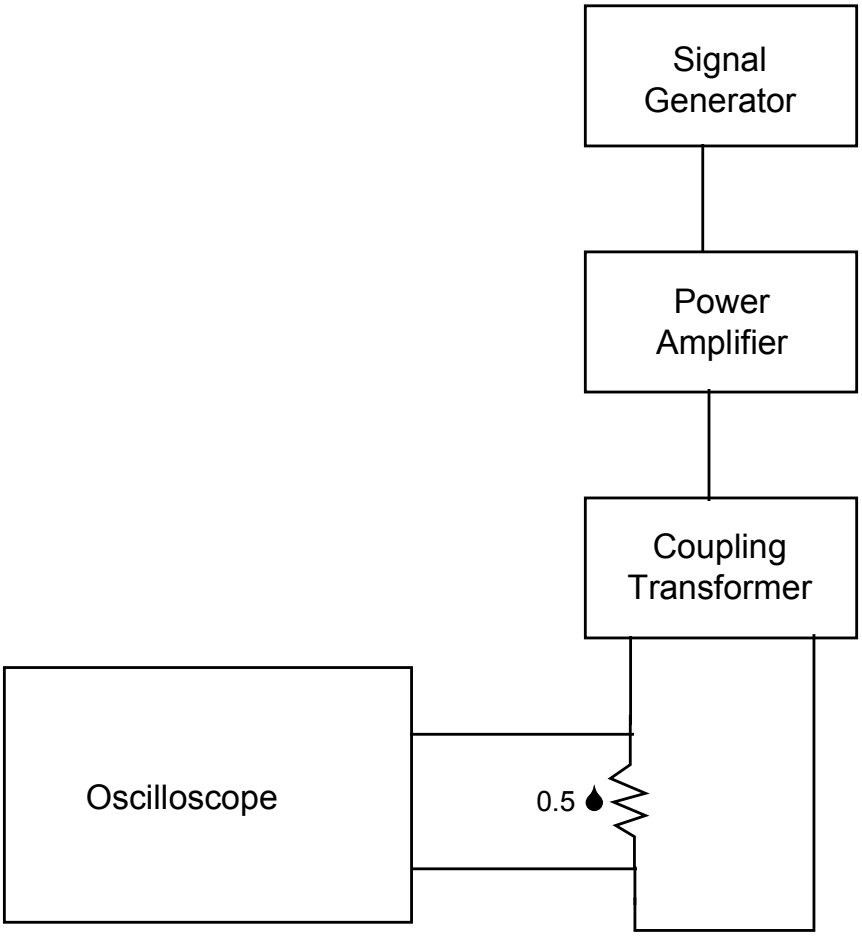


Fig. 2.4. CS101 Calibration Setup

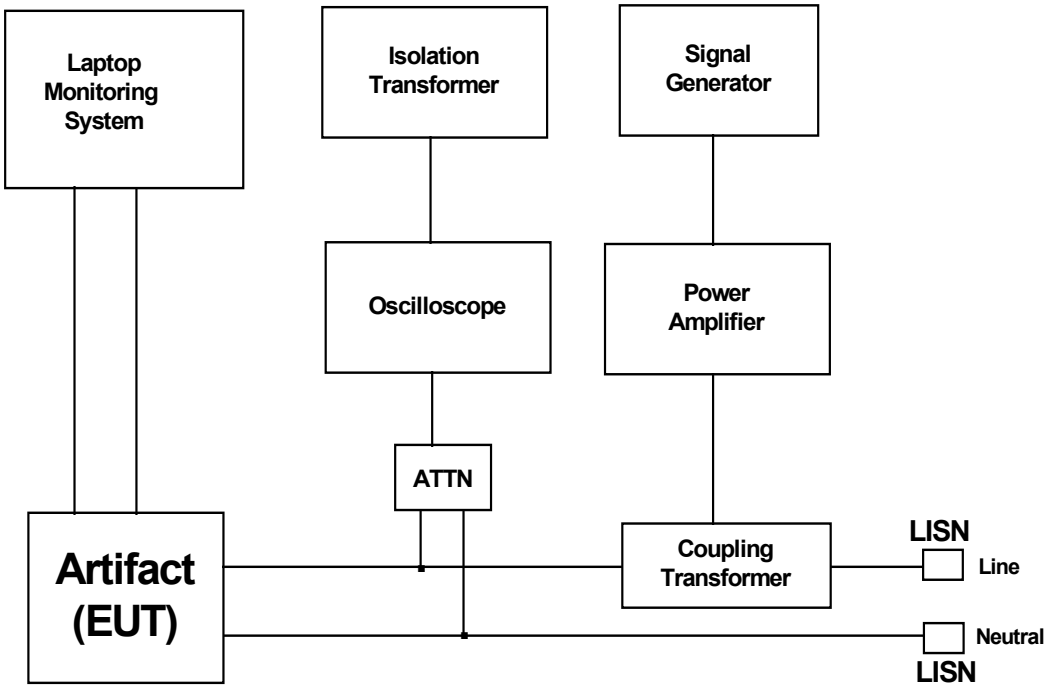


Fig. 2.5. CS101 Signal Injection

2.3 CS101 TEST RESULTS

Table 2.1. CS101 Test Results: test injection point was approximately 1 m from EUT.

Frequency Range	Scope reading (V p-p)	Equivalent injected signal (obtained from calibration step) (Vrms)	Errors
30 Hz - 100 Hz	0.3	2	No
30 Hz - 100 Hz	0.6	4	No
30 Hz - 100 Hz	0.9	6	No
30 Hz - 100 Hz	1.2	8	No
30 Hz - 100 Hz	1.6	10	No
100 Hz - 1kHz	1.6	~10	No
1 kHz - 10 kHz	1.7	~10	No
10 kHz - 50 kHz	1.6	~10	No
30 Hz - 100 kHz	1.6	10	No

2.4 CS114 (CONDUCTED SUSCEPTIBILITY, BULK CABLE INJECTION, 10 kHz to 400 MHz) TEST SUMMARY

The CS114 test is used to verify the ability of the EUT to withstand radio frequency (RF) signals coupled onto EUT associated cabling. The requirement is applicable to all interconnecting cables, including power cables.

The equipment shall not exhibit any malfunction, degradation of performance, or deviation from specified indications beyond the tolerances indicated in the individual equipment's specification, when subjected to a test signal with calibration levels as specified in Fig. 2.6. For a military application, the appropriate limit curve that applies in Fig. 2.6 depends on the intended installation (details are specified in MlL-STD-461D). MIL-STD-461D also states that the requirements of the standard are met if the following currents are induced in the cable under test and the EUT is not susceptible:

Curve 5:	115 dBμA
Curve 4:	103 dBμA
Curve 3:	95 dBμA
Curve 2:	89 dBμA
Curve 1:	83 dBμA

Initial test generator settings for each test frequency range are determined using a calibration fixture. During the EUT testing, the forward power and current are both monitored. Adjustments are made, as necessary, to meet the less stringent of these two.

2.4.1 Artifact Test Procedure for CS114

The signal generator was first calibrated in accordance with MIL-STD-461D (see Fig. 2.7) to determine the signal generator setting needed to maintain the required power level. Actual testing of the Artifact was performed in accordance with MIL-STD-462D (see Fig 2.8). In particular, the following procedure was followed:

1. The signal generator was set to 10 kHz with a 1kHz pulse wave modulation, 50% duty cycle.
2. The forward power, determined during the calibration procedure to be necessary to meet the limit requirement, was applied to the injection probe while monitoring the induced power with a spectrum analyzer.
3. The required frequency range (e.g., 10kHz – 100kHz, 1MHz – 5MHz), was scanned while maintaining the forward power level at the calibration level previously determined.
4. Whenever errors occurred, the applied signal was reduced, then the test was repeated in an attempt to establish a threshold at which the errors occurred for the artifact.

The injection probe was placed around the following conductors during their respective tests:
1. Artifact power cable, for the power line tests;
2. Analog input line to the ADC, for the analog signal line tests;
3. The ribbon connector carrying the datalines, for the digital line tests.

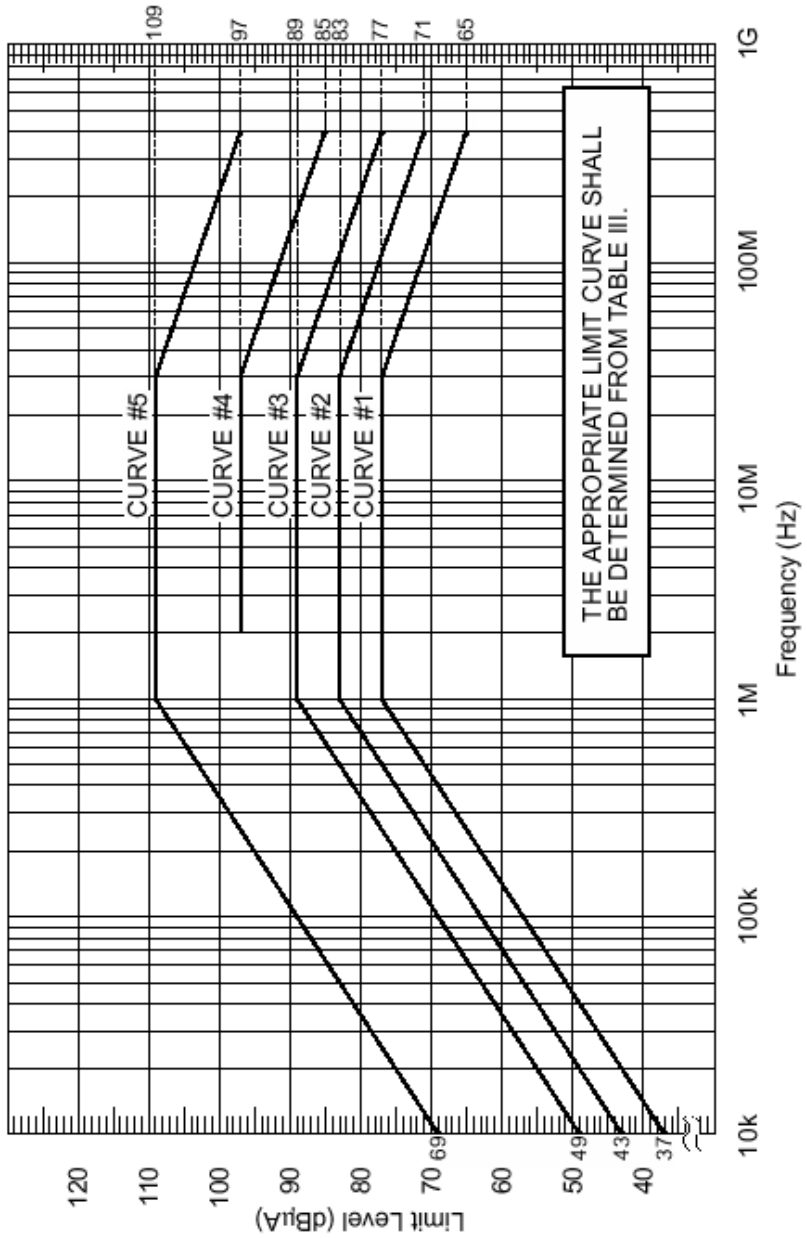


Fig. 2.6. CS114 calibration limit for all applications (MIL-STD-461D)

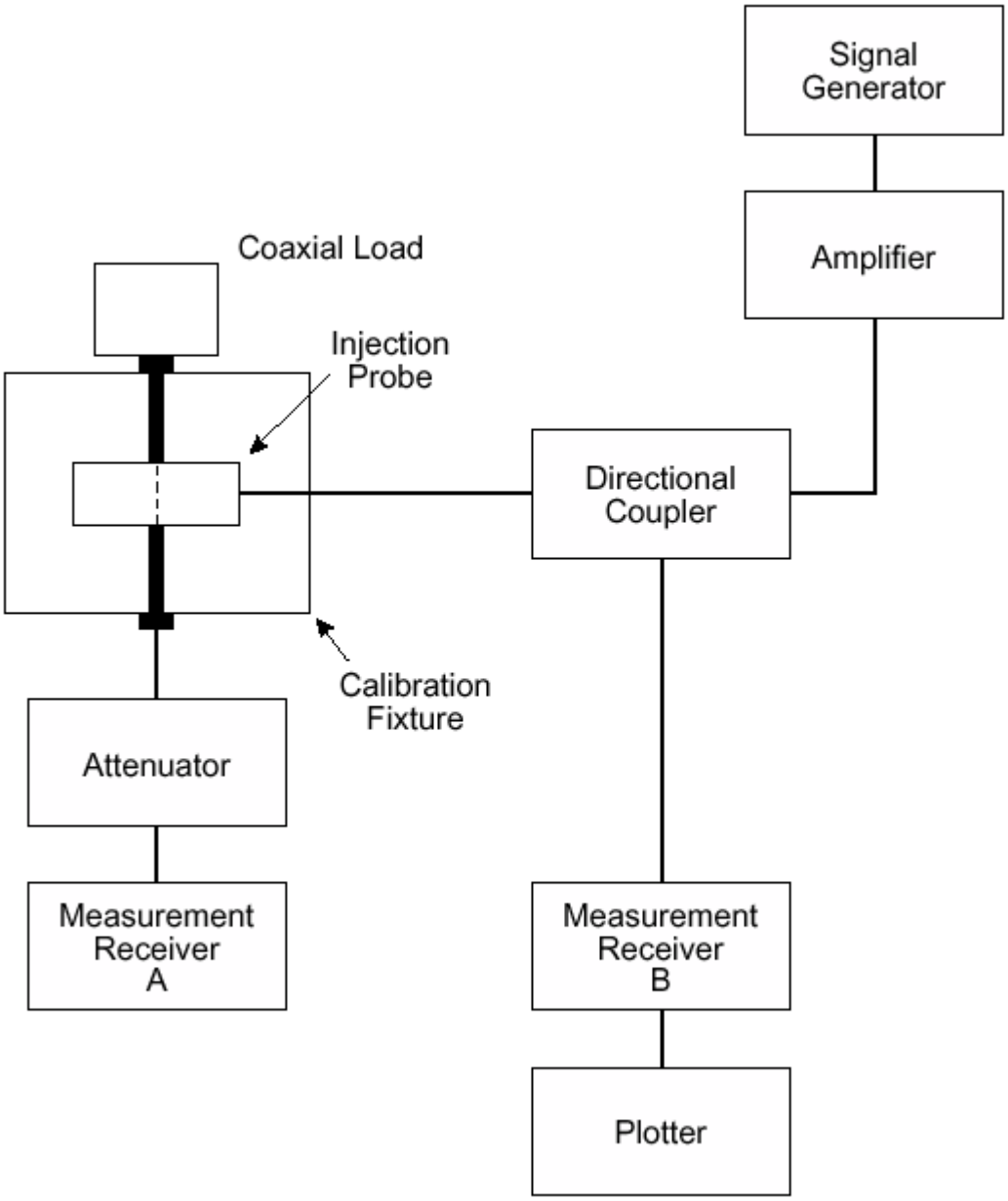


Fig. 2.7. CS114 Calibration setup

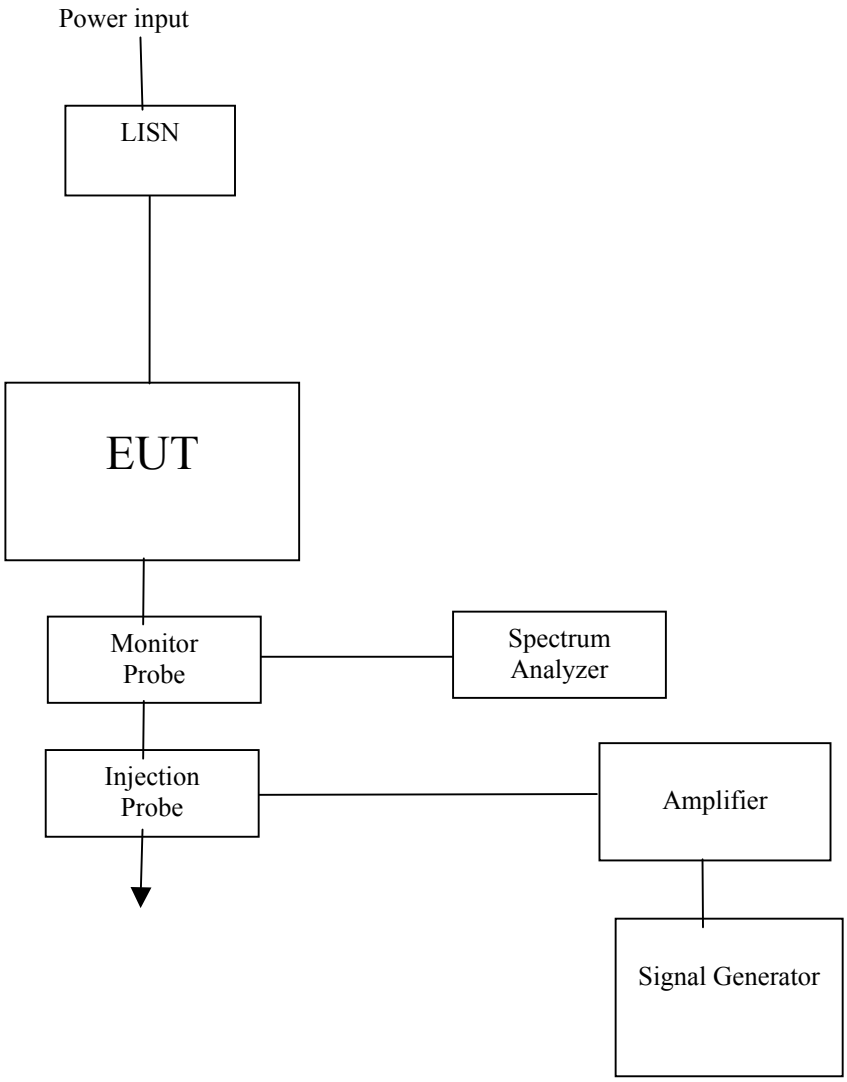


Fig. 2.8 CS114 Test setup

2.5 CS114 TEST RESULTS

Table 2.2. CS114 test results: power line

Sweep Frequency	SG settings (dBm)	SA reading (dBm)	Errors	SA reading (dBμV)	SA reading (dBμA)
10 – 100 kHz	-41	0 to -15	No	107 to 92	73 to 58
10 – 100 kHz	-38	3 to -12	Yes	110 to 95	76 to 61
100 kHz – 1 MHz	-54	-7 to -11	No	100 to 96	66 to 62
100 kHz – 1 MHz	-51	-4 to -7	Yes	103 to 100	69 to 66
1 – 5 MHz	-54	-4 to -30	No	103 to 77	69 to 43
1 – 5 MHz	-51	-1 to -27	Yes	106 to 80	72 to 46
5 – 30 MHz	-45	-1 to -29	No	106 to 78	72 to 44
5 – 30 MHz	-42	2 to -26	Yes	109 to 81	75 to 47
30 – 100 MHz	-36	5 to -29	No	112 to 78	78 to 44
30 – 100 MHz	-33	2 to -26	Yes	109 to 81	75 to 47
100 – 200 MHz	-30	10 to -4	No	117 to 103	83 to 69
100 – 200 MHz	-27	13 to -1	Yes	120 to 106	86 to 72
200 – 400 MHz	-27	14 to -37	No	121 to 70	87 to 36
200 – 400 MHz	-24	17 to -34	Yes	124 to 73	90 to 39

SG = Signal Generator
SA = Spectrum Analyzer

Table 2.3. CS114 test results: analog signal line

Sweep Frequency	SG settings (dBm)	SA reading (dBm)	Errors	SA reading (dBμV)	SA reading (dBμA)
10 – 100 kHz	-50	-7 to –24	No	100 to 83	66 to 49
10 – 100 kHz	-47	-5 to -21	Yes	102 to 86	68 to 52
100 kHz – 1 MHz	-59	-6 to -15	No	101 to 92	67 to 58
100 kHz – 1 MHz	-56	-2 to -12	Yes	105 to 95	71 to 61
1 – 5 MHz	-59	-8 to -22	No	99 to 85	65 to 51
1 – 5 MHz	-56	-4 to -18	Yes	103 to 89	69 to 55
5 – 30 MHz	-47	-12 to -24	No	95 to 83	61 to 49
5 – 30 MHz	-44	-8 to -21	Yes	99 to 86	65 to 52
30 – 100 MHz	-41	-2 to -23	No	105 to 84	71 to 50
30 – 100 MHz	-38	2 to -19	Yes	109 to 88	75 to 54
100 – 200 MHz	-41	-4 to -21	No	103 to 86	69 to 52
100 – 200 MHz	-38	-2 to –17	Yes	105 to 90	71 to 56
200 – 400 MHz	-26	-1 to -10	No	106 to 97	72 to 63
200 – 400 MHz	-23	1 to -7	Yes	108 to 100	74 to 66

SG = Signal Generator
SA = Spectrum Analyzer

Table 2.4. CS114 test results: digital signal line

Sweep Frequency	SG settings (dBm)	SA reading (dBm)	Errors	SA reading (dBμV)	SA reading (dBμA)
10 – 100 kHz	-38	5 to -10	No	112 to 97	78 to 63
10 – 100 kHz	-35	8 to -11	Yes	115 to 96	81 to 62
100 kHz – 1 MHz	-50	3 to -4	No	110 to 103	76 to 69
100 kHz – 1 MHz	-47	6 to -2	Yes	113 to 105	79 to 71
1 – 5 MHz	-53	-1 to -17	No	106 to 90	72 to 56
1 – 5 MHz	-50	1 to -14	Yes	108 to 93	74 to 59
5 – 30 MHz	-44	-4 to -20	No	103 to 87	69 to 53
5 – 30 MHz	-41	1 to -15	Yes	108 to 92	74 to 58
30 – 100 MHz	-35	6 to -8	No	113 to 99	79 to 65
30 – 100 MHz	-32	10 to -10	Yes	117 to 97	83 to 63
100 – 200 MHz	-38	4 to -3	No	111 to 104	77 to 70
100 – 200 MHz	-35	7 to 0	Yes	114 to 107	80 to 73
200 – 400 MHz	-26	-3 to -10	No	104 to 97	70 to 63
200 – 400 MHz	-23	0 to -3	Yes	107 to 104	73 to 70

SG = Signal Generator
SA = Spectrum Analyzer

2.6 CS115 (CONDUCTED SUSCEPTIBILITY, BULK CABLE INJECTION, IMPULSE EXCITATION) TEST SUMMARY

This test is used to verify the ability of the EUT to withstand impulse signals coupled onto EUT associated cabling, including all electrical (analog or digital) cables interfacing with the EUT enclosures.

The EUT should not exhibit any malfunction or degradation of performance beyond specified operational tolerances when subjected to a calibrated test signal as specified in MIL-STD-461D. (This specification is a 5 Amp, 30-ns pulse at a 30 Hz rate for one minute, as shown in Fig. 2.9.)

2.6.1 Artifact Test Procedure for CS115

The injection probe was first calibrated using the setup shown in Fig. 2.10. The pulse generator was adjusted for the specified rise time, width, and repetition rate requirements. The signal was then increased in steps and for each step, the current flowing in the calibration fixture was calculated by noting the oscilloscope voltage reading and taking into account the value of the attenuator connected between the calibration fixture and the oscilloscope. Readings were taken at current steps as shown in Table 2.5 until the oscilloscope indicated that MIL-STD-specified current was flowing in the center conductor of the calibration fixture. This calibration data would later be used to determine the current value at which the EUT might fail.

Actual testing of the Artifact was performed in accordance with MIL-STD-462D (1993) (see Fig 2.11). The test signal was started at a much lower level than the MIL-STD requirement, then gradually increased in steps. At each step, the performance of the Artifact was monitored for about 30 s, as indicated in the general test procedure (section 2.1). If there were no errors, the signal was increased by a predetermined amount. This was continued until either errors occurred or the maximum MIL-STD-specified current was reached.

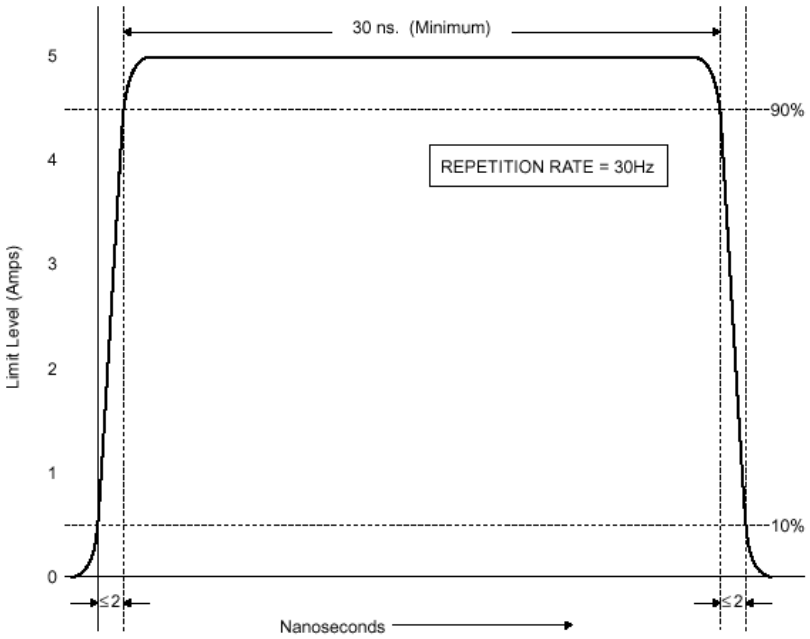


Fig. 2.9. CS115 calibrated signal source characteristics for all applications.

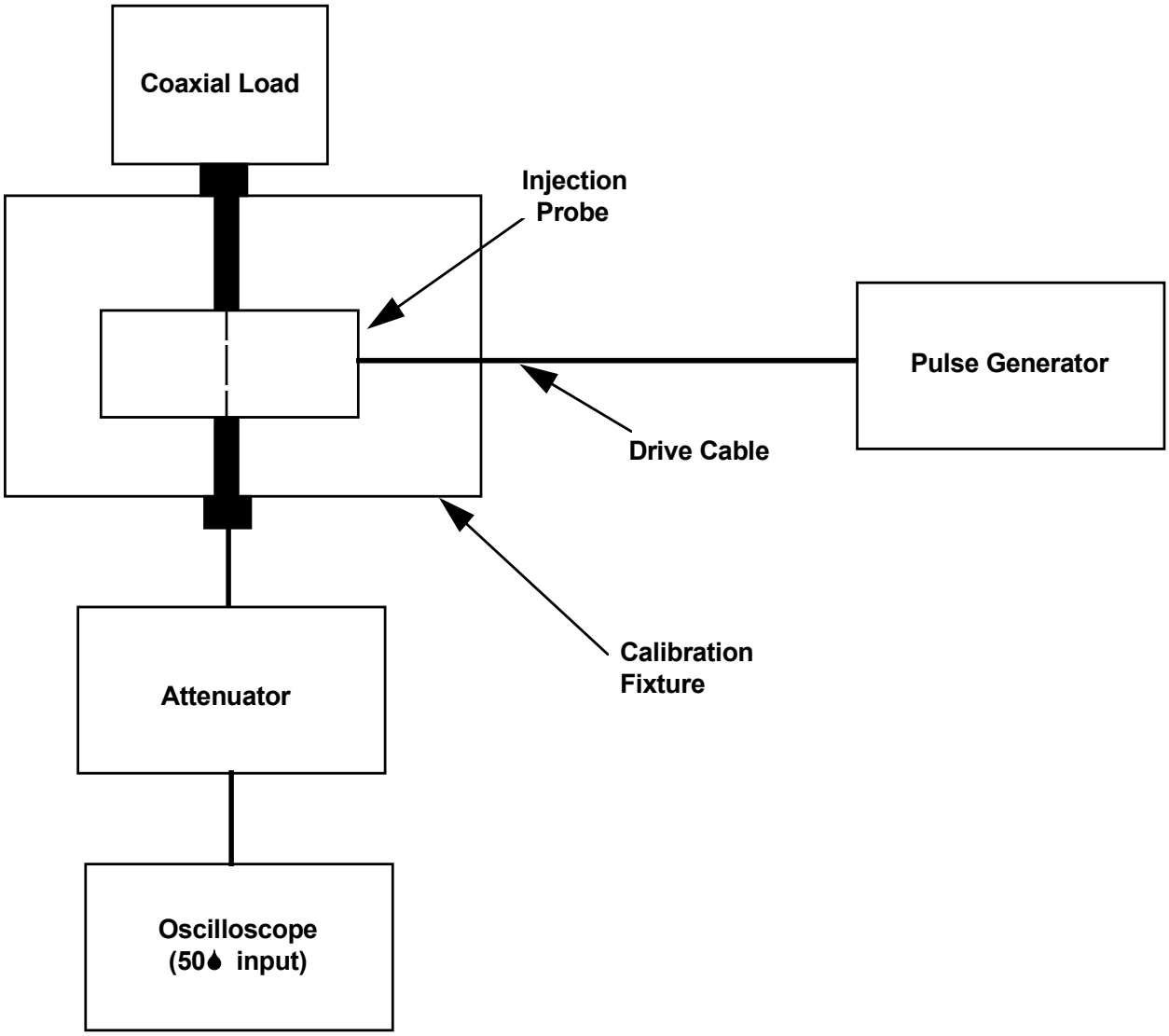


Fig. 2.10 CS115 calibration setup

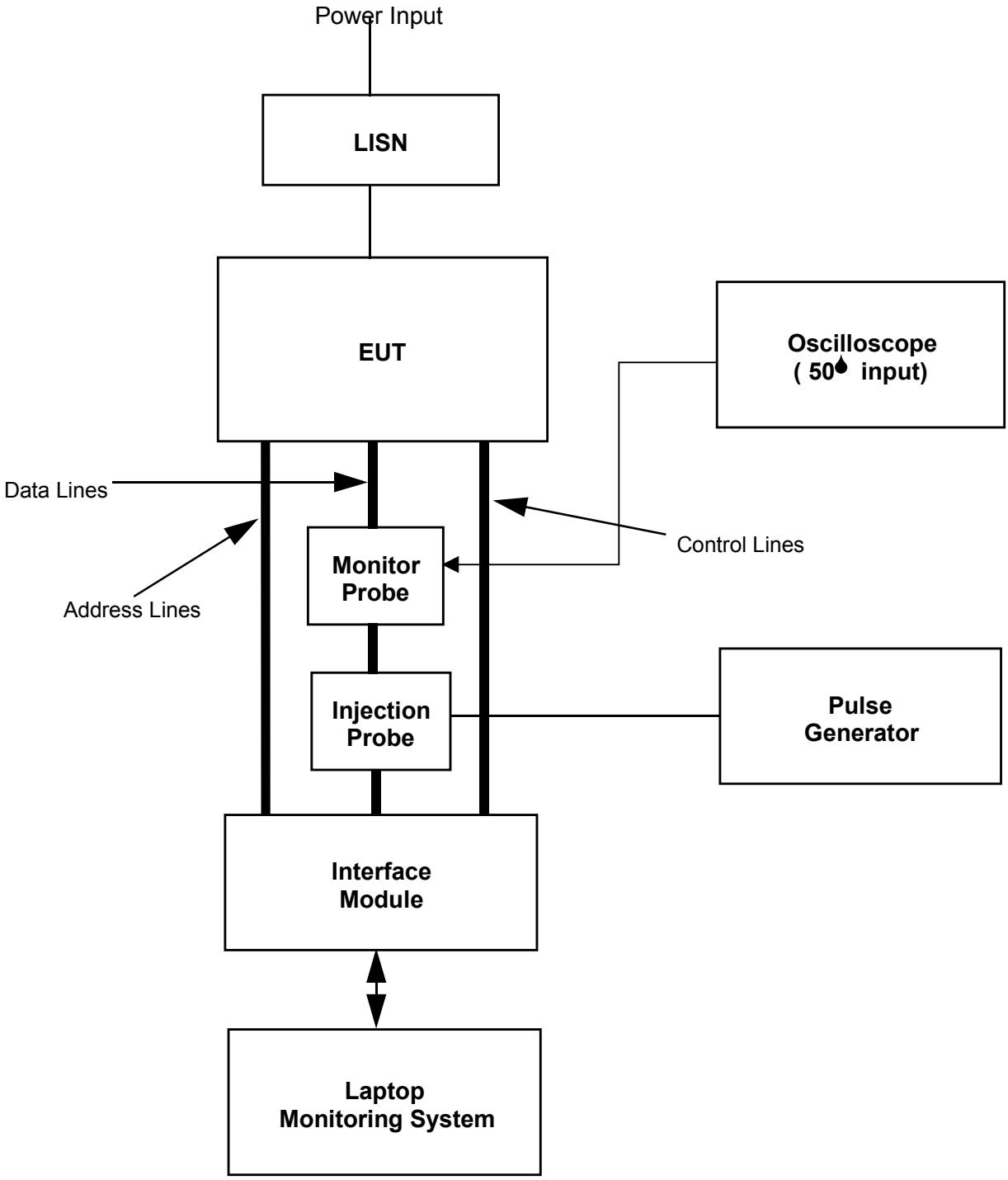


Fig. 2.11 CS115 Bulk cable injection test setup

2.7 CS115 TEST RESULTS

Table 2.5. CS 115 calibration settings for pulse generator

Current in Calibration Fixture (Amps)	Scope Reading (peak volts)	Pule Generator Charge Voltage (Volts)	Pulse Frequency (pps)
5.0	2.5	+918	30
4.5	2.25	+819	30
4.0	2.0	+750	30
3.5	1.75	+632	30
3.0	1.5	+551	30
2.5	1.25	+456	30
2.0	1.0	+382	30
1.5	0.75	+277	30
1.0	0.5	+186	30
0.5	0.25	+98	30

Table 2.6. CS115 test results: power line

Scope reading at which errors occurred (peak volts)	Pulse generator charge voltage (peak volts)	Equivalent current into 50 Ω (Amps)
0.800	89	1.6
-1.2	128	-2.4

Table 2.7 CS115 test results: analog signal line

Scope Reading at which Errors Occurred (peak volts)	Pulse generator charge voltage (peak volts)	Equivalent current into 50 Ω (Amps)
2.0	240	4.0
-1.8	221	3.6

Table 2.8 CS115 test results: digital signal line

Scope Reading at which Errors Occurred (peak volts)	Pulse generator charge voltage (peak volts)	Equivalent current into 50 Ω (Amps)
0.9	71	1.8
-0.6	38	-1.2

2.8 CS116 (CONDUCTED SUSCEPTIBILITY. DAMPED SINUSOIDAL TRANSIENTS, CABLES AND POWER LEADS, 10 kHz to 100 MHz) TEST SUMMARY

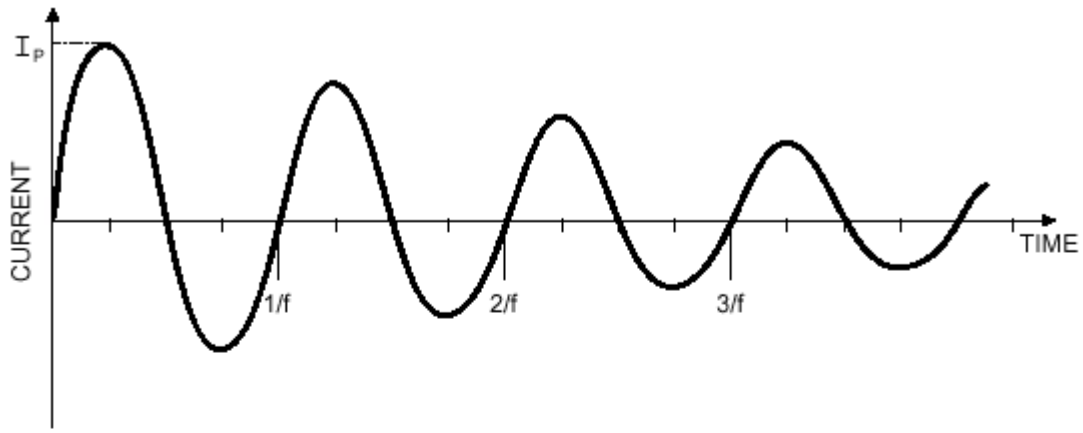
This test is used to verify the ability of the EUT to withstand damped sinusoidal transients coupled onto EUT associated cables and power leads.

The test criterion was that the EUT would not exhibit any malfunction or degradation of performance beyond the preset operational tolerances when subjected to the test signal as specified in MIL-STD-461D. This specification is as shown in Fig. 2.12. The test limit is shown in Fig. 2.13.

2.8.1 Artifact Test Procedure for CS116

The injection probe was first calibrated using the setup shown in Fig. 2.14. Initially, the frequency of the damped sine generator was set to 10 kHz, and the amplitude of the damped sine generator output was adjusted to the level required (Fig. 2.13), as indicated by the oscilloscope reading. The damped sine generator setting was recorded. These steps were repeated for each frequency specified in MIL-STD-461.

Actual testing of the Artifact was performed in accordance with MIL-STD-462D (1993) (see Fig 2.15). The frequency of the test signal was initially set to 10 kHz. The output level of the signal generator was then increased slowly to the required current level as specified by MIL-STD-461. The test signal was maintained at this level and monitoring of the Artifact performance was continued for at least 30s. If there were no errors, the test frequency was increased to the next value and the monitoring was repeated. The results of the tests are shown in Tables 2.9 through 2.12.



NOTES: 1. Normalized waveform: $e^{-(\pi f t)/Q} \sin(2\pi f t)$

Where:
f = Test frequency (Hz)
t = Time (sec)
Q = Damping factor, 15 ± 5

2. Damping factor (Q) shall be determined as follows:

$$Q = \frac{\pi(N - 1)}{\ln(I_P/I_N)}$$

Where:
Q = Damping factor
N = Cycle number (i.e. N = 2, 3, 4, 5,...)
I_P = Peak current at 1st cycle
I_N = Peak current at Nth cycle
ln = Natural log

Fig. 2.12. Typical CS116 damped sinusoidal waveform (see Fig. 2.13 for the value of I_p).

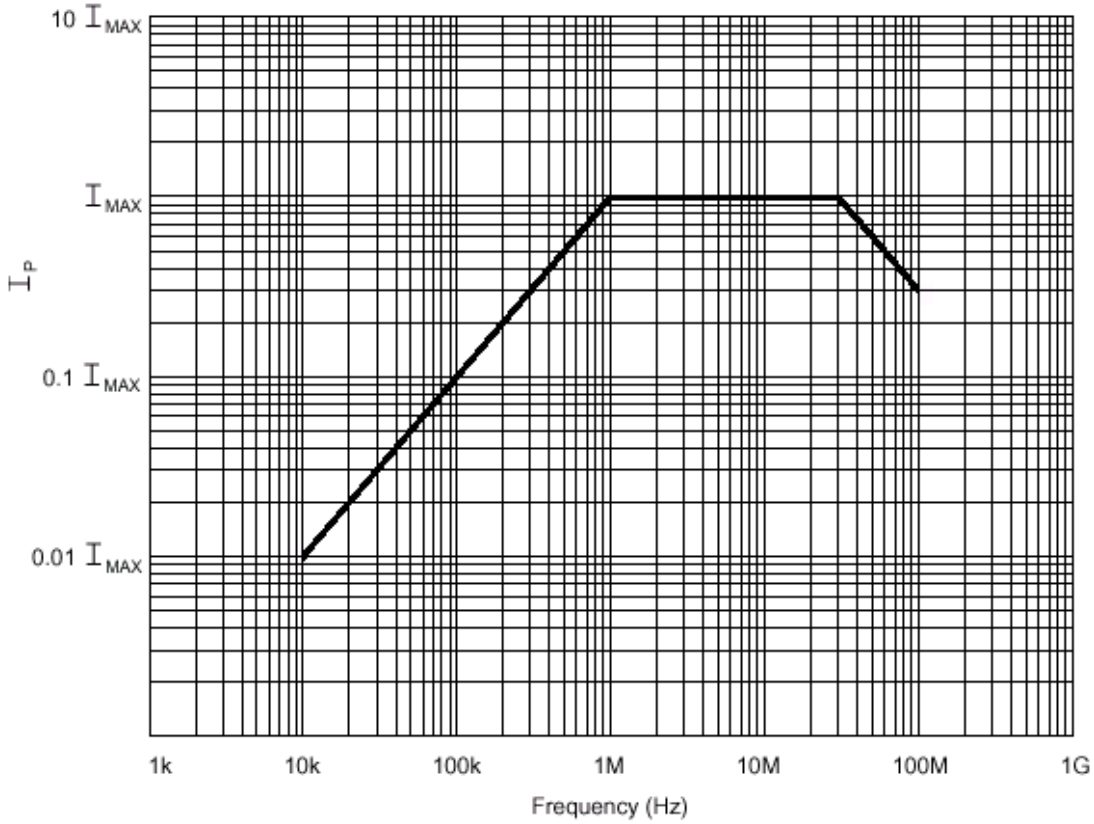


Fig. 2.13. CS116 limit for all military applications (NOTE: I_{max} = 10 amps for army and navy, and I_{max} = 5 amps for the Air Force. For the Artifact tests, I_{max} of 10 amps was used).

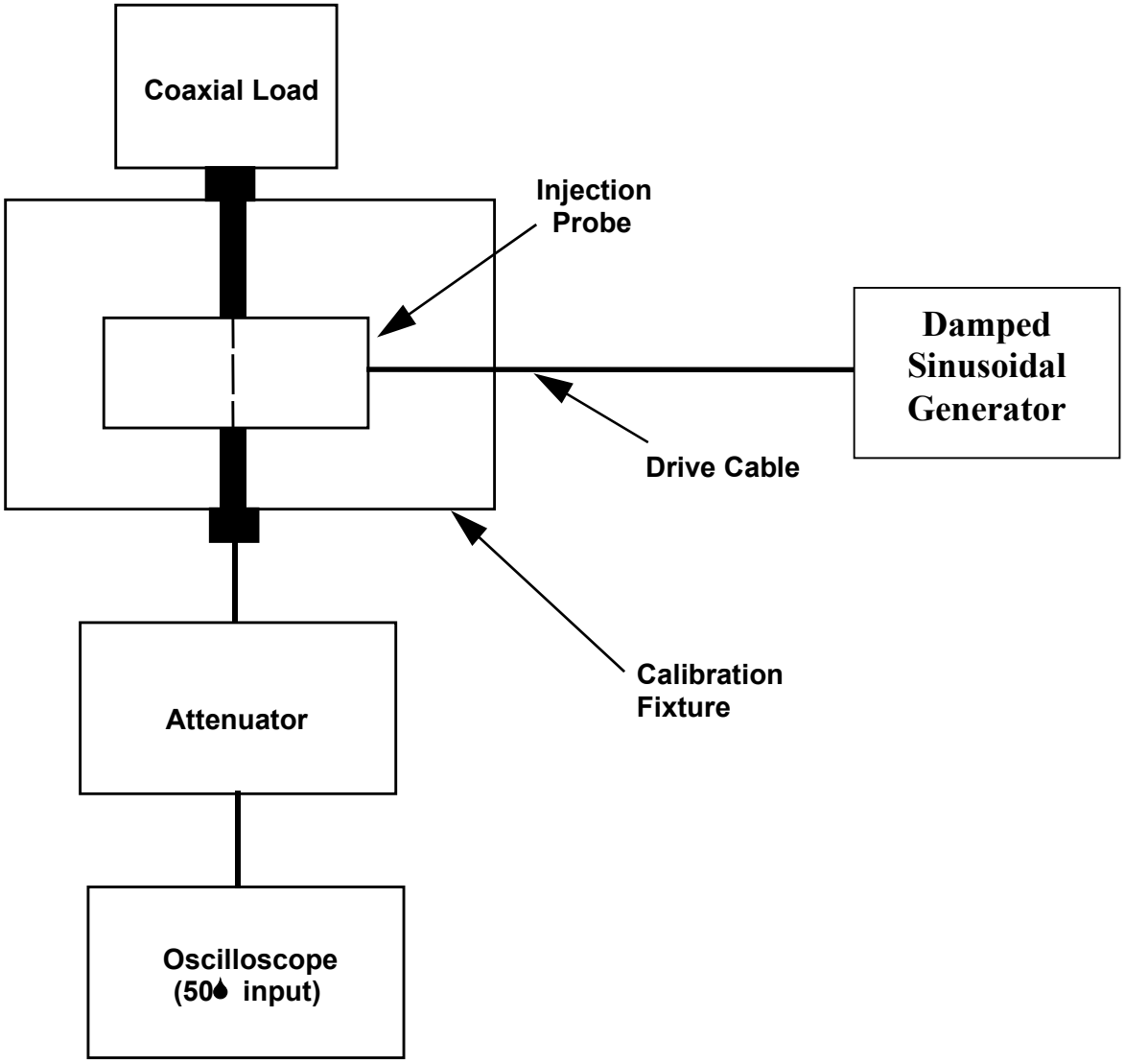


Fig. 2.14 CS116 calibration setup

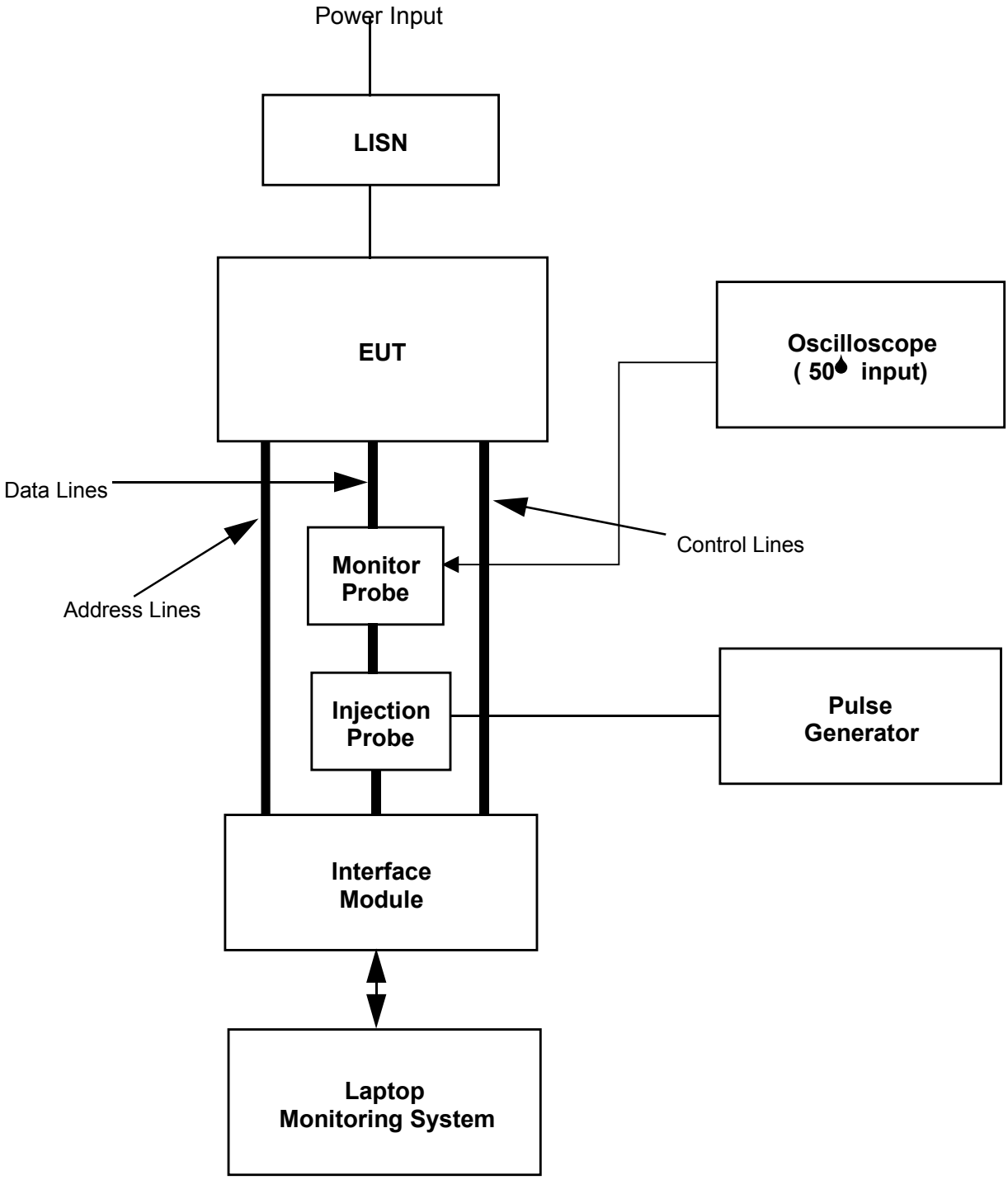


Fig. 2.15. CS116 test setup

2.9 CS116 TEST RESULTS

Table 2.9 CS116 calibration settings for signal generator

Frequency	Calibration Fixture Peak Current (Amps)	Voltage (peak volts)	Generator Setting (Percent of Full Scale Amplitude)
10 kHz	0.1	0.05	43
100kHz	1	0.5	31
1MHz	10	5.0	26
10MHz	10	5	37
30MHz	10	5	87
100MHz	3	1.5	88

Table 2.10. CS116 test results: analog signal line

Frequency	Scope reading (peak volts)	Signal Generator Amplitude Setting (Percent of Full Scale)	Equivalent current into 50Ω	Comments
10kHz	8	45	16	No errors (stopped)
100kHz	5.8	10	11.6	Errors
1MHz	1.4	2	2.8	Errors
10MHz	0.5	1	1.0	Errors
30MHz	0.5	10	1.0	Errors
100MHz	~0.7	95	1.4	Errors

Table 2.11. CS 116 test results: digital signal line.

Frequency	Scope Reading (peak volts)	Signal Generator Amplitude Setting (Percent of Full Scale)	Equivalent current into 50Ω	Comments
10kHz	5.0	57	10	No errors (stopped)
100kHz	4.0	56	8	No errors (stopped)
1MHz	0.8	48	1.6	Errors
10MHz	0.3	<1	0.6	Errors
30MHz	0.17	<2	0.4	Errors
100MHz	~1.4	92	2.8	Errors

Table 2.12. CS116 test results: power line

Frequency	Scope Reading (peak volts)	Signal Generator Amplitude Setting (Percent of Full Scale)	Equivalent current into 50Ω	Comments
10kHz	3.8	62	7.6	No errors (stopped)
100kHz	3.4	~9	6.8	No errors
1MHz	1.4	<1	2.8	Errors
10MHz	2.0	~10	4.0	Errors
30MHz	1.0	25	2.0	Errors
100MHz	0.8	Max	1.6	Errors

2.10 IEC 61000-4-4 (IMMUNITY TO ELECTRICAL FAST TRANSIENT/BURST) TEST SUMMARY

This test is used to verify the ability of the EUT to withstand electrical fast transient bursts such as those originating from switching transients (interruption of inductive loads, relay contact bounce, etc.). Significant for the test are the short rise time, the repetition rate and the low energy of the transients.

2.10.1 Artifact Test Procedure for IEC 61000-4-4

The test was set up in accordance with specifications stipulated in section 7 of IEC 61000-4-4 (see also Fig. 2.16). A capacitive coupling clamp (section 7.2.2 of EN 61000-4-4) was used for coupling the transient burst voltage to the analog and digital lines.

The Electrical Fast Transient/Burst (EFT/B) generator were set in accordance with IEC 61000-4-4, namely:

- Rise time of pulses: 5ns ∀ 30%
- Impulse duration (50% value): 50 ns∀ 30%

The repetition rate of the impulses and peak values of the output voltages for the various levels of application are as shown in Table 2.13. The general graph of a fast transient burst generator is shown in Fig. 2.17, while the waveshape of a single pulse into a 50Ω load is shown in Fig. 2.18.

Table 2.13. Test levels specified in IEC 61000-4-4

Open-circuit output test voltage (∀ 10%) and repetition rate of the impulse (∀ 20%)				
Level	**On power supply port**		**On input/output (I/O) signal, data and control ports**	
	Voltage peak (kV)	**Repetition rate (kHz)**	**Voltage peak (kV)**	**Repetition rate (kHz)**
1	0.5	5	0.25	5
2	1	5	0.5	5
3	2	5	1	5
4	4	2.5	2	5
X[1]	Special	Special	Special	Special
[1] "X" is an open level. The level has to be specified in the dedicated equipment specification.				

Note from the table that, for testing I/O, signal and data, EUT's ports use half the test voltage values applied on power supply ports. Also, the various levels in the table have designations as follows:

Level 1: Well-protected environment
Level 2: Protected environment
Level 3: Typical industrial environment
Level 4: Severe industrial environment
Level 5: Special situations to be analyzed.

The tests documented in this report were performed to the level 1 (representative of the computer room) environment. This level has the following attributes:

- Suppression of all EFT/B in the switched power supply and control circuits:

- Separation between power supply lines (a.c. and DC.) and control and measurement circuits coming from other environments belonging to higher severity levels:
- Shielded power supply cables with the screens earthed at both ends on the reference ground of the installation, and power supply protection by filtering.

The level 1 testing environment was chosen because it is typical of the environment in which microprocessor-based instrumentation in nuclear power plants are likely to be placed.

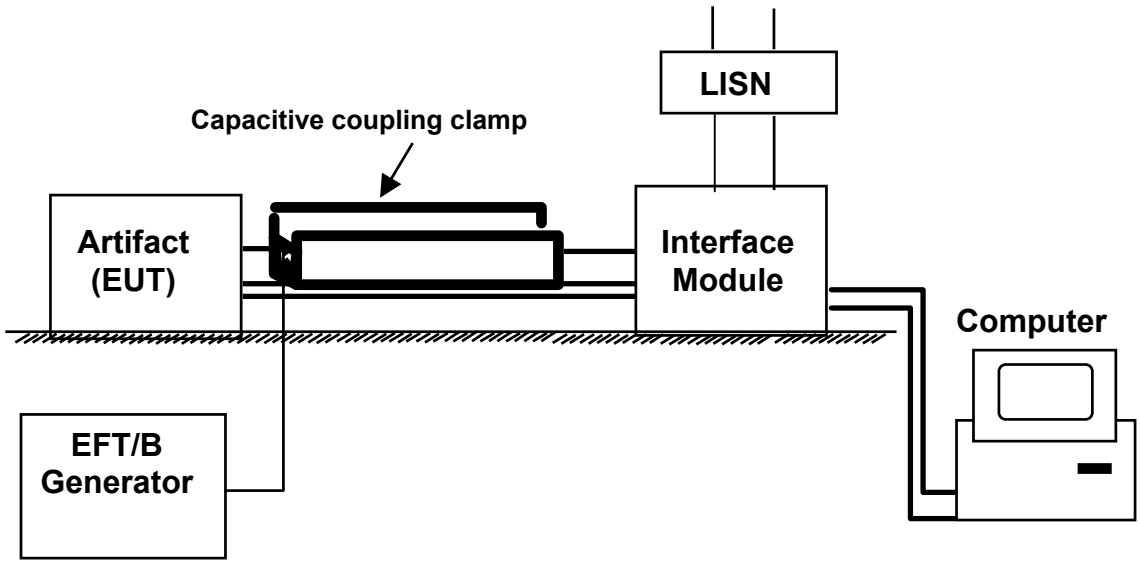


Fig. 2.16. Simplified diagram of setup for IEC 61000-4-4 test.

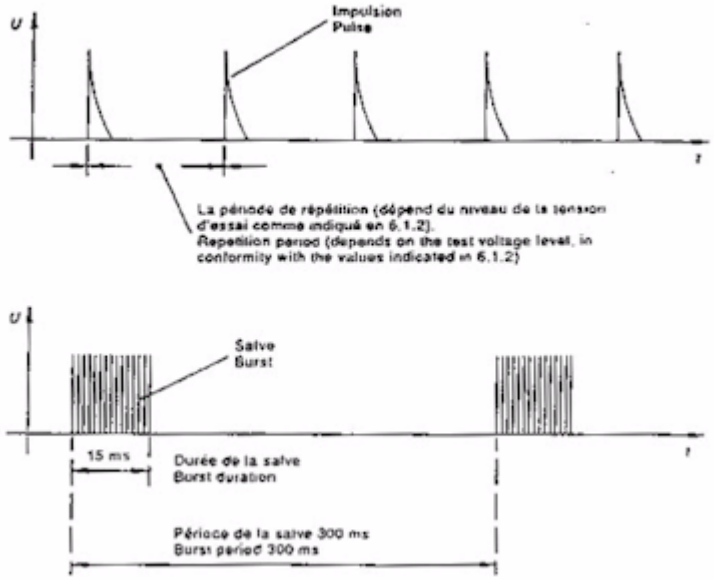


Fig. 2.17. General graph of a fast transient burst.

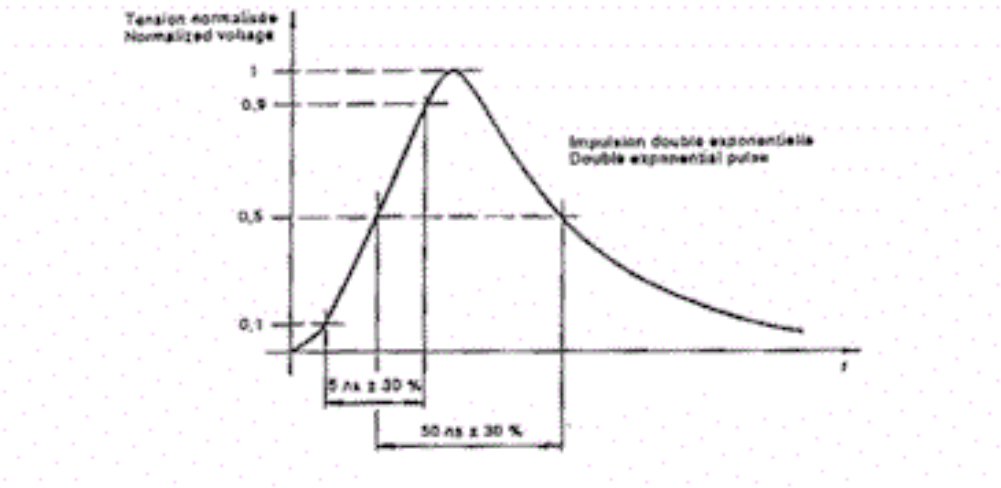


Fig. 2.18. Waveshape of a single pulse into a 50Ω load.

2.10.2 IEC 61000-4-4 Test Results

The IEC 61000-4-4 test results are shown in Tables 2.14 through 2.18.

Table 2.14. IEC 61000-4-4 test results: analog line

Peak voltage (kV)		Comments
Positive polarity	Negative polarity	
0.22	0.22	No errors
0.25	0.25	No errors

Table 2.15. IEC 61000-4-4 test results: digital line

Peak voltage (kV)		Comments
Positive polarity	Negative polarity	
0.22	0.22	No errors
0.25	0.25	No errors

Table 2.16. IEC 61000-4-4 test results: power line—line to ground

Positive polarity peak voltage (kV)	Negative polarity peak voltage (kV)
0.22 (no errors)	0.22 (no errors)
0.25 (no errors)	0.25 (no errors)

Table 2.17. IEC 61000-4-4 test results: power line—neutral to ground

Positive polarity peak voltage (kV)	Negative polarity peak voltage (kV)
0.22 (no errors)	0.22 (no errors)
0.25 (no errors)	0.25 (no errors)

Table 2.18. IEC 61000-4-4 test results: power line—line to neutral

Positive polarity peak voltage (kV)	Negative polarity peak voltage (kV)
0.22 (no errors)	0.22 (no errors)
0.25 (no errors)	0.25 (no errors)

2.11 IEC 61000-4-5 (SURGE IMMUNITY) TEST SUMMARY

This test is used to verify the ability of the EUT to withstand unidirectional surges caused by overvoltages from switching and lightning transients.

2.11.1 Artifact Test Procedure for IEC 61000-4-5

The test was set up as shown in Fig. 2.19. (The figure shows the actual setup for the digital line tests). The point marked "A" in the figure represents the ribbon connector for all the 8-bit data lines, while "B" represents just one of the 8-bit lines. [For the digital lines tests, the data lines (coming off of one ribbon connector) were spliced apart to make it easier to connect the combination wave generator].
The output characteristics of the combination wave (shown in Figs. 2.20 and 2.21) generator were set in accordance with IEC 61000-4-5, section 6.1.1.

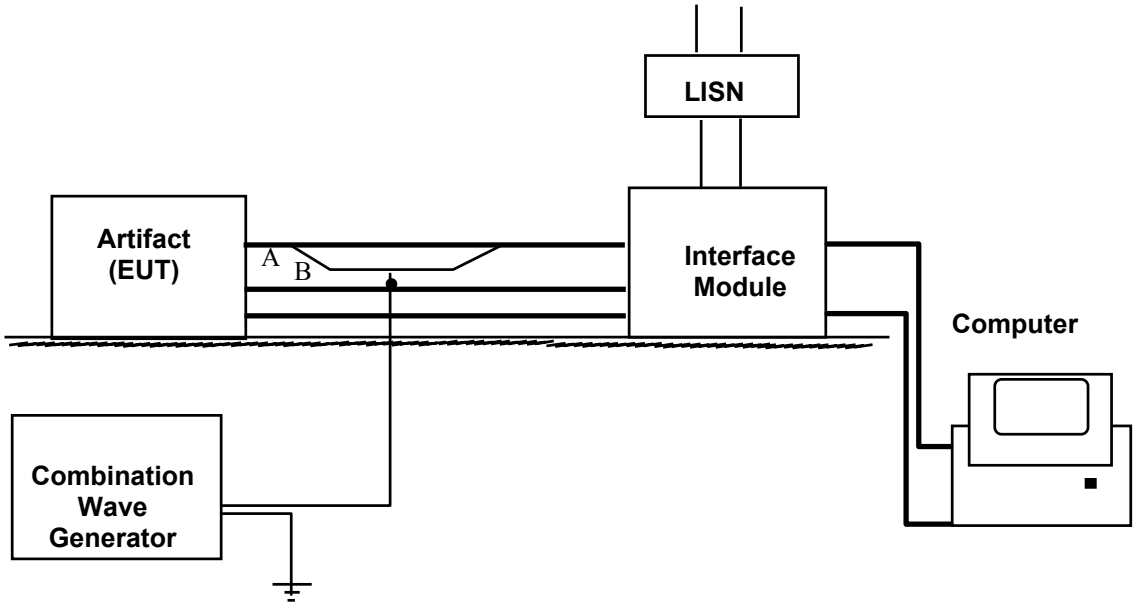


Fig. 2.19. Setup for IEC 61000-4-5 test (see text for points marked A and B).

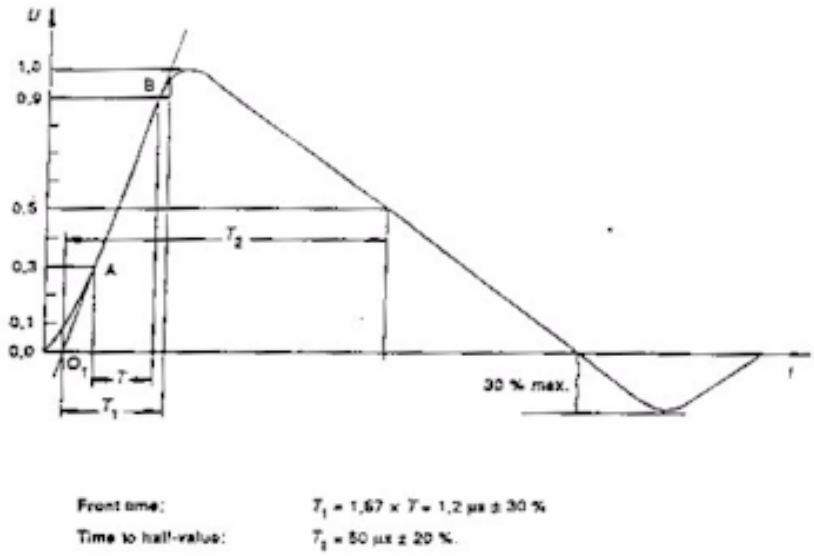


Fig. 2.20. Waveform of open-circuit voltage.

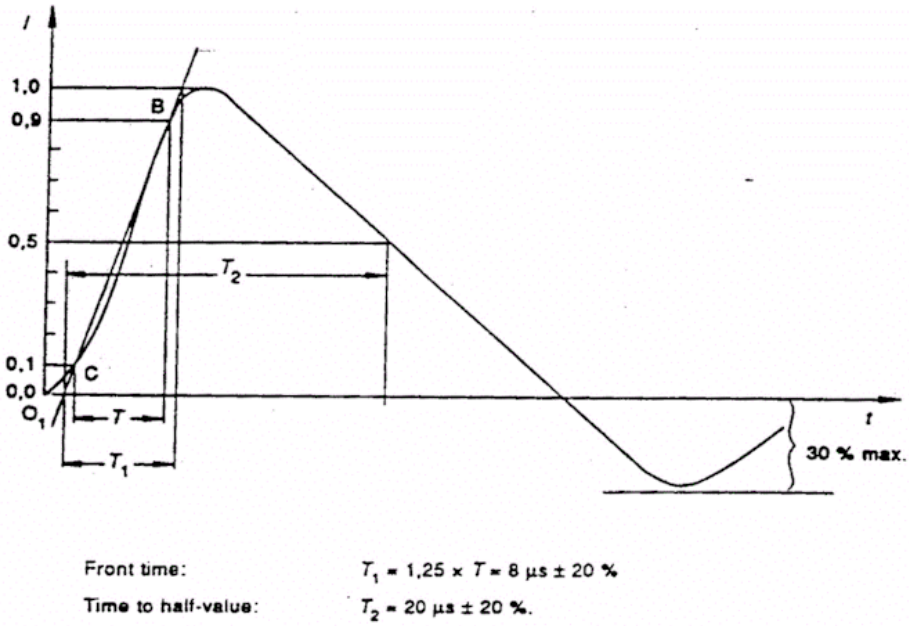


Fig. 2.21. Waveform of short-circuit current.

As for IEC 61000-4-4, IEC 61000-4-5 allows testing to various levels (Table 2.19), depending on the installation conditions of the equipment. Classes of installation conditions are given in B.3 of annex B of IEC 61000-4-5.

Table 2.19. Test levels for IEC 61000-4-5.

Level	Open-circuit test voltage (∀ 10 %), kV
1	0.5
2	1.0
3	2.0
4	4.0
5	Special

2.12 IEC 61000-4-5 TEST RESULTS

Table 2.20. IEC 61000-4-5 power line test results [peak voltage (kV)]

0^B phase	Comments	90^B phase	Comments	270^B phase	Comments
Positive polarity (line to ground)					
+3.0	No errors	+3.0	No errors	+3.0	No errors
Negative polarity (line to ground)					
-3.0	No errors	-3.0	No errors	-3.0	No errors
Positive polarity (neutral to ground)					
+3.0	No errors	+3.0	No errors	+3.0	No errors
Negative polarity (neutral to ground)					
-3.0	No errors	-3.0	No errors	-3.0	No errors
Positive polarity (line to neutral)					
+3.0	No errors	+3.0	No errors	+3.0	No errors
Negative polarity (line to neutral)					
-3.0	No errors	-3.0	No errors	-3.0	No errors

2.13 IEC 61000-4-6 (RADIO-FREQUENCY FIELD-INDUCED CONDUCTED DISTURBANCES) TEST SUMMARY

This test is used to verify the ability of the EUT to withstand electromagnetic disturbances originating from intended radio-frequency (RF) transmitters in the frequency range 9 kHz up to 80 MHz.

2.13.1 Artifact Test Procedure for IEC 61000-4-6

A simplified diagram of the test setup is shown in Fig. 2.22. The RF signal generator used as the test equipment had a bandwidth of 100 MHz, and was amplitude-modulated by a 1 kHz sine wave with a modulation depth of 80%. The modulated and unmodulated waveforms as specified in IEC 61000-4-6 are shown in Fig. 2.23.

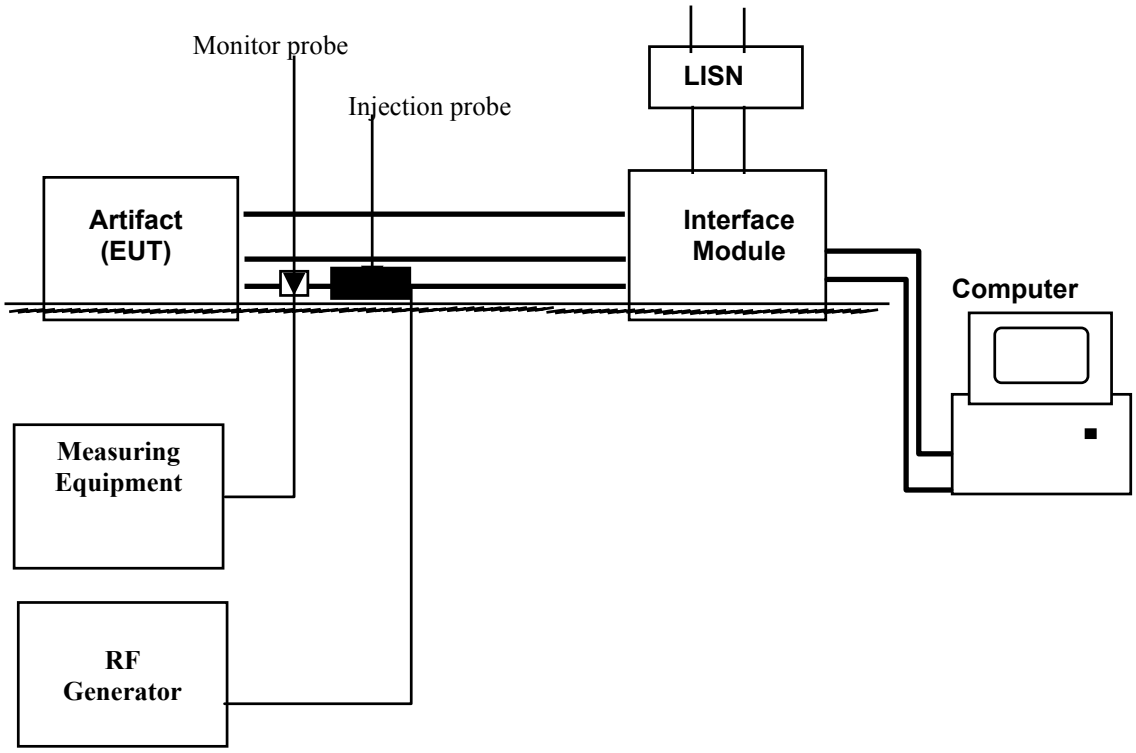


Fig. 2.22. Setup for IEC 61000-4-6 test.

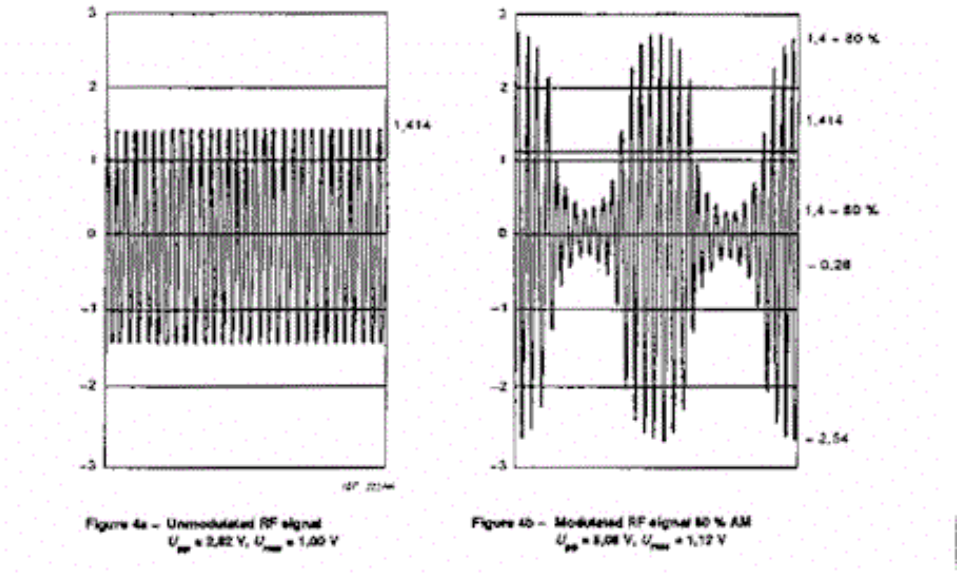


Fig. 2.23. Definition of wave shapes occurring at the output of the EUT port of the coupling device.

2.13.2 IEC 61000-4-6 Test Results

Table 2.21. IEC 61000-4-6 test results: digital signal line

Sweep Frequency	Signal Generator setting (dBm)	Spectrum Analyzer Reading dBm)	Errors	Spectrum Analyzer reading (DbμV)
150 kHz – 1 MHz	-50	2 to -2	No	109 to 105
150kHz – 1 MHz	-47	4 to -1	Yes	111 to 106
1 – 5 MHz	-50	1 to -10	No	108 to 97
1 – 5 MHz	-47	3 to -5	Yes	110 to 102
5 – 30 MHz	-41	-2 to -25	No	105 to 82
5 – 30 MHz	-38	1 to -16	Yes	108 to 91
30 – 80 MHz	-35	6 to -20	No	113 to 87
30 – 80 MHz	-32	9 to -16	Yes	116 to 91

Table 2.22. IEC 61000-4-6 test results: analog signal line

Sweep Frequency	Signal Generator setting (dBm)	Spectrum Analyzer Reading dBm)	Errors	Spectrum Analyzer reading (DbμV)
150 kHz – 1 MHz	-65	-9 to –14	No	98 to 93
150kHz – 1 MHz	-62	-5 to –11	Yes	102 to 96
1 – 5 MHz	-62	-7 to –18	No	100 to 89
1 – 5 MHz	-59	-4 to –16	Yes	103 to 91
5 – 30 MHz	-47	-8 to –34	No	99 to 73
5 – 30 MHz	-44	-6 to –27	Yes	101 to 80
30 – 80 MHz	-44	-3 to –28	No	104 to 79
30 – 80 MHz	-41	-1 to –26	Yes	106 to 81

Table 2.23. IEC 61000-4-6 test results: power line

Sweep Frequency	Signal Generator setting (dBm)	Spectrum Analyzer Reading dBm)	Errors	Spectrum Analyzer reading (DbμV)
150 kHz – 1 MHz	-51	0 to -3	No	107 to 104
150kHz – 1 MHz	-48	3 to –1	Yes	110 to 106
1 – 5 MHz	-57	-1 to –20	No	106 to 87
1 – 5 MHz	-54	2 to –17	Yes	109 to 90
5 – 30 MHz	-42	0 to –25	No	107 to 82
5 – 30 MHz	-39	2 to –21	Yes	109 to 86
30 – 80 MHz	-30	12 to –11	No	119 to 96
30 – 80 MHz	-27	16 to -8	Yes	o 99

2.14 IEC 61000-4-12 (IMMUNITY TO OSCILLATORY WAVES) TEST SUMMARY

This test is used to verify the ability of the EUT to withstand oscillatory waves represented by:

a). Non-repetitive (single shot) damped oscillatory transients (known as "ring wave") in low voltage power, control and signal lines supplied by public and non-public networks. The ring wave occurs at the terminals of equipment as a consequence of switching in power and control lines, as well as a consequence of lightning.

b). Repetitive (burst) damped oscillatory transients (known as "damped oscillatory wave"). The damped oscillatory wave occurs at the terminals of equipment as a consequence of switching with restriking of the arc, typical of electrical plants, high voltage and medium voltage (HV/MV) stations, as well as of heavy industrial installations.

As in the case of the previous tests, various levels are specified for both types of tests. These levels are shown in Tables 2.24 and 2.25, and range from 250 V to 4 kV. The particular level an equipment is tested to depends on the applicability, for a given location or installation, of one or both of the causes considered in IEC 61000-4-12; namely, the *switching* of power and/or control circuits and the indirect effect of *lightning*.

A diagram of the test set up is shown in Fig. 2.24.

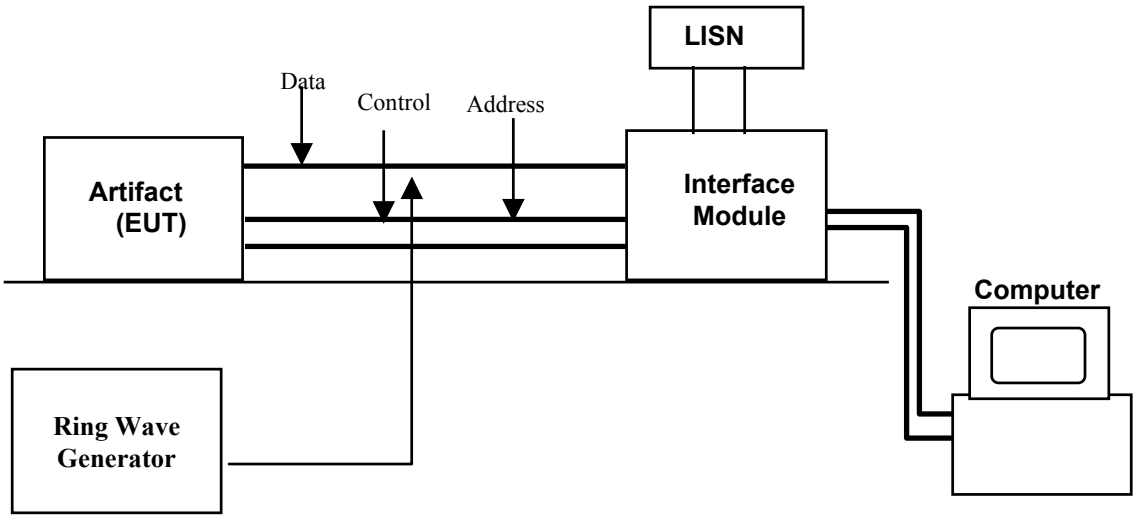


Fig. 2.24 Setup for IEC 61000-4-12 test.

2.14.1 Artifact Test Procedure for IEC 61000-4-12

Ring wave signals (Fig. 2.25) were used in this test of the artifact because they were judged to more closely resemble situations that could occur with microprocessor-based safety equipment (low power signal lines).

In general, five positive and five negative transients were applied. Each test set with identical polarity was applied at 30 sec. intervals. That is, the positive polarity test signals were applied 5 times at 30 sec intervals, and the negative polarity signals were also applied 5 times at 30 sec intervals. The tests were

first conducted by applying the test wave at random angles/phases (in 0.2 kV increments up to 4.0 kV). The tests were then repeated at phase angles of 0^B, 90^B, and 270^B at a test voltage of 4.0 kV only. Tables 2.26 and 2.27 show the results for random applications of the test signal. Tables 2.28 and 2.29 show the results of placing the test signal at particular phase values.

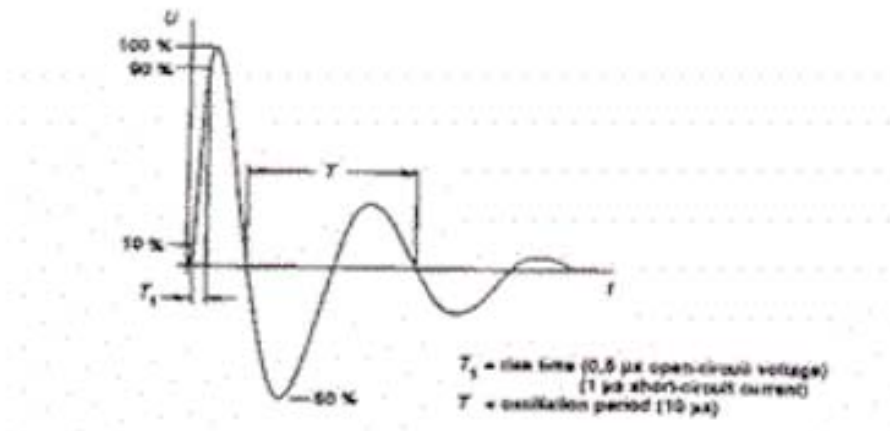


Fig. 2.25. Waveform of the ring wave.

Table 2.24. IEC 61000-4-12: Test levels for ring wave.

Level	Common mode (kV)	Differential mode (kV)
1	0.5	0.25
2	1.0	0.5
3	2.0	1,0
4	4.0	2.0
X[1]	X	X
[1]X is an open level. The level can be given in the product specification.		

Table 2.25: IEC 61000-4-12: Test levels for damped oscillatory wave (ring wave was used in this test).

Level	Common mode (kV)	Differential mode (kV)
1	0.5	0.25
2	1.0	0.5
3	2.0*	1.0
4	-	-
X[1]	X	X
[1]X is an open level. This level can be given in the product specification. *The value is increased to 2.5 kV for substation equipment.		

2.14.2 IEC 61000-4-12 Test Results

Table 2.26. IEC 61000-4-12 test results: power line—line to ground—random

Test voltage (kV)	Method of application of test signal	Polarity	Test results
0.2	Random	Positive	No errors
0.4	Random	Positive	No errors
0.6	Random	Positive	No errors
0.8	Random	Positive	No errors
1.0	Random	Positive	No errors
1.2	Random	Positive	No errors
1.4	Random	Positive	No errors
1.6	Random	Positive	No errors
1.8	Random	Positive	No errors
2.0	Random	Positive	No errors
2.2	Random	Positive	No errors
2.4	Random	Positive	No errors
2.6	Random	Positive	No errors
2.8	Random	Positive	No errors
3.0	Random	Positive	No errors
3.2	Random	Positive	No errors
3.4	Random	Positive	No errors
3.6	Random	Positive	No errors
3.8	Random	Positive	No errors
4.0	Random	Positive	No errors

Table 2.27. IEC 61000-4-12 test results: power line—line to line—random

Test voltage (kV)	Method of application of test signal	Polarity	Test results
0.2	Random	Positive	No errors
0.4	Random	Positive	No errors
0.6	Random	Positive	No errors
0.8	Random	Positive	No errors
1.0	Random	Positive	No errors
1.2	Random	Positive	No errors
1.4	Random	Positive	No errors
1.6	Random	Positive	No errors
1.8	Random	Positive	No errors
2.0	Random	Positive	No errors
2.2	Random	Positive	No errors
2.4	Random	Positive	No errors
2.6	Random	Positive	No errors
2.8	Random	Positive	No errors
3.0	Random	Positive	No errors
3.2	Random	Positive	No errors
3.4	Random	Positive	No errors
3.6	Random	Positive	No errors
3.8	Random	Positive	No errors
4.0	Random	Positive	No errors

Table 2.28. IEC 61000-4-12: Power line test results—line to line—phase

Test voltage (kV)	Application of test signal	Polarity	Test results
4.0	0^B phase	Positive	No errors
4.0	90^B phase	Positive	No errors
4.0	270^B phase	Positive	No errors
4.0	0^B phase	Negative	No errors
4.0	90^B phase	Negative	No errors
4.0	270^B phase	Negative	No errors

Table 2.29. IEC 61000-4-12: Power line test results—line to ground—phase

Test voltage (kV)	Application of test signal	Polarity	Test results
4.0	0^B phase	Positive	No errors
4.0	90^B phase	Positive	No errors
4.0	270^B phase	Positive	No errors
4.0	0^B phase	Negative	No errors
4.0	90^B phase	Negative	No errors
4.0	270^B phase	Negative	No errors

3 ANALYSIS OF TEST RESULTS

3.1 INTRODUCTION

The objectives of the tests reported in this document are to answer the following questions; (1) are the test methodologies comparable, (2) are the test limits comparable, and (3) for the test standards which are comparable, did the results show failure at comparable levels? In the next sections, the tests are analyzed with these objectives in mind.

3.2 MIL-STD AND IEC COMPARISON OF TEST RESULTS

Table 3.1 shows a shows a high-level comparison of the MIL-STD and IEC standards used in the tests, while Table 3.2 shows a description of the limit verification methods.

6) MIL-STD-461 tries to control the delivered current to the EUT, while IEC 61000-4 focuses on controlling the source voltage (and sometimes power).

7) The operating envelopes of MIL-STD-461 use units of amps, while IEC 61000-4 uses units of volts.

8) MIL-STD-461 uses injection probes (inductive), while IEC 61000-4 uses capacitive coupling (except for IEC 61000-4-6).

9) MIL-STD-461 typically calls for adjusting the test generator output to maintain a given level of current injection with the EUT in the circuit; while IEC 61000-4 series does not typically adjust for the impedance realities of the EUT.

10) MIL-STD-461 typically calls for probe to EUT distances of about 5 cm, whereas IEC 61000-4 allows for up to 1 m. This can affect test results above 30 MHz ($\lambda < 10$ m) since the cable length becomes a significant portion of a wavelength. When the insertion distance becomes a significant portion of a wavelength, the looking-in impedance of the EUT, translated to the injection point, can be greatly affected.

CS114 and IEC 61000-4-6 are the closest equivalents in that they address RF interference, use injection probes, and use fairly similar frequency ranges. Almost all thresholds were a few dB for the two tests. Since the test methods are similar and both use injection probes for coupling, the similarity of these tests is expected. The differences in modulation types and sweep rates were the likely causes for the slight deviations in the test results.

CS116 and IEC 61000-4-12 are similar in that they both apply the damped sine wave with approximately the same power. CS116 and IEC 61000-6-12 both apply the damped sine waveform. However, IEC 61000-4-12 also calls for a Ring Wave test. In the artifact test of IEC 61000-4-12, only the ring wave waveform was used. Therefore, any comparison would be suspect, especially since the threshold of energy necessary to cause errors were not reached in the IEC 61000-4-12 tests. Further investigation is needed to complete the comparison of these tests.

CS101 only addresses power lines and is not comparable with any of the IEC standards used in the post.

CS115 is the only one of the test methods dedicated to exciting natural resonances.

IEC 71000-4-4 and IEC 61000-4-5 are similar, but the first is aimed at applying electrically fast transient voltages and the second is aimed at applying surge voltages, such as those caused by lightning. Therefore, IEC 61000-4-4 uses a much higher coupling impedance (lower capacitance) than does IEC 61000-4-5. The tests produced very dissimilar results. Further investigation is needed to determine why the results differed so much.

Table 3.1 – Overview of military and European standards used in artifact tests

Standard	Frequency	Waveform	Purpose	Coupling
CS101	30 Hz – 150 kHz	Sine	Power Line Only	Trans-former
CS114	10 kHz – 200 MHz	Pulsed Sine	RF	Injection Probe
CS115	NA	Impulse	Natural Resonance.	Injection Probe
CS116	10 kHz – 100 MHz	Damped Sine	Transients	Injection Probe
61000-4-4	1 MHz – 100 MHz	Combi-nation	High voltage transients	Capacitive
61000-4-5	NA	Combination	Surge	Capacitive
61000-4-6	9 kHz – 80 MHz	Amplitude modulated sine	RF	Injection Probe
61000-4-12	100 kHz, 1MHz	Ring/ Damped Sine	Transients	Capacitive

Table 3.2 – Limit verification methods used in the MIL-STD and IEC standards

Standard	Verification method
	MAJOR DIFFERENCE BETWEEN MIL-STD AND IEC STANDARDS: MIL-STD-461 focuses on current delivered to the EUT, while the IEC 61000 series focuses on the voltage (and/or power) available at the output of the test generator
CS101	Initial test generator settings are determined using a calibrated load. During the EUT testing, the power and voltage are both monitored. Adjustments are made, as necessary, to maintain either voltage and/or power limits given, without going over the power setting determined during calibration.
CS114	Initial test generator settings are determined using a calibrated load. During the EUT testing, the forward power and current are both monitored. Adjustments are made, as necessary, to meet the less stringent of these two.
CS115	Initial test generator settings are determined using a calibrated load. During the EUT testing, the actual currents delivered to the EUT are recorded, but no adjustments are made.
CS116	Initial test generator settings are determined using a calibrated load. During EUT testing, the test generator voltage is adjusted, as necessary, to maintain the test limit current into the EUT without going over the calibrated settings. The actual delivered current is recorded.
IEC 61000-4-4	In this standard the shape and magnitude of the waveform are verified at the input to a 50 □ calibration fixture. These measurements are not necessarily verified after connecting the test generator to the actual EUT cable.
IEC 61000-4-5	The short-circuit current and open-circuit voltage capability of the test generator are measured at the output of the coupling/decoupling network. These measurements are not necessarily verified after connecting the test generator to the actual EUT cable.
IEC 61000-4-6	In this standard the magnitude of the signal is verified at the input to a 50 □ measurement equipment. These measurements are not necessarily verified after connecting the test generator to the actual EUT cable.
IEC 61000-4-12	The size of the coupling capacitor is chosen to match the test generator impedance to that of the load. All waveform parameters such as rise time, frequency, open-circuit voltage and short-circuit current are verified before testing. Different impedance values are selected whenever the test voltage at the EUT terminals is reduced to 50% or less of the selected test level.