Introduction And Overview

Advanced Power Electronics and Electrical Machines Quarterly Review

Laura D. Marlino
Engineering Science and Technology Division
PEEM Program Manager

Tuesday, January 11, 2005
National Transportation Research Center

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OAK RIDGE NATIONAL LABORATORY
U. S. DEPARTMENT OF ENERGY

Agenda for January 11, 2005

- **Introduction and Overview of Power Electronics**
- **Capacitors**
  - **Thin film- David Kaufman, ANL**
  - **Glass ceramic, Mike Lanagan, PSU**

Break

- **Polymer film, Bruce Tuttle, SNL**
- **Capacitor Discussion**

Lunch

- **Wide Band Gap Materials, Burak Ozpineci, ORNL**
- **Integrated DC to DC Converter for Multi Voltage Bus Systems, Gui Jai Su, ORNL**
- **Integrated Inverter for HEV and Fuel Cell Vehicles, Gui Jai Su, ORNL**

Break

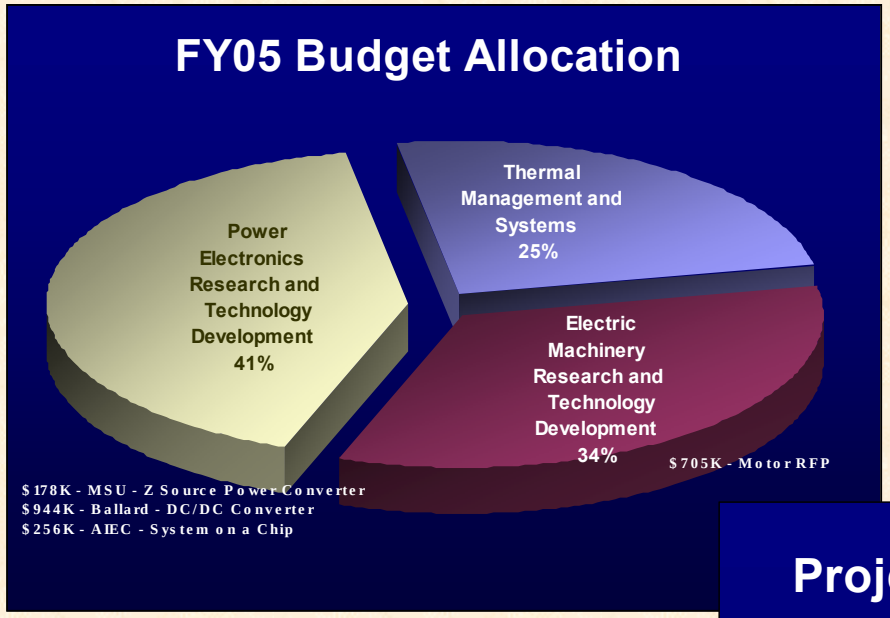
- **Inverter Validation/Testing, Sam Nelson, ORNL**
- **Inverter Discussion**

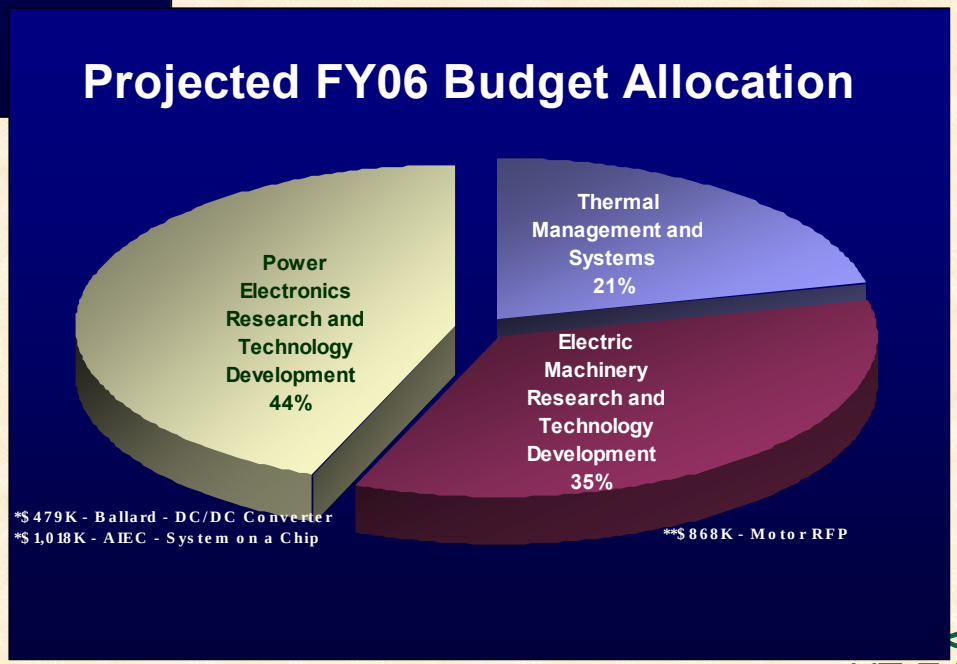
Technology Choices: Challenges and Approaches

Simultaneous Achievement is Required

Challenges	Approaches				
Temperature Capability of Power Electronics	**SiC Technologies** Modeling (ORNL) SiC hybrid inverter (Semikron/Cree) All SiC (RS)	**Two-Phase Cooling** Spray Cooling (OSR) Jet Impingement (RS) VIBE Technology (GT) Modeling (NREL)	**Ceramic or Glass Capacitors** Glass Ceramic (PS)	**Film Capacitors** Polymer Film (SNL) Film on foil (ANL)	**Thermal Resistance** Modeling (NREL) (Semikron)
Cost-Effective Size Reduction of Motors	**Magnetic Materials** Bonded Magnets (AMES)	**Advanced Motor Designs** Reluctance IPM (ORNL) Motor RFP (ORNL) Flux Weakening/CPSR Study (ORNL) Benchmarking (ORNL)	**Material Fabrication Technologies** Motor RFP (ORNL) Benchmarking (ORNL)	**Interior PM Motor** Reluctance IPM (ORNL) Motor RFP (ORNL) Benchmarking (ORNL)	**Thermal Management** Floating Loop (ORNL) Motor slinger/jacket cooling (ORNL)
Weight and Volume of Power Electronics	**Advanced Topologies** Integrated inverter (ORNL) Dual converter (ORNL) DC/DC Converter (Ballard) SoC (AIEC)	**Z-Source Inverter** (MSU)	**Advanced Packaging** (Semikron) DC/DC Converter (Ballard) SoC (AIEC)	**DC/DC Converter** (Ballard) Dual converter (ORNL)	**System On a Chip** (AIEC)

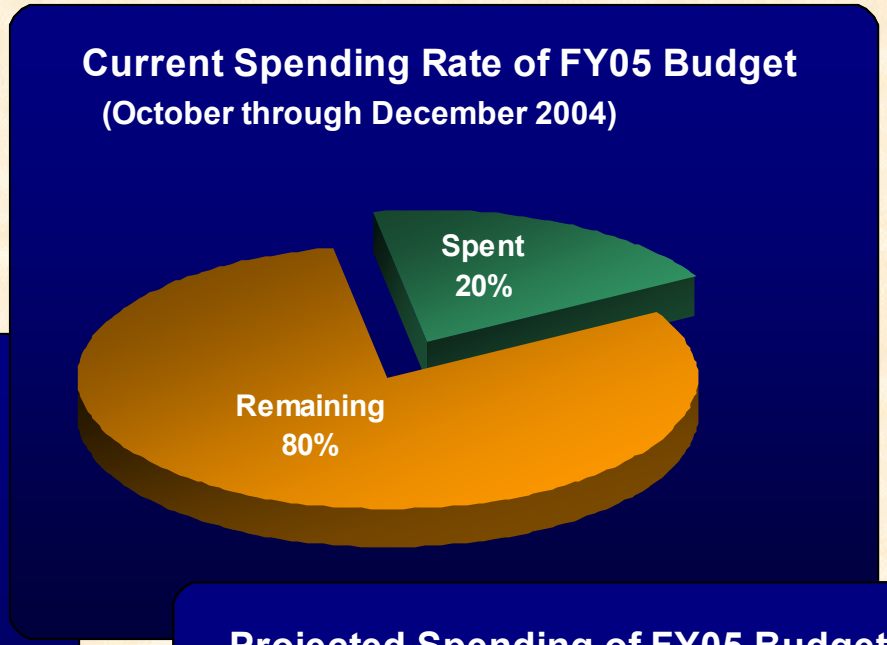
Budget

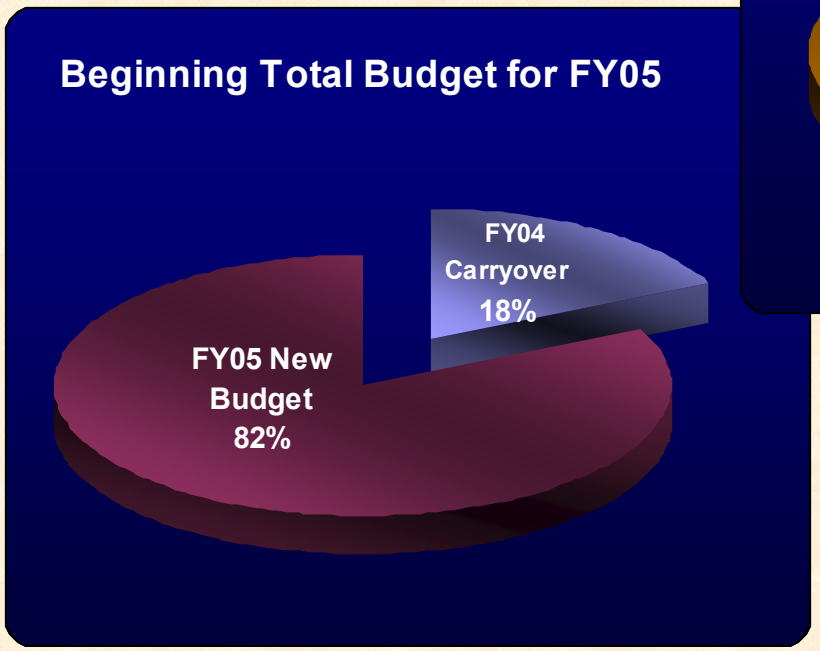

FY05 Budget Allocation
Thermal Management and Systems 25%
Power Electronics Research and Technology Development 41%
Electric Machinery Research and Technology Development 34%
$705K - Motor RFP
$178K - MSU - Z Source Power Converter
$944K - Ballard - DC/DC Converter
$256K - AIEC - System on a Chip

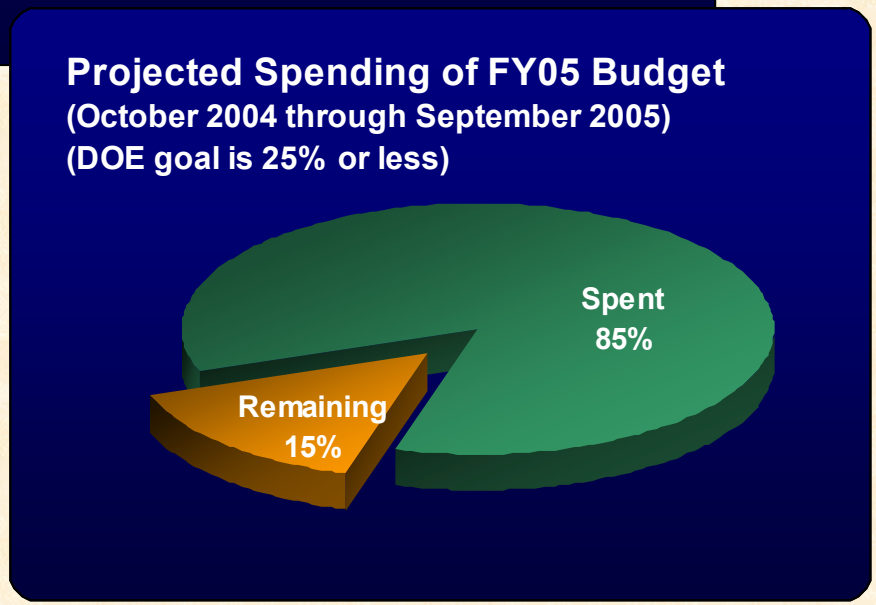

Projected FY06 Budget Allocation
Thermal Management and Systems 21%
Power Electronics Research and Technology Development 44%
Electric Machinery Research and Technology Development 35%
*$479K - Ballard - DC/DC Converter
*$1,018K - AIEC - System on a Chip
**$868K - Motor RFP

Spending

Spending Rate – On Target







Power Electronics

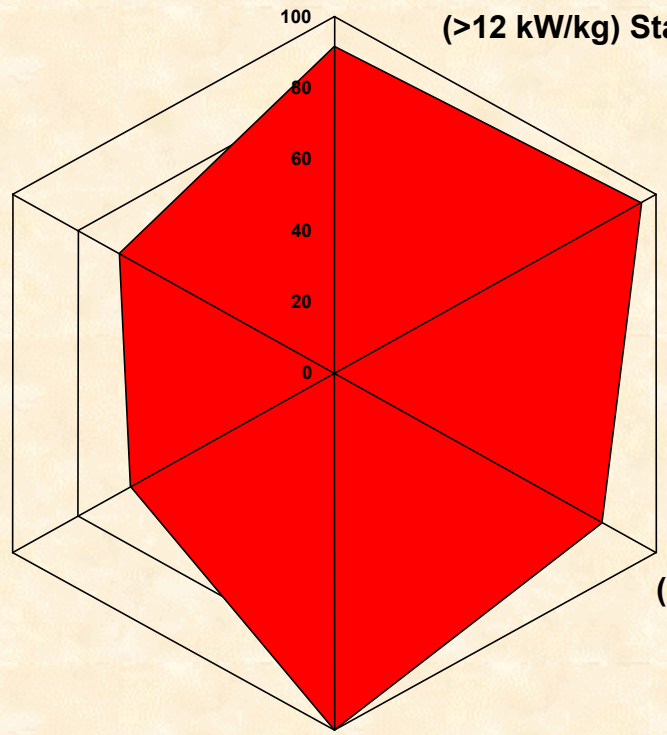
Project Focus in 2005

- **Passive Components**
  - **Capacitors**
    - **Increasing dielectric constants and voltage ratings**
    - **Safe failure modes**
    - **Higher temperature operation**
  - **Planar Magnetics**
    - **Reducing size, weight**
    - **Optimizing performance**

- **Inverters/Converters**
  - **Integration of functionalities**
  - **New topologies**
  - **High temperature operation**

- **Semiconductor Devices**
  - **SiC**
  - **SoC dual motor controller**

Power Electronics: Status versus Targets



Peak Power to Weight Ratio

(>12 kW/kg) Status 11 kW/kg

Peak Power to Volume Ratio

(>12 kW/L) Status 11.5 kW/L

Cost (200 W/$)

Status $167 W/$

Efficiency (97%)

Status 97%

Lifetime (15 Years)

Status 10+ Years

Coolant Inlet Temperature (105°C)

Status 70°C

NOTE: Lifetime and efficiency status based on projections – 10 year verification is in progress; expect to meet 15 year target by 2010

Capacitor Projects

High Dielectric Constant Thin Film Capacitor for Power Electronics
David Kaufman, ANL

Glass Ceramic Capacitors
Mike Lanagan, PSU

Polymer Film and Nano-Ceramic Dielectric Capacitors
Bruce Tuttle, SNL

Capacitor Targets/AVX Film Caps

PARAMETER	YEAR 2004	Current Status (Semikron AVX film caps)
CAPACITANCE	2000 uF +/-10%	1000 uF +/-10%
VOLTAGE RATING	600 VDC	600 VDC
TRANSIENT VOLTAGE	700 V peak for 50ms	1000 V peak for 50ms
LEAKAGE CURRENT	1 ma at rated voltage	unknown
DISSIPATION FACTOR	<1%	unknown
ESR	< 3 milli ohms	< 1 milli ohms
ESL	< 20 nH	< 10 nH
RIPPLE CURRENT	250 amps rms	250 amps rms @ 5kHz & 50C
TEMPERATURE RANGE	-40°C to +140°C	-40°C to +125°C
WEIGHT DENSITY	5.4 grams/uF (10.8 kg)	~ 2.3 grams/uF
SIZE DENSITY	5uF/CC	~ 1.35 uF/CC
COST	$0.02/uF ($40.00)	$0.08/uF
FAILURE MODE	BENIGN FAILURE Fail open	BENIGN FAILURE Fail open
LIFE 80% rated voltage	>10,000 hours 200 amps rms +85°C	>10,000 hours 200 amps rms +85°C
APPLICATION	AUTOMOTIVE UNDERHOOD	AUTOMOTIVE UNDERHOOD

High Dielectric Constant Thin Film Capacitor for Power Electronics

David Kaufman, ANL

Overview	• **To develop film on foil capacitors which will significantly reduce inverter weight, volume and improve performance.** • **Development of technology will allow passive component to be embedded directly into printed wire board.**
2005 Expectations	• **Evaluation of electrical and temperature characteristics** –**Dielectric constant, breakdown voltage** –**Insulation resistance an degradation** • **Continue work on benign failure modes** • **Begin work on embedding and multi-layering into PC boards**
Risks/Barriers	• **Ability to manufacture defect free films over large surface area** • **Ability to be cost competitive**

Glass Ceramic Capacitors

Mike Lanagan, PSU

Overview	• **To develop the materials and process technology for reliable high temperature, low cost DC bus capacitors.** • **Combine the benign failure mode of polymer film capacitors with the superior high temperature ripple current capabilities of ceramic capacitor technologies.**
2005 Expectations	• **Further work on benign failure modes for glass/ceramic compositions** • **Development of higher capacitance/voltage prototypes**
Risks/Barriers	• **Glass coatings effects on capacitor characteristics** • **Achieve benign failure mode at currently required voltage levels** • **Ability to be cost competitive**

Polymer Film and Nano-Ceramic Dielectric Capacitors

Bruce Tuttle, SNL

Overview	• **To develop polymer films and nano-ceramic dielectrics that will address the FCVT requirements for DC bus capacitors.**
2005 Expectations	• **Continue work on new polymer film chemistries** • **Perform electric and temperature characterizations of polymer film dielectrics** • **Fabricate and test nano-dielectric capacitors to meet FreedomCAR requirements**
Risks/Barriers	• **Ability to resolve film brittle properties** • **Polymers able to withstand 140ºC for 15 yrs?** • **Ability to be cost competitive**

ORNL Power Electronic Projects

Wide Bandgap Materials
Burak Ozpineci

Low Cost Bidirectional dc/dc Converter for Multi-Voltage Bus Systems
Gui Jai Su

Integrated Inverter for HEVs and Fuel Cell Powered Vehicles
Gui Jai Su

DC to DC Converter targets (RFP)

- **Dual outputs**
  - **14v—3kW, 92% eff**
  - **42v—5kW, 92% eff**
- **Single output**
  - **14v—5kW, 92% eff**
- **$75/kW (100k volume)**
- **Volume =5 l**
- **Weight = 5 kg**
- **15yr or 150K miles lifetime**
- **Status for automotive converters..$130/kW (1.5kW=$200-260)**

Inverter Targets

Taken from original AIPM specifications

Requirement	Series	Parallel
Continuous power (kW)	30	15
Peak power (kW)	55	30
Battery voltage (Vdc)	325 (200-450)	325 (200-450)
Power factor	>.8	>.8
Max current out (A)	300	200
Eff (10-100% speed, 20% rated T)(%)	97*	97*
Output current ripple (pk-pk) (%)	≤5	≤5
Input voltage & current ripple (%)	≤5	≤5
Current loop bandwidth (kHz)	2	2
Max fundamental electrical freq (Hz)	1000	1000

Requirement	Series	Parallel
Ambient operating temp (ºC)	-40 to 125	-40 to 125
Cooling system flow rate, max (gpm)	2.5	2.5
Max coolant inlet temp (ºC)	105	105
Max inlet pressure (psi)	25	25
Max inlet pressure drop (psi)	2	2
Useful life (yrs/miles)	15/150*	15/150
Minimum isolation impedance-terminal to gnd (M ohm)	1	1
Max weight (kW/kg	5	5
Max volume kW/liter	12	12
Max cost ($/kW)	5	5

*not yet proven

Wide Bandgap Materials

Burak Ozpineci, ORNL

AOP Task 4.1

Overview	• **To develop simulation tools to quantify the impact of WBG semiconductors and verify the results with experimental testing.** • **Future cost reductions and processing improvements will allow SiC power converter systems to possibly surpass FCVT targets and goals.**
2005 Expectations	• **Continue modeling, characterization and testing of new SiC devices** • **Perform comparison of hybrid SiC/Si and all SiC inverter with Si inverter** • **Begin long term reliability studies of SiC devices**
Risks/Barriers	• **Manufacturing defects must be resolved** • **Cost**

Low Cost Bidirectional dc/dc Converter for Multi-Voltage Bus Systems

Gui Jai Su, ORNL

AOP Task 4.2

Overview	• **Develop converter which reduces component costs and volume by 50%.** • **Produce dc to dc converter that will enable quantitative evaluation of integrated converter's ability to meet FreedomCAR needs and assist in establishing technical targets.**
2005 Expectations	• **Design, fabricate and test 2kW prototype with reduced parts count**
Risks/Barriers	• **Acceptance by industry**

Integrated Inverter for HEVs and Fuel Cell Powered Vehicles

Gui Jai Su, ORNL

AOP Task 4.3

Overview	• **Design and build an inverter topology that can reduce the number of components and cost by one third.** • **Develop integrated power conversion topologies for motor drives to reduce size and cost of power electronics systems for EV/HEV traction and accessory drives.**
2005 Expectations	• **Design, fabricate and test prototype for dual PM motors** • **Develop sensorless technology for motor control**
Risks/Barriers	• **Acceptance by industry**

Ongoing Subcontracts

Z Source Inverter…Michigan State University

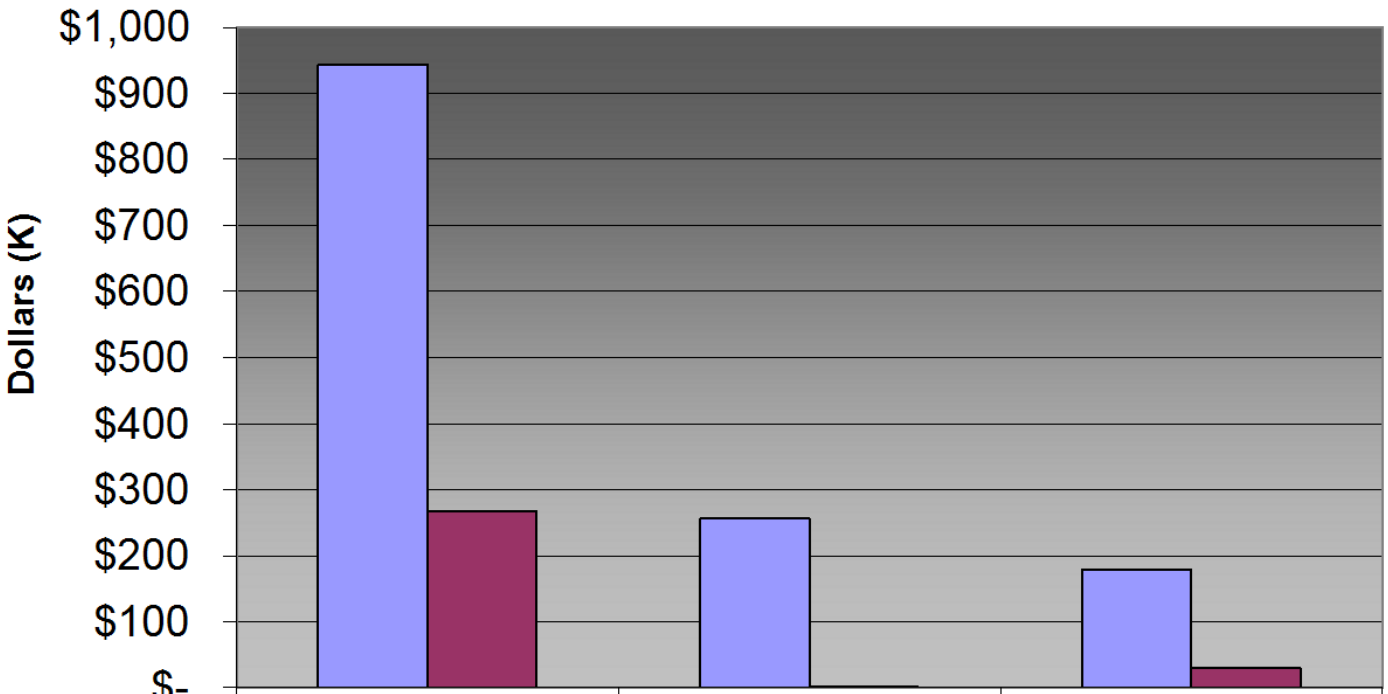
DC to DC Converter…Ballard Power Systems

Dual Motor Controller SoC…Automotive Integrated Electronics Company

Subcontract Power Electronic Projects

AOP Task	Title	Summary
4.4	Z Source Power Converter for Fuel Cell Powered Vehicles	To develop new power conversion topology combining dc/dc converter with inverter. Significantly reduce cost and reliability over comparable existing systems.
4.5	Dc to Dc Converter (Ballard Power Systems)	To achieve higher reliability, efficiency, and temperature capabilities while reducing volume and cost of a dc to dc converter through innovative design, and manufacturing methods.
4.5	Dual Motor Controller SoC Development (AIEC)	To dramatically reduce the costs and improve efficiency of existing motor control circuitry by combining functionalities within a single ASIC.

Subcontract Spending Status



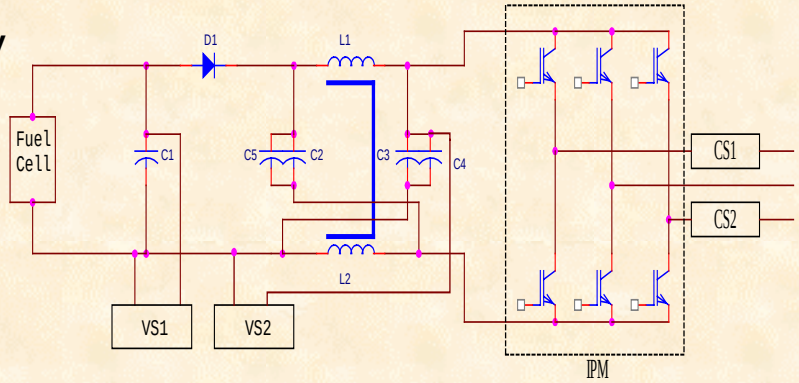
	DC/DC Converter Development (Ballard)	System on a Chip Development (AIEC)	Z Source Power Converter for Fuel Cell Powered Vehicles (MSU)
FY05 Budget (K)	$944	$256	$178
FY05 Actual Costs (K)	$268	$1	$30

Z Source Converter

Subcontract through MSU

Project Overview

- Need to oversize the inverter and motor due to the wide range of voltage change and great CPSR requirement.
  - Leads to high cost, high stress, low reliability
- New topology and new power conversion technology
- Ability to buck/boost the voltage and to extend CPSR
- No need for dead time
- Minimized power electronics and machines
- Low cost, high efficiency, and high reliability



C1--C5:UL31Q207K;
L1+L2: One inductor using core AMCC_250;
VS1, VS2: voltage sensors LV25-400;
CS1,CS2: Current sensors HC6F300-S;
IPM: PM600CLA060
D1: QRS0660T30

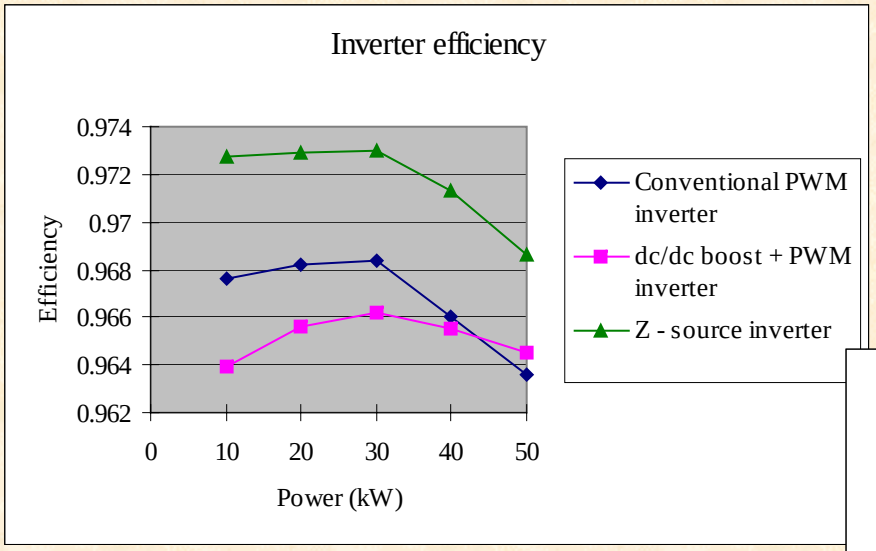
Z Source Project Task Schedule

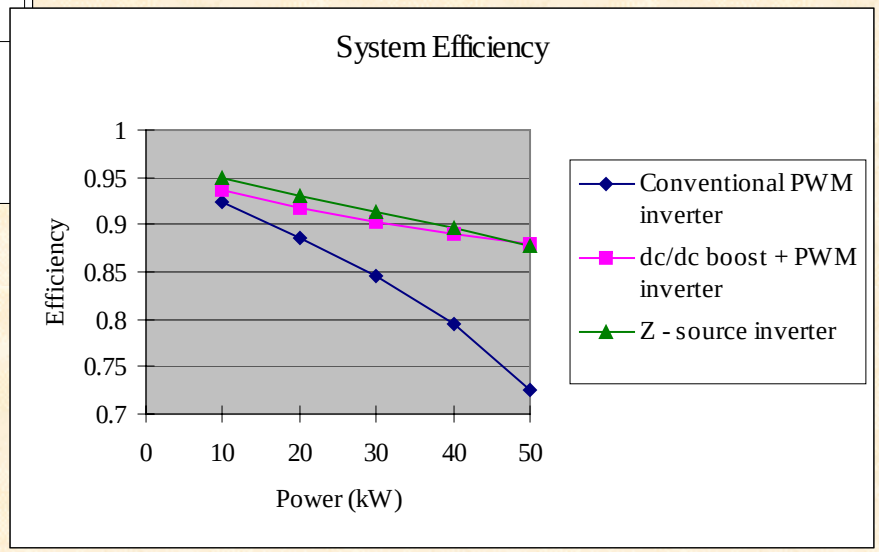
- Tasks 1&2: Develop specifications for a Z source inverter prototype with ORNL. Perform a comprehensive cost comparison, model development, and computer simulation – March 31, 2004
- Task 3: Design and fabricate a 55-kW Z source inverter prototype to prove the concept experimentally.
  - Design and design review with ORNL – August 31, 2004
  - Main, control circuit design, printed circuit board layout, and purchase of components – November 30, 2004
  - Circuit fabrication and assembly – January 31, 2005
  - Main and control circuit test and debug – March 31, 2005
- Task 4: Test and demonstrate the prototype.
  - Debug and test.
  - Operating demonstration and data acquisition at MSU with ORNL's participation and on-site evaluation – August 31, 2005
- Task 5: Performance study and final report.
  - Summarize the data obtained from the prototype; perform analysis and comparison with the traditional inverter.
  - Documentation, presentation, and final report.
  - *Deliver the 55 kW working prototype and final report to ORNL for independent evaluation* – September 30, 2005

Comparison Results Summary

- **Z source inverter improves inverter conversion efficiency by 1% over the two existing inverters and inverter/motor system efficiency by 2 to 15% over the conventional PWM inverter.**
- **Z source also reduces the average current SDP by 15%, which leads to cost reduction.**
- **Z source extends CPSR by 1.68 times over the system driven by the conventional PWM inverter.**
- **Achieves significant cost reduction over conventional systems.**
- **High reliability due to no shoot-through problem.**

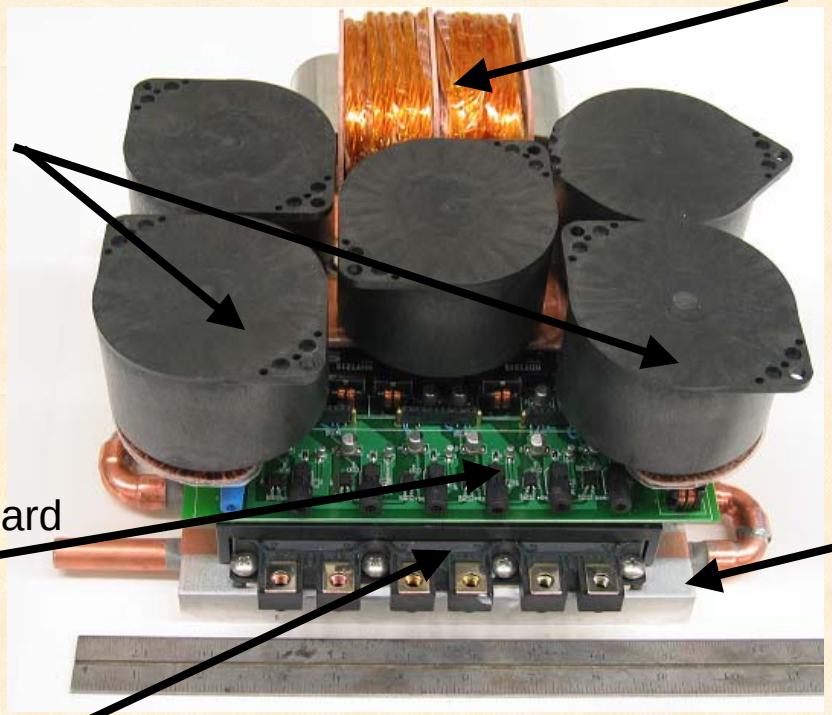
Inverter and System Efficiency Comparisons



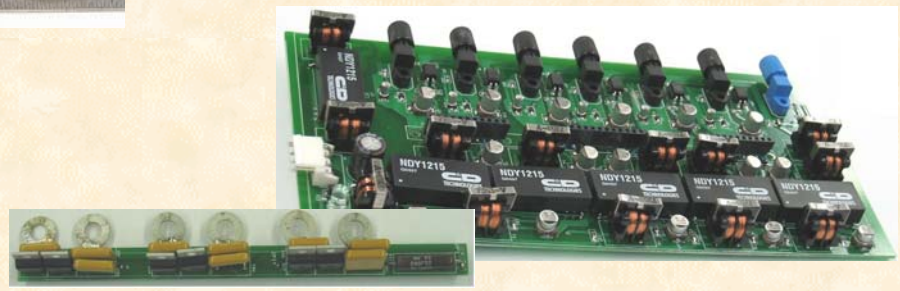


Final Inverter Assembly

The final inverter module 11”x11.5”x5”



gate drive board



snubbers

Project Risks and Barriers

- **Ability to reach simulated performance**

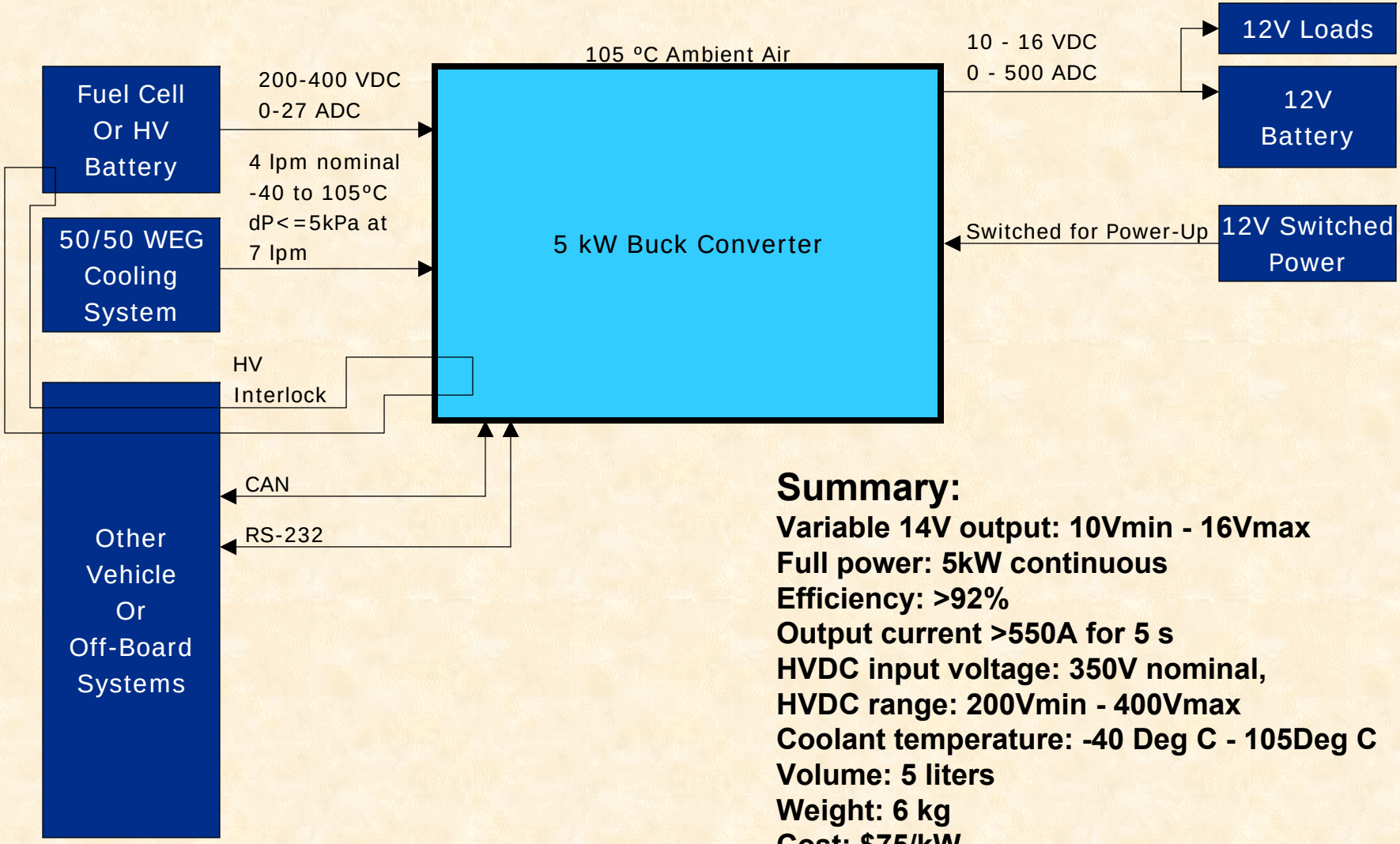
Future Direction

- **Perform debugging, testing, and data acquisition of the system performance of the inverter**
- **Delivery of final report and 55 kW unit to ORNL for evaluation**

DC to DC Converter

Subcontract through Ballard Power Systems

Specification: 5 kW Buck Converter



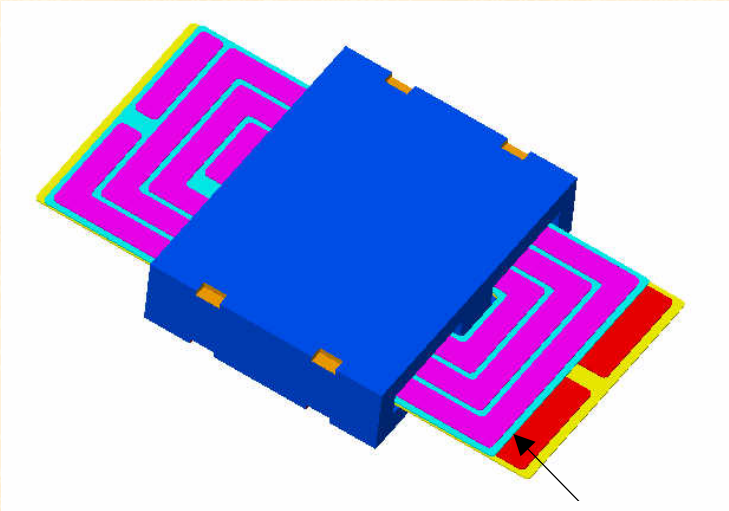
Summary:

Variable 14V output: 10Vmin - 16Vmax
Full power: 5kW continuous
Efficiency: >92%
Output current >550A for 5 s
HVDC input voltage: 350V nominal,
HVDC range: 200Vmin - 400Vmax
Coolant temperature: -40 Deg C - 105Deg C
Volume: 5 liters
Weight: 6 kg
Cost: $75/kW

Project Tasks

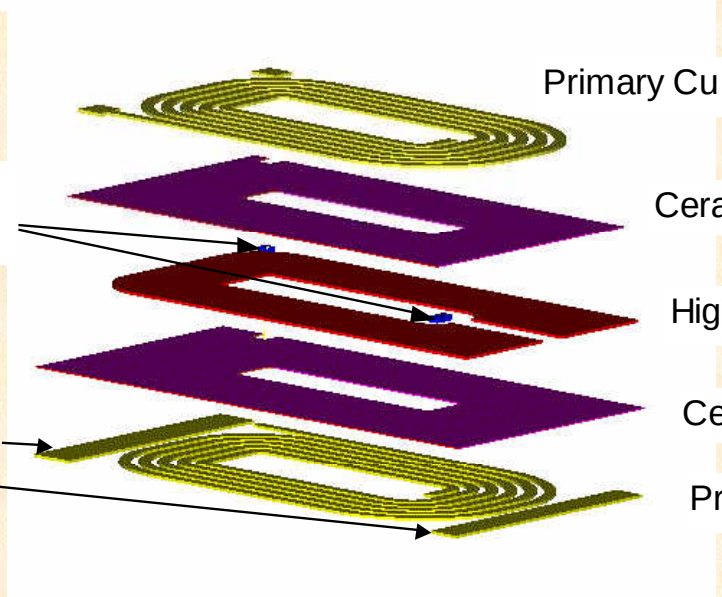
- Built segmented prototype
  - Solder-process development for DBC based winding
  - Interconnection between power devices and transformer
  - Integration of passive components
- Test the prototype
  - Functional test
  - DBC-based transformer electrical and thermal performance
  - High voltage power stage – losses and thermal resistance
  - Low voltage power stage - losses and thermal resistance
- Identify key variable effecting performance
- Analyze the tradeoffs
- Select the components for DOE/ORNL project based on the test results of segmented prototype
  - Interleaved vs. non-interleaved design
  - The best power devices for LV and HV
- Build DOE/ORNL prototype 5kW DC-DC converter

Prototype Transformer DBC Winding



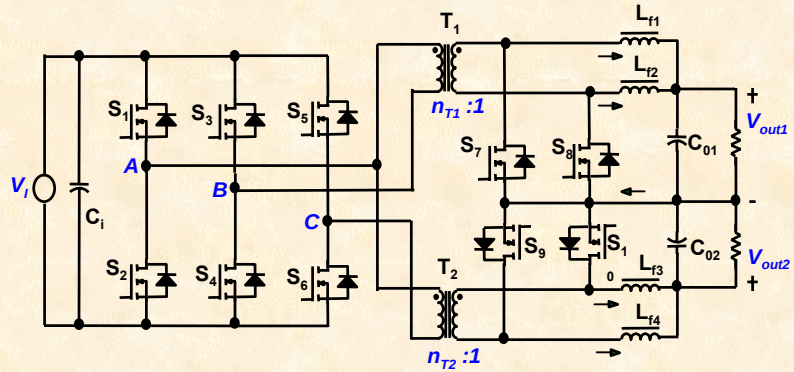
Magnetic core size:

64mm long & 51mm wide

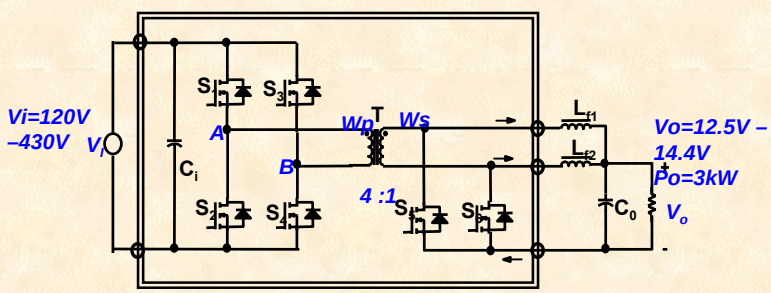


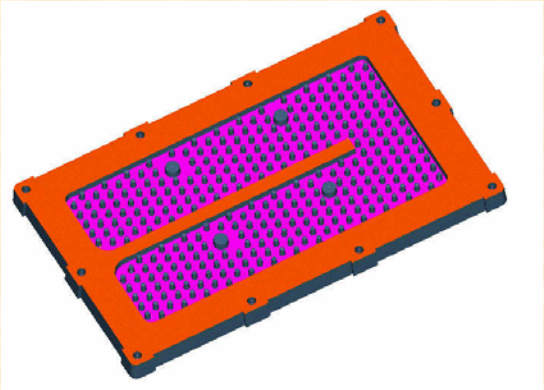
Segmented Converter

Dimensions ~ 5”x10”



Segmented prototype





Pinfin AlSiC baseplate for final design

Project Status

Test of prototype

- **Converter functions successfully**
- **Reverse recovery of body diodes in MOSFETs were not optimum (dominant losses)**
  - **Redesign with MOSFETs with faster recovery characteristics**
  - **Add capacitors to improve ringing**
- **15 mil wire bonds to LV DBC adds significant resistance**
  - **Increase number of bonds, change to 20 mil**
- **Inductance in LV side was too low**
  - **Inductors will need to be added to reduce di/dt transition**

Project Risks and Barriers

- **Ability to meet cost target**
  - **Using interleaved design increases risk**
  - **AlSiC baseplate**
  - **High coolant temperature requirement necessitates use of more expensive components**
- **Ability to meet performance targets if have to resort to non interleaved design**

Future Direction

- **Build new prototype with MOSFETs having improved diode characteristics**
- **Evaluate electrical and thermal performance of DBC based transformer**
- **Measure high voltage power stage-losses and thermal resistance**
- **Measure low voltage power stage-losses and thermal resistance**
- **Analyze cost/performance tradeoffs between interleaved vs. non- interleaved design**
- **Select the components for project based on test results**
- **Build 5kW prototype and deliver to ORNL for evaluation**

Dual Motor Controller System on a Chip

Subcontract through Automotive Integrated Electronics Corporation (AIEC)

Project Overview

- **Technical Overview**
  - **System on a Chip (SoC) dual motor controller for use in hybrid and fuel cell-based vehicles.**
  - **Through the reduction in parts count and manufacturing efforts, it is hoped a cost reduction of 40 to 60% can be realized in high volume production.**
  - **SoC component cost less than $90 in high volume production.**
- **Phase 1 Objectives**
  - **Detailed cost study and analysis of potential processes and packaging methods that will meet the technical requirements.**
- **Phase 2 Objectives**
  - **Culminate in the delivery of a functioning packaged controller chip.**

AIEC Status at End of Phase I

- **Selected Technology: STMicroelectronics CMOSM9 process**
  - **0.13 µm logic process with flash module**
- **Completed preliminary design**
- **Characterized at -40°C to 125°C (junction temperatures to 150°C)**
- **Completed power budget**
  - **Estimated average power consumption: 543 mW**
- **Completed cost estimations**
- **Selected packaging**
  - **BGA**
    - **27mm x 27mm body size**
    - **300 balls**
    - **30°C/W thermal impedance to ambient air**
      - **Thermal vias**
      - **No thermal balls required**

Phase II Estimated Cost and Schedule

- Estimated Cost (Real Cost, Not 50% Cost Sharing)
  - Non-Recurring Engineering
    - ✓ Design Engineering $500K
    - ✓ Physical Design $500K
  - Semiconductor Tooling
    - ✓ Production Tooling up to $1M
    - ✓ Multi-Project Wafer between $75K and $150K
  - BGA package design $37.5K
- Total Production Path=$2,037,500
- Total Multi-Project Path=$1,075,000-$1,150,000
- Estimated Schedule
  - Design Engineering / Physical Design between 0.5 and 1 Year
    - ✓ Depends on Macrocell Development
  - Prototype Manufacturing between 4 Months and 1 Year
    - ✓ Depends on Validation / Qualification Requirements

Project Risk and Barriers

- **NRE production costs**
- **TI and Freescale have already achieved majority of technical targets**
  - **TI DSP available at $18.00/K vs AIEC projected $55.00**
  - **Both achieve temperature targets**
- **Large amount of support, software, compilers, emulation and design tools exist for TI/Freescale chips**
  - **With giants in industry already established, can AIEC ever catch up?**

Future Direction

- **Decision needed as to whether or not to proceed to Phase II**