

Multilevel DC Link Inverter

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Abstract— This paper presents a new class of multilevel inverters based on a multilevel dc link (MLDCL) and a bridge inverter to reduce the number of switches, clamping diodes or capacitors. A MLDCL can be a diode-clamped phase leg, a flying capacitor phase leg, or cascaded half-bridge cells with each cell having its own dc source. A multilevel voltage source inverter can be formed by connecting one of the MLDCLs with a single-phase bridge inverter. The MLDCL provides a dc voltage with the shape of a staircase approximating the rectified shape of a commanded sinusoidal wave, with or without pulse width modulation, to the bridge inverter, which in turn alternates the polarity to produce an ac voltage. Compared with the cascaded H-bridge, diode-clamped and flying-capacitor multilevel inverters, the MLDCL inverters can significantly reduce the switch count as the number of voltage levels increases. For a given number of voltage levels, m , the required number of active switches is $2 \times (m-1)$ for the existing multilevel inverters but is $m+3$ for the MLDCL inverters. Simulation and experimental results are included to verify the operating principles of the MLDCL inverters.

Keywords—multilevel inverter; cascaded half-bridge; diode-clamped; flying capacitor; multilevel dc link; reduced part count

I. INTRODUCTION

Multilevel voltage source inverters based on the diode clamped phase-legs, flying capacitor phase-legs or cascaded H-bridges were proposed for replacing the two-level inverters with series connection of switches or transformer coupled multiple two-level inverters in medium- or high-voltage level applications such as motor drives and static var compensators [1–10]. Advantages of the multilevel inverters include: (1) the multilevel structures can ensure even voltage sharing, both statically and dynamically, among the active switches while it is difficult for a two-level inverter with a series connection of switches to do so, (2) substantial reduction in size and volume is possible due to the elimination of the bulky coupling transformers or inductors, (3) multilevel inverters can offer better voltage waveforms with less harmonic contents and thus can significantly reduce the size and weight of passive filter components. The last feature was further explored in multilevel inverters using IGBTs for replacing GTO-based two-level

inverters because IGBTs can switch faster and have less-demanding gate drive requirements than GTOs. On the other end of the power spectrum, because of their low cost resulting from widespread use in the automotive and power supply industries, low on-resistance, and fast switching capability, low voltage MOSFETs are utilized in multilevel inverters to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage at high efficiency that it is unable to achieve with linear amplifiers [11–13].

Despite the superior voltage waveform quality provided by higher level inverters, the neutral point clamped inverter in [1] is perhaps the most widely used multilevel structure because of its relatively small number of switches. The high switch count and the difficulty to balance the voltage of the capacitors in the diode-clamped configuration have been preventing the wide acceptance of the higher level inverters in practical applications. As the number of voltage levels, m , grows, the number of active switches increases according to $2 \times (m-1)$ for the cascaded H-bridge, diode-clamped and flying capacitor multilevel inverters. In addition, for each phase, the diode-clamped inverter requires at least $2 \times (m-2)$ clamping diodes and $(m-1)$ capacitors for dividing the dc voltage, and the flying capacitor inverter needs $(m-2)$ clamping capacitors.

This paper presents a new class of multilevel inverters based on a multilevel dc link (MLDCL) and a bridge inverter. Compared with the existing multilevel inverters, the new MLDCL inverters can significantly reduce the switch count as the number of voltage levels increases. For a given number of voltage levels, m , the new inverters requires $m+3$ active switches, roughly half the number of switches, clamping diodes, voltage splitting capacitors in the diode clamped configuration, or clamping capacitors in the flying capacitor configuration. Simulation and experimental results are included to verify the operating principle of the proposed MLDCL inverters.

II. PROPOSED MLDCL INVERTER TOPOLOGIES

A. Cascaded Half-Bridge Based MLDCL Inverter

Fig. 1(a) shows a schematic diagram of the proposed inverter topology, which consists of a multilevel dc source and a single-phase full-bridge (SPFB) inverter. The dc source is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two switches. The two switches, S_{ak} and S_{bk} , operate in a toggle

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fashion. The cell source is bypassed with S_{ak} on and S_{bk} off, or adds to the dc link voltage by reversing the switches. The operating principle can be explained in Fig. 1(b) by looking at the operating voltage, current and gating signal waveforms given for the most common load, an inductive load, where V_{bus} is the dc bus voltage of the SPFB inverter, i_{bus} the dc bus current, v_{an} the output ac voltage, v_{an-1} the fundamental components of v_{an} , i_a the output ac current, and $S_1 \sim S_4$, $S_{b1} \sim S_{bn}$ represent the corresponding switch's gating signals. The usual convention is used where "1" dictates on and "0" off. The MLDC provides a dc bus voltage, V_{bus} , with the shape of a staircase that approximates the rectified waveform of the commanded sinusoidal voltage, to the SPFB inverter, which in turn alternates the voltage polarity to produce an ac voltage of a staircase shape, v_{an} . While the switches in the cells can perform pulse width modulation if necessary or switch at twice the fundamental frequency of the output voltage, the four switches in the SPFB inverter S_1 and S_4 , S_2 and S_3 always work in pairs at the fundamental frequency of the output voltage. This topology was initially introduced in [14], where a three-phase bridge is used instead of a SPFB, to reduce current ripple for brushless dc motors with an extremely low leakage inductance.

Specifically, the MLDC formed by the n half-bridge cells provides a staircase-shaped dc bus voltage of n steps, to the SPFB inverter, which in turn alternates the voltage polarity to produce an ac voltage, v_{an} , of a staircase shape with $(2 \times n + 1)$ levels, whose voltages are $-(V_{s1} + V_{s2} + \dots + V_{sn})$, $-(V_{s1} + V_{s2} + \dots + V_{sn-1})$, ..., $-V_{s2}$, $-V_{s1}$, 0 , V_{s1} , V_{s2} , ..., $(V_{s1} + V_{s2} + \dots + V_{sn-1})$, $(V_{s1} + V_{s2} + \dots + V_{sn})$. The dc bus voltage and current are therefore related to their output ac counterparts by

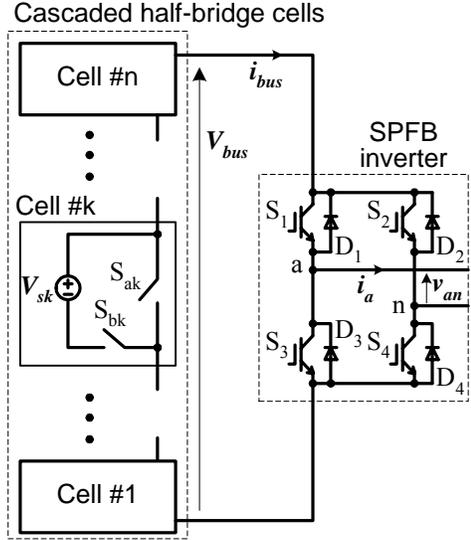
$$V_{bus} = |v_{an}|$$

$$i_{bus} = \begin{cases} i_a & \text{for } v_{an} \geq 0 \\ -i_a & \text{for } v_{an} < 0 \end{cases}$$

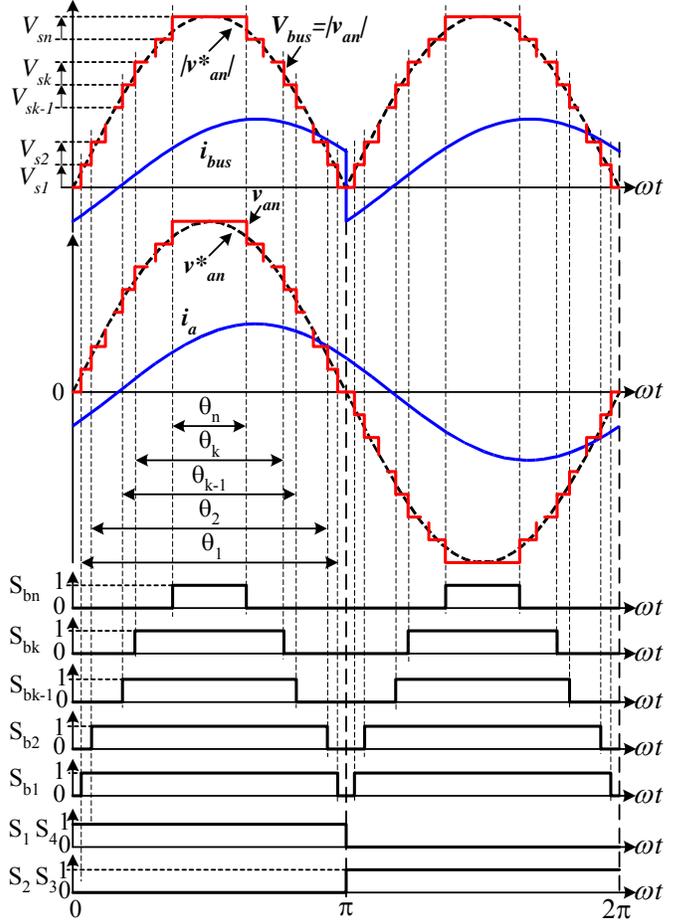
Assuming each cell adds its source voltage V_{sk} to the dc bus over an angular period of θ_k in each half cycle without performing PWM, the peak fundamental component of the ac output can be determined by

$$v_{an-1(peak)} = \frac{4}{\pi} \sum_{k=1}^n V_{sk} \sin \frac{\theta_k}{2}$$

Fig. 2 plots a chart for comparison of the required number of switches between the proposed MLDC inverter and the cascaded H-bridge count part. As the number of voltage levels, m , grows, the number of active switches increases according to $m+3$ for the MLDC inverter, compared to $2 \times (m-1)$ for the cascaded H-bridge multilevel inverters. A similar trend also occurs for the diode-clamped and flying capacitor multilevel inverters, to be discussed in the following subsections. Another salient feature of the new inverter is that, with an inductive load, the switches $S_1 \sim S_4$ in the SPFB inverter always turn off at zero voltage and turn on at both zero voltage and current.



(a) $2n+1$ level MLDC inverter



(b) Operating waveforms

Figure 1. A proposed MLDC inverter based on cascaded half-bridge cells and a single-phase full-bridge inverter.

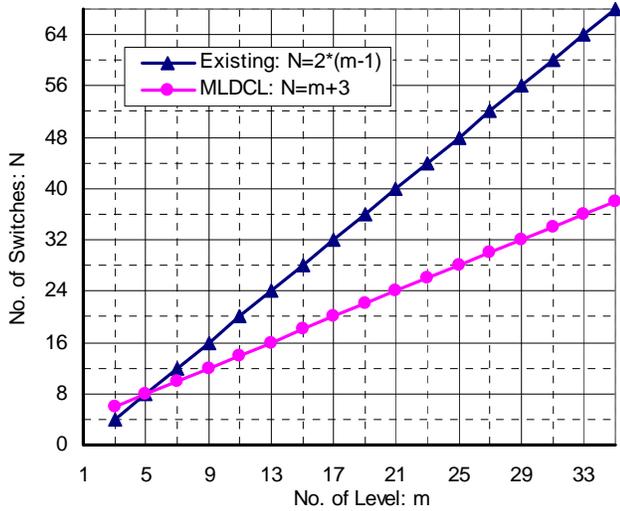


Figure 2. Comparison of required number of switches.

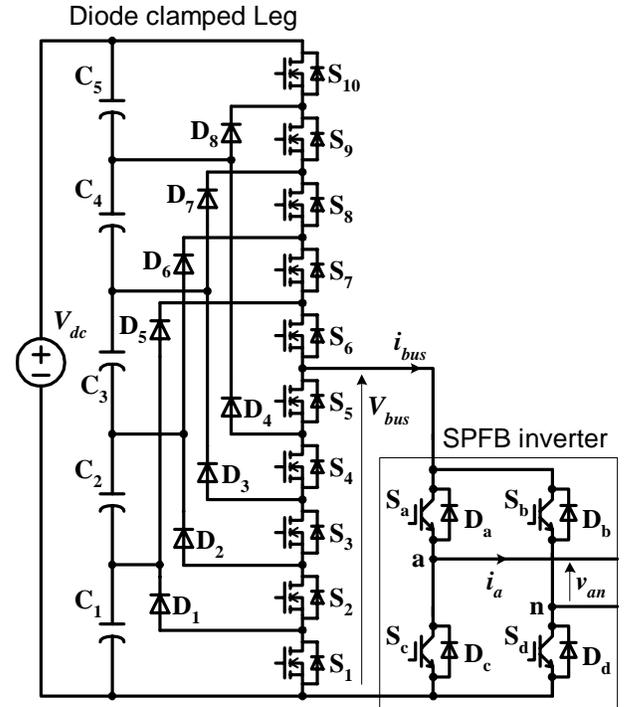
B. Diode-Clamped Phase Leg Based MLDCL Inverter

The diode-clamped phase leg can also be used to provide a multilevel dc bus voltage with the shape of a staircase to the SPFB inverter. As an example, Fig. 3(a) is an eleven-level MLDCL inverter based on the diode-clamped phase leg. The diode-clamped phase leg, consisting of ten switches, $S_1 \sim S_{10}$, eight clamping diodes, $D_1 \sim D_8$, and a voltage divider of five capacitors, $C_1 \sim C_5$, provides a dc bus voltage of six voltage levels. Assuming the dc source voltage, V_{dc} , is evenly split by the capacitors, the six voltage levels of 0 , $(1/5)V_{dc}$, $(2/5)V_{dc}$, $(3/5)V_{dc}$, $(4/5)V_{dc}$, and V_{dc} , can be produced by turning on simultaneously the switch combinations of $(S_1 S_2 S_3 S_4 S_5)$, $(S_2 S_3 S_4 S_5 S_6)$, $(S_3 S_4 S_5 S_6 S_7)$, $(S_4 S_5 S_6 S_7 S_8)$, $(S_5 S_6 S_7 S_8 S_9)$, and $(S_6 S_7 S_8 S_9 S_{10})$, respectively. Again, the SPFB inverter flips the polarity of the dc bus voltage, V_{bus} , to produce an eleven-level ac voltage, v_{an} as shown in Fig. 3(b), where the dc bus current, i_{bus} , inverter output current, i_a , and the current conducting states of the switches, $S_a \sim S_d$ and diodes, $D_a \sim D_d$ in the SPFB are shown for an inductive load. As for the section A inverter, switches $S_a \sim S_d$ in the SPFB inverter always turn off at zero voltage and turn on at both zero voltage and current with an inductive load. It is also clear from Fig. 3 (b) that the turn-off current approaches 0 as the power factor approaches 1.

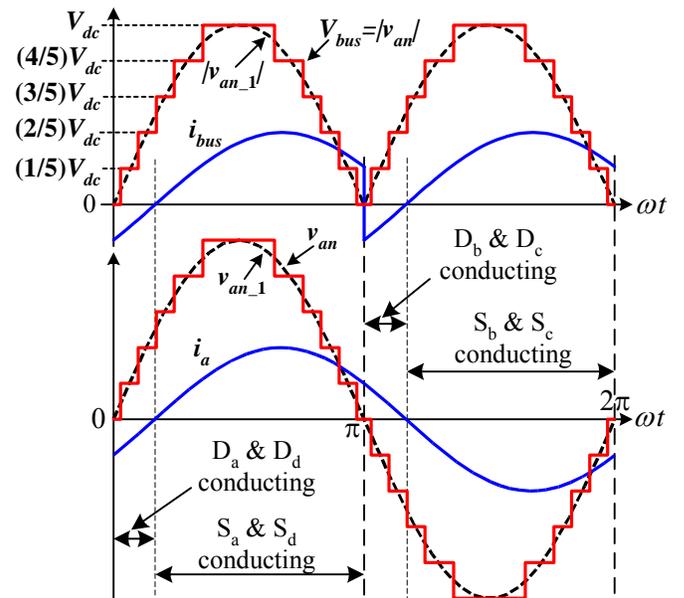
Table I gives a comparison of the number of switches, clamping diodes and voltage dividing capacitors required to produce an eleven-level output voltage for the proposed inverter and the existing counterpart, clearly showing substantial component reduction with the proposed structure. This saving in components grows as the number of voltage level increases as mentioned before.

TABLE I. PART COUNT COMPARISON FOR PRODUCING AN ELEVEN-LEVEL OUTPUT VOLTAGE.

Components	Proposed	Existing
Switches	14	20
Clamping diodes	8	18
Capacitors	5	10



(a) eleven-level MLDCL inverter



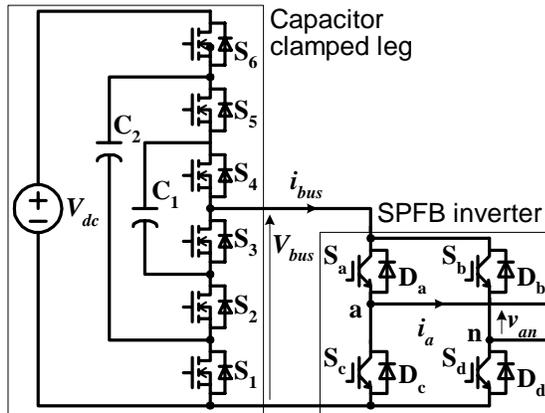
(b) Operating waveforms

Figure 3. A proposed MLDCL inverter based on a diode-clamped leg and a single-phase full-bridge inverter.

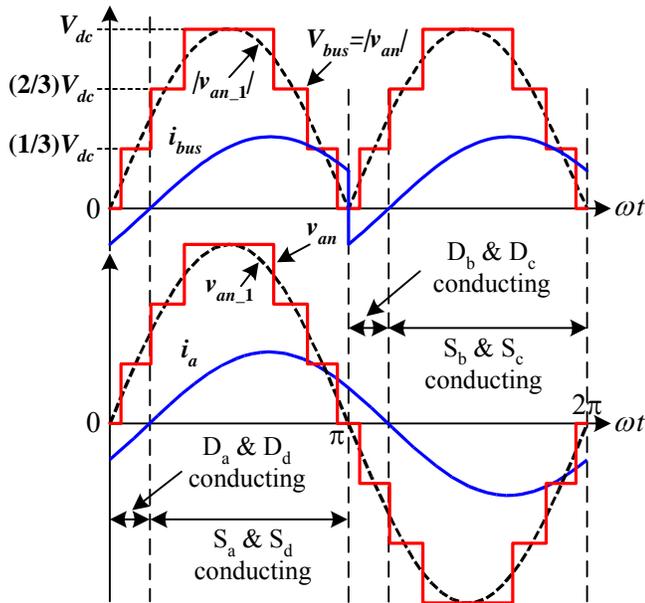
C. Flying Capacitor Phase Leg Based MLDCL Inverter

Fig. 4(a) shows the arrangement of a seven-level MLDCL inverter based on a capacitor-clamped phase leg and a single-phase bridge. The capacitor-clamped phase leg, consisting of six switches, $S_1 \sim S_6$, and two clamping capacitors, C_1 and C_2 ,

provides a dc bus voltage of four voltage levels, 0 , $(1/3)V_{dc}$, $(2/3)V_{dc}$, and V_{dc} , by turning on the switches according to the voltage levels as listed in table II. There are multiple choices of switch combinations to produce the two middle levels and the capacitors will be charged or discharged as indicated in the table too. By controlling the duration of these switch combinations, the voltage across C_1 and C_2 can be maintained at the required level of $(1/3)V_{dc}$ and $(2/3)V_{dc}$, respectively. This is a desirable feature for preventing drift of the capacitor voltages, which is lacked in the diode clamped configuration, leading to difficulty in keeping the capacitor voltages balanced. Again, the SPFB inverter flips the polarity of the dc bus voltage, V_{bus} to produce a seven-level ac voltage, v_{an} , as shown in Fig. 4(b), where the dc bus current, i_{bus} , inverter output current, i_a , and the current conducting states of the switches, $S_a \sim S_d$ and diodes, $D_a \sim D_d$ in the SPFB are shown for inductive load.



(a) seven-level MLDCI inverter



(b) Operating waveforms

Figure 4. A proposed MLDCI inverter based on a capacitor-clamped leg and a single-phase full-bridge inverter.

TABLE II. SWITCHING TABLE

V_{bus}	Switches to be turned on	Charge/discharge the capacitors
0	$S_1 S_2 S_3$	No
$(1/3)V_{dc}$	$(S_1 S_2 S_4)$ or $(S_1 S_3 S_5)$	Discharge C_1
	$(S_2 S_3 S_6)$	Charge C_2
	$(S_1 S_4 S_5)$ or $(S_3 S_5 S_6)$	Charge C_1 and discharge C_2
$(2/3)V_{dc}$	$(S_1 S_4 S_5)$ or $(S_3 S_5 S_6)$	Discharge C_2
	$(S_3 S_5 S_6)$	Charge C_1
V_{dc}	$S_4 S_5 S_6$	No

With the new configuration, the number of switches is reduced from twelve to ten and the number of capacitors from five to two. Again, this saving grows with the number of levels.

III. SIMULATION AND EXPERIMENTAL RESULTS

Detailed circuit simulation was conducted to verify the operating principles of the proposed MLDCI inverters.

A. Half-bridge Based MLDCI Inverter

A three-phase eleven-level half-bridge cell-based MLDCI inverter was first studied for powering an inductive resistor load, as shown in Fig. 5. The load resistance and inductance are $18 \text{ m}\Omega$ and $25 \text{ }\mu\text{H}$ per phase, and the voltage of each dc source, V_s , is set at 30 V . At an output frequency of 100 Hz , the load power factor is 0.75 .

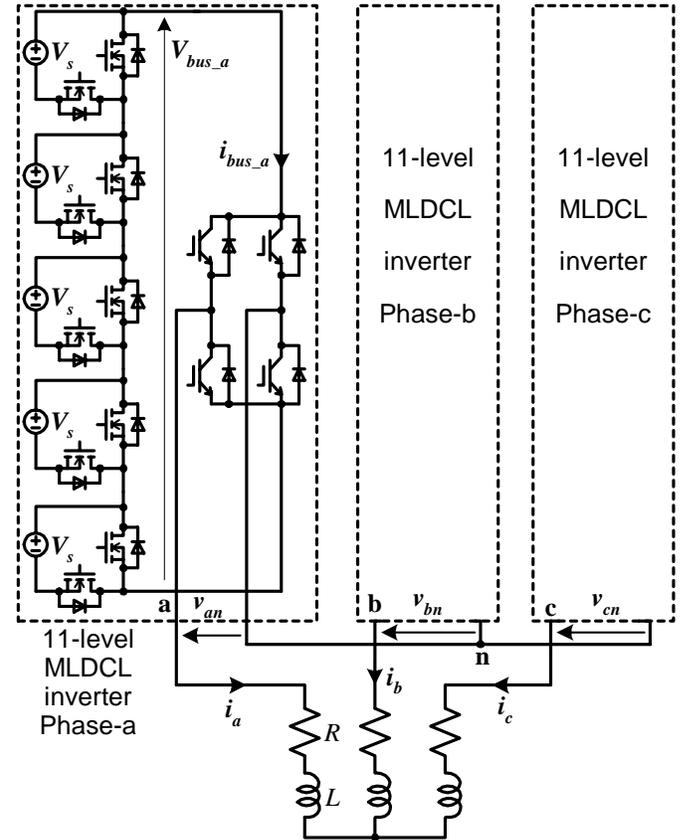


Figure 5. An 11-level half-bridge MLDCI for three-phase configuration with an inductive resistor load.

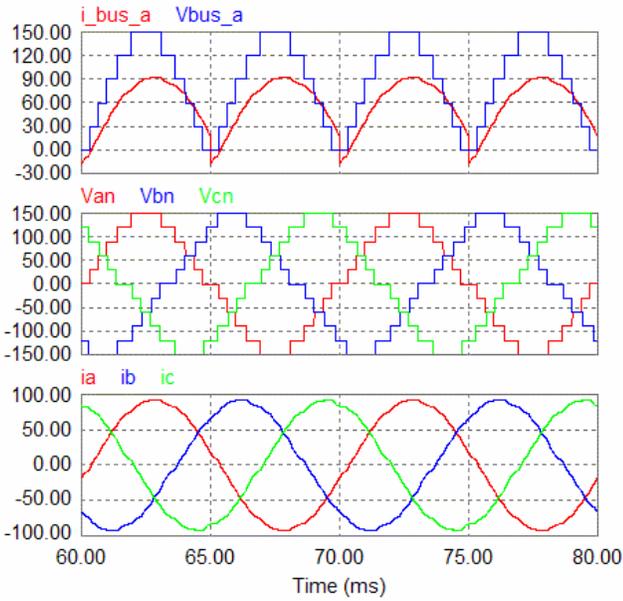


Figure 6. Simulated waveforms of the 11-level half-bridge MLDCLI for three-phase configuration with an inductive resistor load.

Fig. 6 shows simulated phase-a dc bus voltage, V_{bus_a} , current, i_{bus_a} , three phase line-to-neutral voltages, v_{an} , v_{bn} and v_{cn} , and the three phase current, i_a , i_b and i_c , waveforms at an output frequency of 100 Hz. These waveforms confirm the operating principle described in section II.A. Despite the intentionally selected very low inductance, the rms value of the load current ripple is less than 2 % of the fundamental current of 65.5 Arms, clearly demonstrating the superior waveform quality over the two-level PWM inverters.

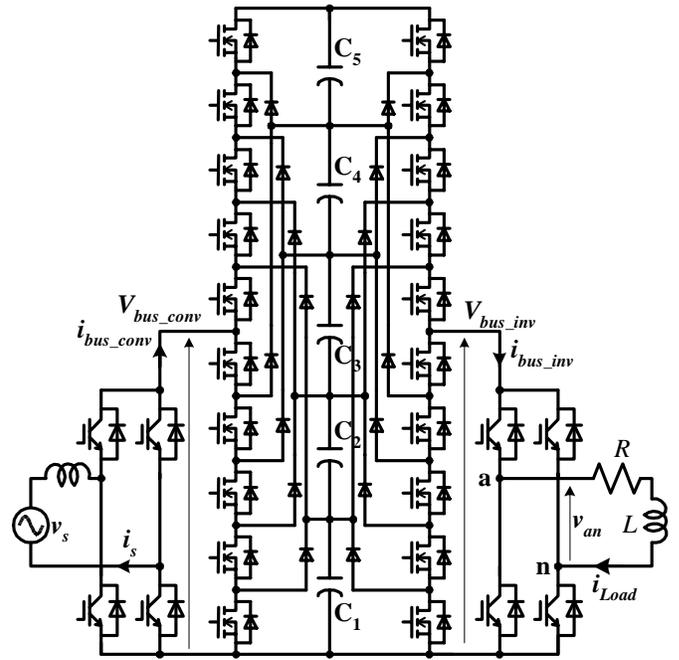
B. Back-to-Back Connection of Two Single-Phase Diode-Clamped MLDCL Inverters

Fig. 7(a) shows a back-to-back connection of two eleven-level single-phase diode-clamped MLDCL inverters, one acting as a converter connected to a voltage source of 100 Vrms at 60 Hz, v_s , through an inductor of 2.9 mH and the other powering an inductive resistor load of 2 Ω and 1.8 mH. Simulated waveforms are given in Fig. 7(b), where i_{bus_inv} and V_{bus_inv} are the bus current and voltage of the inverter, i_{Load} and v_{an} are load current and voltage, i_{bus_conv} and V_{bus_conv} are the bus current and voltage of the converter, i_s and v_s are the source current and voltage, and $V_{c1} \sim V_{c5}$ are the voltages across the capacitors, $C_1 \sim C_5$, respectively. These waveforms clearly verify the operating principle described in section II.B. In addition, the following observations can be stated: (1) near sinusoidal source and load currents are produced, again demonstrating the superior waveform quality of the multilevel inverter over the two-level PWM inverters, and (2) while the capacitor voltages fluctuate at twice the source voltage frequency, they closely track with each other due to the back-to-back connection.

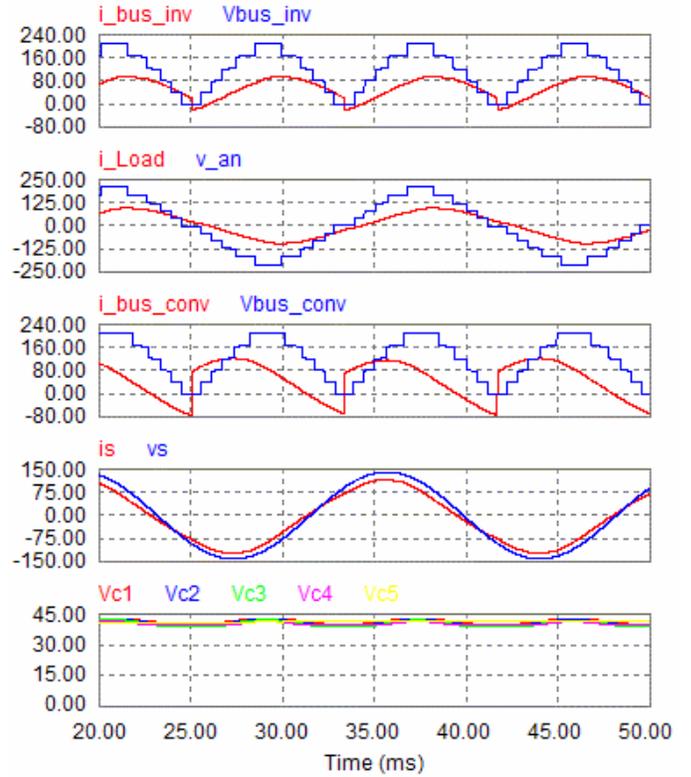
C. Seven-Level Capacitor-Clamped MLDCLI

Fig. 8 shows simulated dc bus voltage and current, load voltage and current waveforms of the seven-level capacitor-

clamped MLDCLI for powering an inductive resistor load, clearly verifying the operating principle described in section II.C.



(a) Back-to-back connection of two 11-level DMLDCLIs.



(b) Simulated voltage and current waveforms.

Figure 7. Simulated waveforms of a back-to-back connection of two 11-level diode-clamped MLDCLIs supplying an inductive resistor load.

D. Testing of a Thirteen-Level MLDCL Inverter

For proof-of-concept, a single-phase thirteen-level half-bridge cell based MLDCL inverter was assembled and tested with an inductive resistor load ($R=13.2 \Omega$, $L=10 \text{ mH}$) as shown in Fig. 9(a). The individual dc sources are obtained by using single-phase diode rectifiers and transformers operating off the utility line. Fig. 9(b) shows typical testing waveforms when the inverter was programmed to produce a near sinusoidal output voltage and the four switches in the SPFB are switching at the fundamental frequency of 100 Hz while the other switches at 200 Hz, twice the fundamental frequency. A near sinusoidal load current with a harmonic distortion factor of less than 1% was produced.

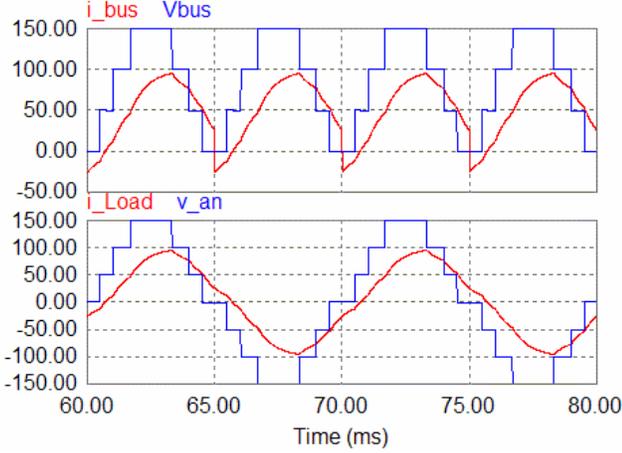
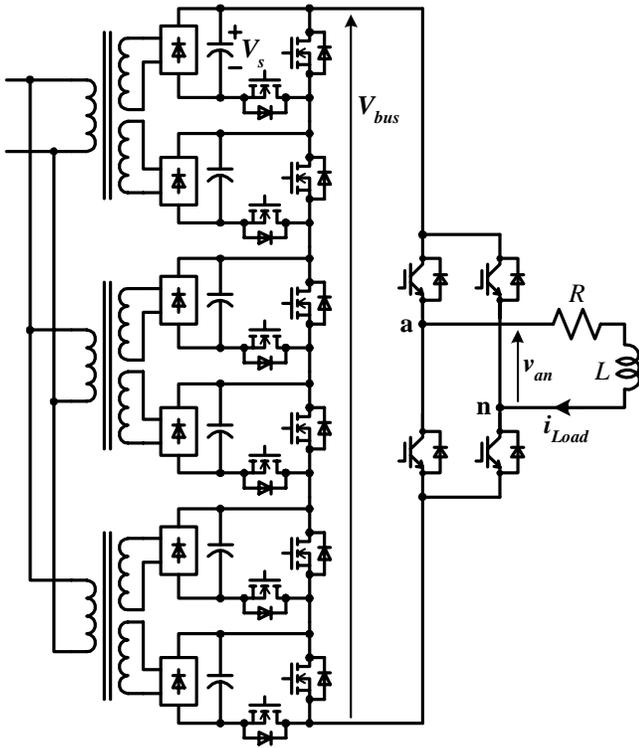
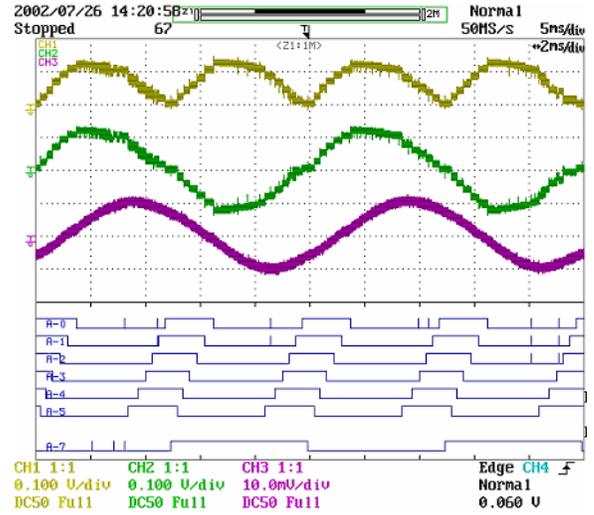


Figure 8. Simulated waveforms of the 7-level capacitor-clamped MLDCLI for single-phase configuration with an inductive resistor load.



(a) Testing setup



(b) Testing waveforms. From top to bottom: V_{bus} : 100V/div, v_{an} : 100V/div, i_{Load} : 5A/div, Gating signals. Time: 2 ms/div

Figure 9. Testing waveforms of a half-bridge cell based 13-level MLDCLI for single-phase configuration with an inductive resistor load.

TABLE III. COMPONET COUNT COMPARISON

	Cascaded		Diode Clamped		Flying Capacitor	
	new	existing	new	existing	new	existing
Switches	$m+3$	$2 \times (m-1)$	$m+3$	$2 \times (m-1)$	$m+3$	$2 \times (m-1)$
Clamping Diodes			$m-3$	$2 \times (m-2)$		
Clamping Capacitors					$(m-3)/2$	$m-2$
Voltage splitting Capacitors			$(m-1)/2$	$m-1$		

IV. CONCLUSIONS

The proposed MLDCL inverters can significantly reduce the component count as the number of voltage levels increases. Table III summarizes the required number of switches, clamping diodes, capacitors of the three proposed new inverters compared with their existing counterparts, for a given number of output voltage level, m .

One application area in the low power range ($< 100 \text{ kW}$) for the MLDCL inverters is in PM motor drives employing a PM motor of very low inductance. The proposed inverters can utilize the fast-switching, low cost low-voltage MOSFETs in the half-bridge cells, the diode-clamped or capacitor-clamped phase legs and IGBTs in the single-phase bridges to dramatically reduce current and torque ripples and to improve motor efficiency by reducing the associated copper and iron losses resulting from the current ripple. These configurations may also be applied in distributed power generation involving fuel cells and photovoltaic cells.

For high-voltage, high-power applications, high-voltage IGBTs or GTOs, switching at the fundamental frequency, can be used in the single-phase bridge inverters, while lower-voltage but fast-switching IGBTs, which may or may not perform PWM, can be employed in the MLDCL sources.

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