

LABORATORY DEMONSTRATION OF THE DUAL MODE INVERTER CONTROL

Jack S. Lawler
The University of Tennessee
Knoxville, Tennessee

John M. Bailey and John W. McKeever
Oak Ridge National Laboratory
Oak Ridge, Tennessee

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ABSTRACT*

Previous theoretical work has shown that when all loss mechanisms are neglected the constant power speed range (CPSR) of a brushless dc motor (BDCM) is infinite when the motor is driven by the dual-mode inverter control (DMIC) [1,2]. In a physical drive, losses, particularly speed-sensitive losses, will limit the CPSR to a finite value. In this paper we report the results of laboratory testing of a low-inductance, 7.5-hp BDCM driven by the DMIC. The speed rating of the test motor rotor limited the upper speed of the testing, and the results show that the CPSR of the test machine is greater than 6:1 when driven by the DMIC. Current wave shape, peak, and rms values remained controlled and within rating over the entire speed range. The laboratory measurements allowed the speed-sensitive losses to be quantified and incorporated into computer simulation models, which then accurately reproduce the results of lab testing. The simulator shows that the limiting CPSR of the test motor is 8:1. These results confirm that the DMIC is capable of driving low-inductance BDCMs over the wide CPSR that would be required in electric vehicle applications.

1. INTRODUCTION

Transmissionless electric passenger vehicles require a constant power speed range (CPSR) of 4:1 or more. Larger electric vehicles, such as heavy trucks, tanks, and other heavy equipment, can require a CPSR of 10:1. All these applications can benefit from use of the brushless dc motor (BDCM) that has high power density and efficiency relative to other motor types. The power density and efficiency of the BDCM is greatest when rare-earth magnet materials such as samarium-cobalt or neodymium-iron-boron are used. The magnetic induction in such motors is higher than in designs using low-strength magnets. Consequently, relatively few turns of copper wire are required in the high-strength magnet designs to achieve the same induced voltage level. Thus, the BDCM designed with rare-earth magnets generally has a "low" internal inductance. The low inductance makes it difficult to drive these machines over a wide CPSR without exceeding the current rating of the motor [1,2,3]. Depending on the inductance, the motor current magnitude at high speed may be several times greater than rated when conventional phase advance (CPA) is used to control the high-speed operation. We have developed an alternative to CPA for driving the BDCM over a wide CPSR, while remaining within the rms current rating of the motor. This alternative is called the dual-mode inverter control (DMIC).

In previous work we have shown that when all drive loss mechanisms are neglected the CPSR of the BDCM is infinite when driven by the DMIC [1,2]. Losses are unavoidable in a physical drive and will limit the CPSR to a finite value. Speed dependent losses such as skin effect in winding resistance, hysteresis and eddy currents, and friction and windage consume progressively more input power as speed increases. Consequently, the extent of the CPSR is limited by the speed-dependent losses when the motor current is constrained to its rating. In this work we report laboratory test results for a low-inductance, 7.5-hp BDCM driven by the DMIC. Dynamometer measurements show that the CPSR is greater than 6:1. The speed rating of the test machine precluded evaluation at higher speeds. Test results

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The corresponding author of this paper is John W. McKeever, a Senior R&D Staff Member with the Oak Ridge National Laboratory. Mr. McKeever's address is National Transportation Research Center, 2360 Cherahala Boulevard, Knoxville, Tennessee 37832; phone 865-946-1316; fax 865-946-1262; and email mckeeverjw@ornl.gov.

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show that the motor current waveform, peak, and rms values remain under control as speed increases.

The laboratory testing allowed quantification of the important speed-sensitive losses of the test motor. These losses were incorporated into simulation models of the DMIC. Simulation results, including the loss effects, are shown to agree with test measurements. Current waveform shape, rms current, and useful output power of the model match the experimental results. The model is then used to show that the CPSR of the test motor is 8:1.

The test motor was not designed to be operated with the DMIC over a wide speed range. For example, the stator laminations are 14 mils thick. The core losses of the motor can be reduced, and the CPSR extended, by using thinner laminations. The proof-of-principle testing reported here is sufficiently encouraging that we have designed and built a 20 kW BDCM specifically for operation with the DMIC. In future work we will report the results of laboratory testing on this new motor.

The remainder of this paper is organized in four sections. In Section 2 we give the parameters of the test motor including speed-dependent losses. Section 3 provides the inverter topology and firing scheme of the DMIC and the motor model used by the simulators. Section 4 contains the test results and compares them with simulated results that include losses. Our conclusions and plans for future work are contained in Section 5.

2. TEST MOTOR PARAMETERS

Let the parameters of the BDCM be denoted by

- p = number of poles
- N_b = base speed in rpm
- E_b = magnitude of the phase-to-neutral back-emf at base speed
- P_r = rated output power
- T_r = rated output torque = $\frac{30 P_r}{\pi N_b}$
- L_s = self-inductance per phase
- L_o = leakage inductance per phase
- M = mutual inductance
- L = equivalent inductance per phase
= $L_s + L_o + M$
- R = winding resistance per phase
- v_{an} = phase A to neutral voltage
- e_{an} = phase A back-emf (to neutral)
- e_{ab} = phase A to phase B back-emf
- N = actual rotor speed in rpm

$$n = \text{relative rotor speed} = \frac{N}{N_b}$$

$$E_{an}(n) = \text{peak phase-to-neutral back-emf at speed } n = n E_b$$

$$E_{ab}(n) = \text{peak phase-to-phase back-emf at speed } n = 2 n E_b$$

$$\begin{aligned} \Omega_b &= \text{base speed in electrical rad/sec} \\ &= \frac{p}{2} \frac{2\pi N_b}{60} \end{aligned}$$

The test motor is a 12-pole, axial gap, 2600 rpm, 49.5-hp, 220-V motor with samarium-cobalt magnets. This motor was not designed for operation significantly above 2600 rpm. To demonstrate the broad CPSR capability of the DMIC, and remain within the safe speed rating of the rotor, testing was conducted with reduced supply voltage. This effectively reduces the base speed of the motor and lowers the power rating. A base speed of 400 rpm was chosen so that a CPSR of 6:1 could be safely demonstrated on the test machine.

Running on a 220 V_{dc} supply, the efficiency of the example motor is approximately 94% at rated conditions. Under the reduced voltage/power conditions of this test, the motor efficiency will be around 70% at base speed and above. We will not dwell on efficiency calculations in this work since its purpose is to confirm the broad CPSR capability of the DMIC. A motor specifically designed for operation with the DMIC has been built and will be tested at a later time to provide a more accurate picture of the efficiency.

At speeds below base speed a hysteresis band current regulator controls the torque of the BDCM. Base speed is the highest speed at which the current regulator can produce rated torque. Rated current is the current required to produce rated torque at base speed, and rated power is the power at rated current when operating at base speed. Above base speed the current regulator becomes ineffective in controlling motor current and the DMIC uses phase advance. The CPSR of the drive is the highest speed at which the phase advance can produce rated useful power at rated current divided by the base speed.

The dc supply voltage is a key parameter affecting the base speed of the motor. An accurate test of the motor CPSR cannot be conducted if the supply voltage is larger than the minimum necessary to supply rated torque at the specified base speed. To establish a base speed of no more than 400 rpm, the motor was tested in the laboratory with the current

regulator disabled and the phase advance set to about 30°. The dc supply voltage was slowly increased until at 41.9 V, the output power measured by the dynamometer equaled 7.5 hp at 400 rpm. This ensured that the supply voltage is less than what would be required in the current regulation mode to support a base speed of 400 rpm. The measured motor rms current at this condition was 212 A, and this was accepted as the current rating of the motor while rated power is 7.5 hp. Even though the true base speed of the test setup is less than 400 rpm, we will use 400 rpm as “the” base speed and our conclusions about the CPSR range of the DMIC will be understated.

In the absence of motor and inverter losses the CPSR of the DMIC-driven BDCM is theoretically infinite. In a practical situation, such as this test, the CPSR will be finite because of winding resistance, inverter losses, and speed sensitive motor losses. Speed-sensitive motor losses include rotational losses such as friction, windage, core losses including hysteresis and eddy current losses, and skin effect increase in winding resistance.

The aggregate of the speed-sensitive core and rotational losses can be measured easily using a dynamometer to drive the de-energized motor. For convenience, the aggregate of these losses is referred to simply as rotational losses. A plot of measured total rotational losses vs rotor speed is shown in Fig. 1.

In addition to skin effect changes, the winding resistance is sensitive to winding temperature. To characterize winding resistance, the laboratory setup included measurement of the total three-phase power entering the motor and rms motor current. When operating near rated rms motor current, the output power measured by the dynamometer plus the appropriate rotational losses from Fig. 1 can be subtracted from the measured total input power to the motor. The resultant is the total copper loss. Dividing the copper loss by three and by the square of the rms motor current yields the per phase winding resistance appropriate for rated current and the speed at which the measurements are made. Test data for the example motor when operating near rated current for speeds of 400, 1215, and 2424 rpm were used to construct the winding resistance vs. speed plot shown in Fig. 2.

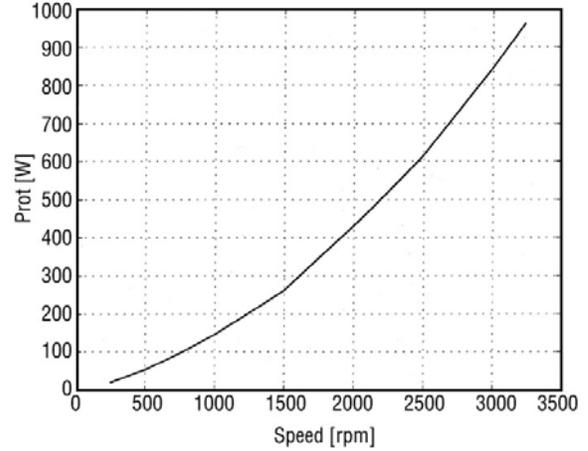


Fig. 1. Measured rotational losses vs rotor speed for the test motor.

The curve of Fig. 2 is a straight line, and for the rotor speed of N (in rpm) the motor winding resistance is given by

$$R = 1.423 \cdot 10^{-2} + 1.433 \cdot 10^{-6} \cdot N \quad \Omega \text{ per phase.} \quad (1)$$

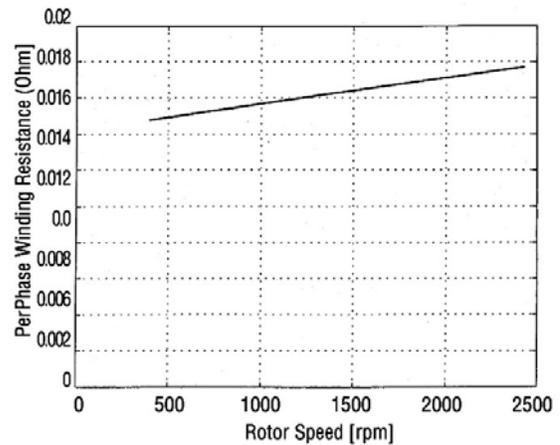


Fig. 2. Winding resistance vs rotor speed for operation at rated current, calculated from measurements at 400, 1215, and 2424 rpm.

The equivalent per-phase inductance of the test motor is 73.6 μH . This value is relatively insensitive to the frequency of operation. However, extensive cables were used to connect the DMIC inverter to the motor, which increased the equivalent inductance to 94 μH per phase.

Important parameters of the example motor, as tested, are:

- $p = 12$ poles
- $N_b =$ base speed = 400 rpm
- $\Omega_b =$ base speed in elec rad/sec
= 251.3 rad/sec
- $L = 94 \mu\text{H}$ per phase
- $R = 0.1423 + 1.433 \cdot 10^{-6} \cdot N$ ohms per phase
- $E_b =$ peak phase-to-neutral
back-emf at base speed
= 11.41 V
- $I_b =$ rated rms current = 212 A
- $P_r =$ rated power
= 5595 W (7.5 hp)
- $T_r =$ rated torque = 133.6 Nm
- $V_{dc} =$ dc supply voltage = 41.9 V

Inverter semiconductor switching frequency during high-speed operation of the DMIC is at the fundamental electrical rate. This rate was 240 Hz or less during the testing of the example motor so that inverter switching losses are small. Conduction losses are important, and their effect is to reduce the supply voltage available at the terminals of the motor. During testing, the line-to-line voltage at the motor terminals was observed using an oscilloscope. It was observed that of the 41.9 V at the dc supply, only 33.6 V was available to the motor. When testing at the 212-A rms current rating, the value of 33.6 V was consistently observed regardless of the motor speed. In our MATLAB and PSPICE simulators, the inverter switching logic of transistors, diodes, and thyristors are represented in detail. However, the devices are modeled as ideal elements. Consequently, in the simulators, the equivalent value of 33.6 Vdc rather than the 41.9 V of the actual supply, represents the supply voltage.

3. DMIC INVERTER TOPOLOGY, FIRING SCHEME, AND MOTOR MODEL

The DMIC inverter topology and motor model used in this work are shown in Fig. 3. The DMIC firing scheme for the phase A semiconductors during high-speed motoring operation are shown in Fig. 4. The firing logic for phases B and C are analogous to that of phase A with delays of one third and two thirds of a cycle respectively. Detailed rationale behind the inverter topology and its firing scheme can be found in companion work [1,2].

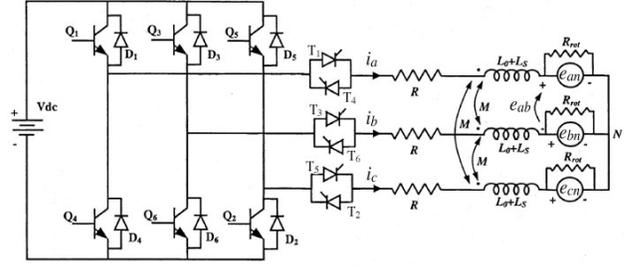


Fig. 3. DMIC inverter topology and BDCM model.

The parameter, R_{rot} , in Fig. 3, is an equivalent resistance representing the aggregate rotational losses of the motor. Since the rotational losses vary with speed, as shown in Fig. 1, the value of R_{rot} changes with rotor rpm. The phase-to-neutral back-emfs are trapezoids with the rms value at relative rotor speed, n , given by

$$V_{rms} = n E_b \sqrt{\frac{7}{9}} \text{ volts.} \quad (2)$$

Combining this with a point from the rotational loss curve of Fig. 1, the value of R_{rot} can be calculated for a given speed as

$$R_{rot} = \frac{3 V_{rms}^2}{P_{rot}}. \quad (3)$$

The simulators use the speed dependent values of R_{rot} and winding resistance R given by Eqs. (3) and (1), respectively.

4. EXPERIMENTAL RESULTS

The main objective of the testing was to show that the DMIC is capable of a CPSR of 6:1. To achieve this objective, dynamometer testing of the example motor was conducted at three speeds; the base speed of 400 rpm, 1215 rpm ($n = 3.0375$), and 2424 rpm ($n = 6.06$). A detailed report on the experimental setup is contained in [4]. At each speed the advance angle was adjusted so that the motor current was close to the specified rated value of 212 A rms. The dynamometer used was a “water brake” type unit which can sustain a steady operating condition but is hard to adjust. Consequently, the experimenters took measurements whenever the motor current was within a few amperes of the specified rating.

The results of the laboratory test are contained in Table 1, which shows the dc supply voltage, rotor rpm, advance angle, blanking angle, rms motor current, and useful output horsepower at the three speed conditions.

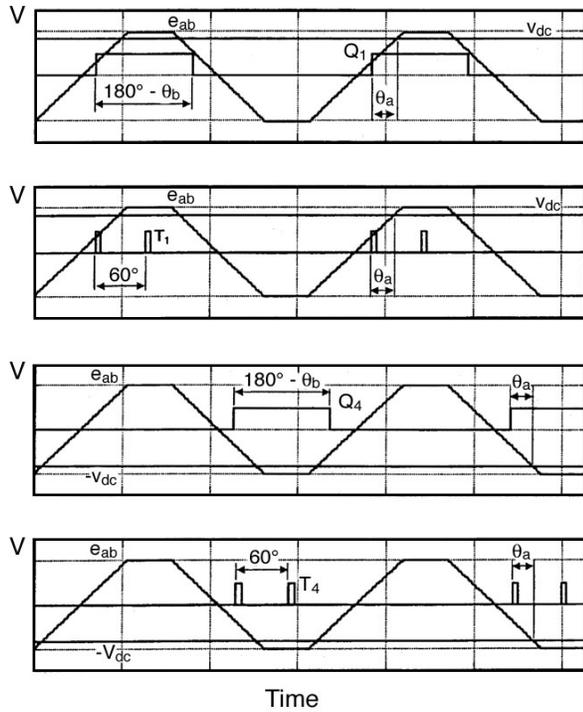


Fig. 4. Firing scheme for phase A semiconductors in high-speed motoring mode.

Table 1. Experimental data for supply voltage, speed, advance angle, blanking angle, rms current, and useful output horsepower

V_{dc} (volts)	N (RPM)	θ_a / θ_b (elec deg)	I_{rms} (A)	P_{out} (hp)
41.9	400 (n = 1)	31.1 / 60	212	7.5
41.9	1215 (n = 3.0375)	49.9 / 20	214	9.27
41.9	2424 (n = 6.06)	46.4 / 20	206	8.12

The experimental data show that the CPSR of the test motor is greater than 6:1 since 8.12 hp is developed at 2424 rpm, relative speed of $n = 6.06$, compared with the 7.5 hp developed at the 400 rpm base speed, relative speed of $n = 1$. Also note that the 9.27 hp developed at a relative speed of 3 is 24% more than the rated power. It is characteristic of the DMIC that greater power can be developed above base speed than at base speed. The amount of additional power depends heavily on the motor inductance.

A blanking angle of 20° was used in the high-speed runs instead of zero. This is done as a safety precaution against inadvertent short circuits of the dc supply.

The motor current waveforms for the three experimental conditions of Table 1 are shown in Fig. 5 part a. The waveforms of Fig. 5 show that the DMIC is able to maintain the current wave shape, peak, and rms values despite increases in motor speed. This is in contrast with the conventional phase advance method where the current magnitude generally increases with speed, resulting in a reduced CPSR [1,2,3].

For comparison, the MATLAB simulator was used to investigate the performance at the same speed/current conditions as in the laboratory experiments. The results are given in Table 2.

Table 2. Simulator data for supply voltage, speed, advance angle, blanking angle, rms current, and useful output horsepower

V_{dc} (volts)	N (RPM)	θ_a / θ_b (elec deg)	I_{rms} (A)	P_{out} (hp)
33.6	400 (n = 1)	31.1 / 60	212	7.48
33.6	1215 (n = 3.0375)	52.2 / 20	214	9.16
33.6	2424 (n = 6.06)	48.6 / 20	206	8.06

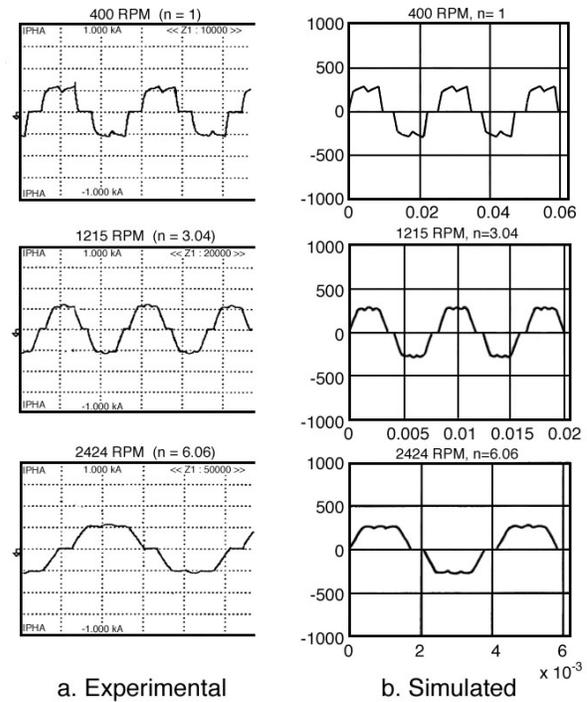


Fig. 5. Comparison of measured and simulated phase A current waveforms.

Comparing Tables 1 and 2 shows that the simulated results agree favorably with the experimental measurements. This confirms that the treatment of inverter, skin effect, and rotational losses used by the simulator, as described previously, are accurate. The simulated current waveforms for the three speed conditions are shown in Fig. 5(b) and have the same wave shape, peak, and rms values as the experimental observations of Fig. 5(a).

Based on the experimental data, we concluded that the DMIC was able to drive the example motor over a CPSR greater than 6:1, but it is not clear how much greater. Concern for the speed rating of the test motor precluded testing at higher speeds. However, the simulator has sufficient accuracy to further investigate the extent of the CPSR of the DMIC when driving the test motor.

The simulator was used to study the performance of the example motor over the entire speed range. Below base speed, the simulator uses hysteresis band current regulation. At base speed and above, the current regulator is ineffective and phase advance controls the motor current. The motor controls were adjusted to produce rated rms current for speeds from 50 rpm through 3200 rpm. The results of the simulations are shown in Fig. 6. The controls of the motor shown in the figure are the set point of the current regulator, I_{set} , the advance angle, θ_a , denoted as “tha” in the figure, and the blanking angle, θ_b , denoted as “thb.” Below base speed, the phase advance is set to zero and the blanking angle is held at 60°. All control is done by adjustment of the current regulator set point, I_{set} . The hysteresis band around I_{set} was ± 5 A. As the speed approaches base speed, the current regulator begins to lose effectiveness and the regulator tries to compensate by increasing the set point. At the base speed, further increases in set point have no effect; in fact, without phase advance the current would begin decreasing no matter how large the current regulator set point might be. Above base speed, the advance regulator becomes active. We have found it convenient to ramp the blanking angle from 60 to 20° between base speed and 1.6 times base speed. As explained in [1,2], reducing the blanking angle increases the commutation time, which in turn, increases power conversion. However, control of the current magnitude and torque production is mainly through the advance angle, θ_a . The effectiveness of the controls is shown in Fig. 6 which indicates that the rms current was maintained at the rated value of 212 for each speed. The power vs speed capability is also

displayed in Fig. 6. For comparison, the rated power of 7.5 hp is marked in the figure. Note that the power produced at rated current exceeds 7.5 hp for all speeds between 400 rpm and 3200 rpm. Thus, the simulator predicts that the CPSR for the example motor is 8:1.

The experimental data of Table 1 are overlaid on the simulated performance in Fig. 6. Experimental data points are marked with an “X.” There is reasonable agreement between simulated and experimental data, which indicates that the treatment of losses in the simulator is accurate and that the CPSR of the test motor is close to 8:1.

A CPSR of 6:1 is more than adequate for many applications. However, heavy-duty electric vehicles might require a CPSR in the range of 10:1. To achieve such a CPSR would require design for small speed-dependent losses.

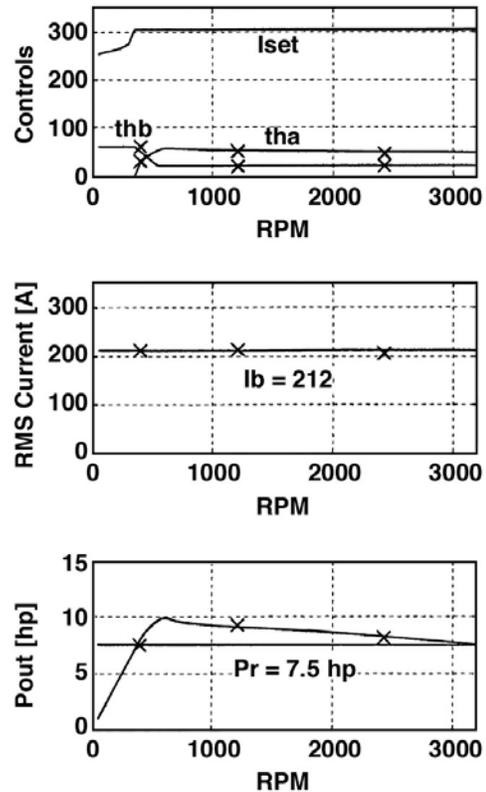


Fig. 6. Simulated (curves) and experimental (X) performance of the test motor from 50 to 3200 rpm.

5. CONCLUSIONS

Laboratory testing has shown that the DMIC can drive a low-inductance BDCM over the wide CPSR

required in electric vehicle applications. The CPSR of a test motor was experimentally shown to be greater than 6:1. Experimentation at speeds greater than six times base speed was precluded by the speed rating of the test motor rotor.

Key factors limiting the CPSR are the speed-dependent losses of the motor. These include hysteresis and eddy currents, friction and windage, and winding resistance increase caused by skin effect. Simulation, including speed-dependent motor losses, shows that the CPSR limit of the test motor is 8:1. The test motor was not designed for broad CPSR operation, and design changes to reduce speed dependent losses will increase the CPSR. For example, the stator laminations of the test motor are 14 mils thick and using a 5-mil lamination would reduce the core losses.

A 20-kW BDCM has been designed and built for broad CPSR operation with the DMIC. This motor will be laboratory tested in the near future.

6. REFERENCES

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