

Development of Prototype Electronics for the BTeV Straw-Tube Tracking Detector

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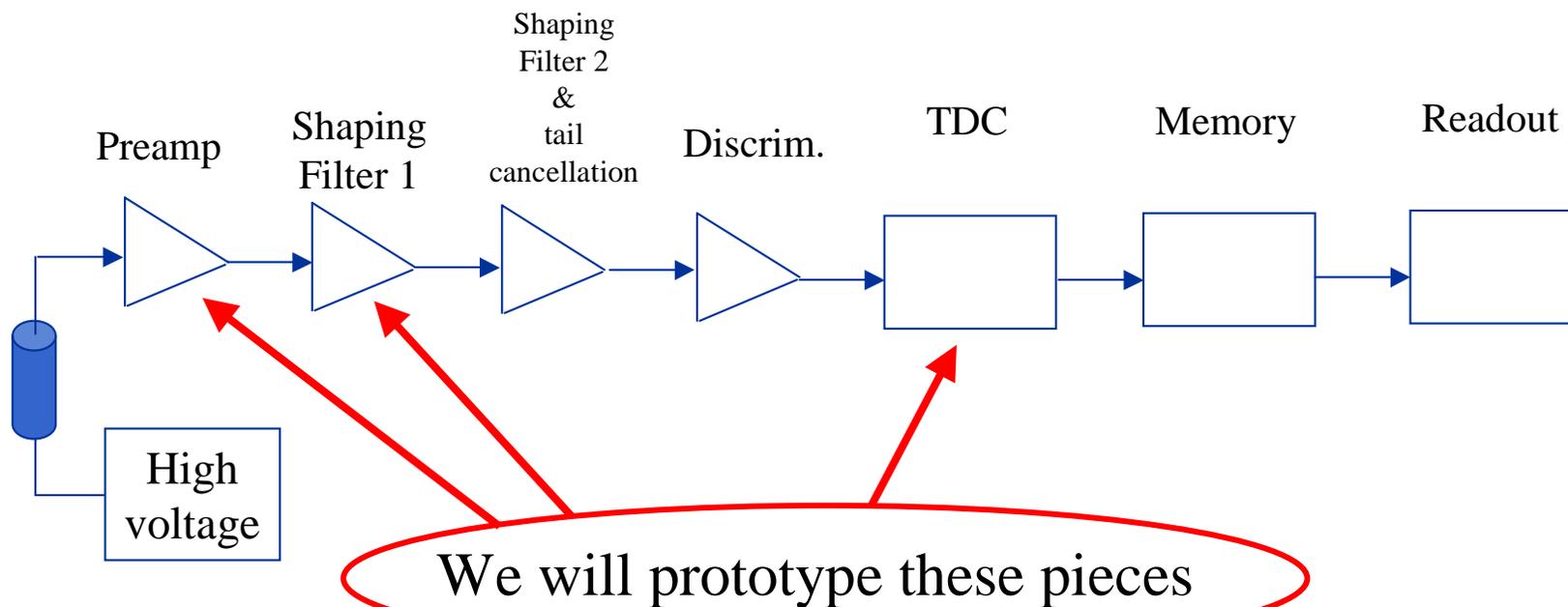


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The system as we presently see it....

- Preamp through discriminator will be one chipset
- TDC and memory will be second chipset

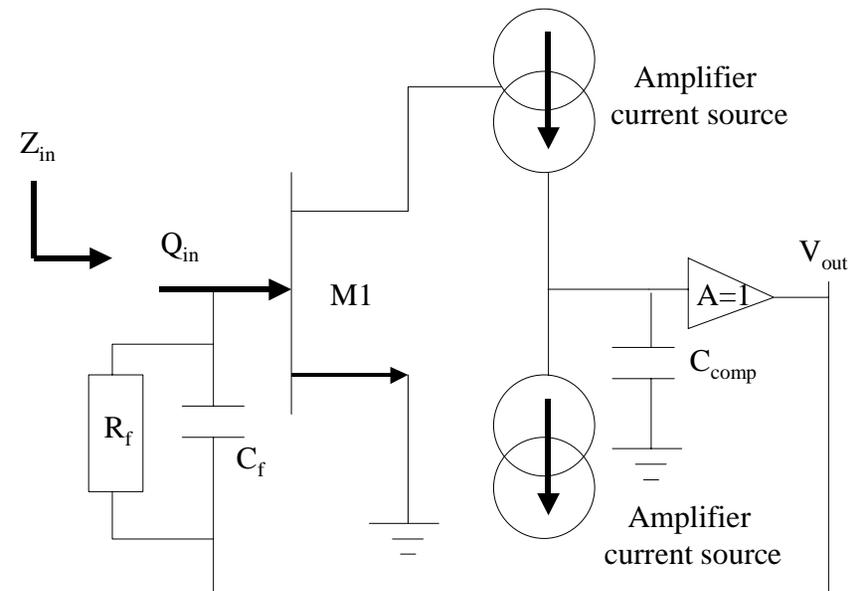


The preamplifier....

- The preamp is used to terminate the transmission line impedance of the straw tube

$$Z_{in} \cong \frac{C_{comp}}{C_f} * \frac{1}{g_m}$$

- This requires a very high bandwidth semiconductor process ($f_t > 30$ GHz)
- Both small feature size CMOS (*Peregrine Semi.* and *Taiwan Semiconductor Manufacturing Corp.*) and SiGe (*Austrian Mikrosystems, IBM*) will be considered



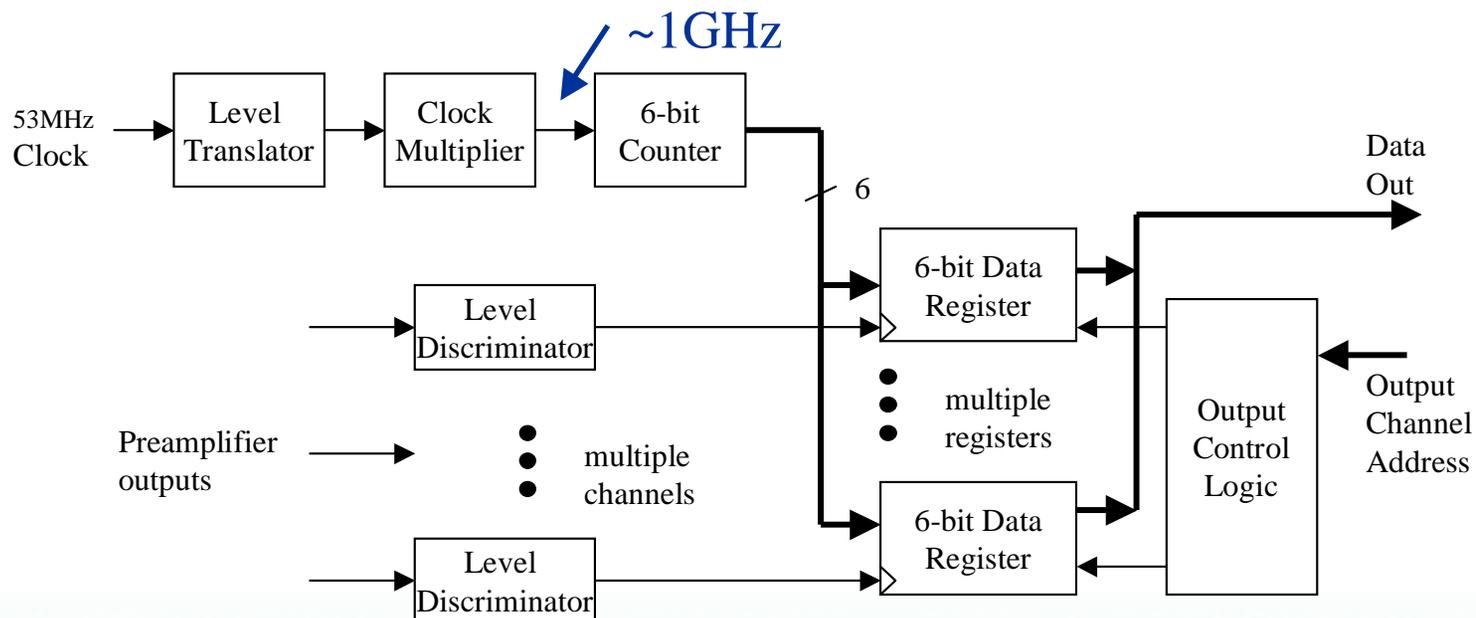
Simplified preamplifier schematic.

Decisions to be made regarding preamplifier

- **Agree upon final noise and signal-processing parameters with collaboration**
- **Finalize radiation dose expectations**
- **Perform preliminary design in**
 - AMS 0.8 μm SiGe
 - Peregrine 0.5 μm SOS
 - TSMC 0.25 μm CMOS
- **Confirm production costs and rules**

Time-to-Digital Converter

- This structure for a TDC time-stamps events to the nearest nanosecond
 - uses clock multiplier originally developed for 915-MHz wireless
 - level discriminators from LHC R&D
- With current IC processes, this can likely be done
 - compactly and power efficiently
 - without the complication of other TDC designs using delay-locked loop time interpolators



We also need to model the straw system

- We need to know the expected rates of data flows and occupancy of the individual channels
- This will require development of the Monte Carlo simulation code
- Code will be based on GEANT blended with BTeV event generator
- Calculate more accurate dose rates
- Compare simulations with test beam results (Spring 2002)