

# Design and Analysis of a Low Cost, High Performance Single Phase UPS System

Gui-Jia Su

Oak Ridge National Laboratory  
National Transportation Research Center  
2360 Cherahala Blvd.  
Knoxville, Tennessee 37932  
Email: [sugi@ornl.gov](mailto:sugi@ornl.gov)

**Abstract** \* -This paper presents design considerations and performance analysis of an on-line low cost, high performance single-phase UPS system based on a novel converter topology. The converter, consisting of an ac-dc/dc-dc boost converter combined with a half bridge inverter, uses only five active switches to realize very desirable features. These include sinusoidal input currents, a common neutral connection – eliminating the requirement of an isolation transformer, capability of voltage balancing control for the dc bus capacitors, low voltage storage battery as well as its charge or discharge regulations. Further, voltage stresses on the switches in the boost converter are reduced to half of those in conventional half bridge converters. A new, unified boost converter control strategy is also presented. Detailed computer simulation and experimental results are included in this paper to demonstrate the superior performances of the UPS system.

## I. INTRODUCTION

Uninterruptible power supply (UPS) systems are being widely used for a wide variety of critical loads including computers, telecommunication systems and medical equipment to overcome the disruption in utility power supply that may occur in the form of outage, voltage sag or voltage surge. Although UPSs have been applied in the past for large computers, increased installation volume of small or personal computers (PCs) has created a tremendous increase in the use of small capacity UPSs operating off a single-phase supply. Given the decreased cost of the computing capability of PCs, these single-phase UPSs are extremely sensitive to cost.

On-line systems are preferred where highly reliable uninterruptible power supply is required. Among various topologies for the on-line UPS systems of 5 kVA and lower ratings reported in the literature [1][2], UPS systems based on a half bridge converter combined with a half bridge inverter, as shown in Fig. 1, have attracted attention in recent development for applications in computer and telecommunication systems. Compared with systems based on full bridge converters with a high frequency or commercial ac line fre-

quency isolation transformer [3], the half bridge topology offers several advantages including a simple power conversion circuit with possibly the least switching device count and no need of an isolation transformer. Adding other desirable features such as sinusoidal ac line currents with unity power factor, and load regulation with non-linear loads, the half bridge topology can thus provide the potential for realizing compact, low cost and high performance systems.

While directly connecting the storage battery to the dc bus results in a very simple system, many battery cells connected in series are required to maintain a high dc bus voltage, which is usually raised to at least twice the peak line voltage to shape the input current waveform. This high voltage storage battery requirement leads to increased cost and reduced reliability, since for a given storage capacity the cost rises but the reliability decreases as the number of storage batteries increase. Further, during battery powered operations, voltages across each of the dc bus capacitors can become unequal when a load draws a different amount of power between the positive or negative half cycles. To make the situation even worse, once the voltages become unbalanced, it is hard to correct them during the battery powered operation period since the battery current always charges the two capacitors in series. This can cause difficulties for the inverter in the control of output voltage and often leads to a degraded quality of voltage waveform. A solution is required for many applications since short-term unbalanced loading can not be avoided during load transient periods, for instance, at the first few cycles of starting a load with a capacitive input diode rectifier or a load with a transformer.

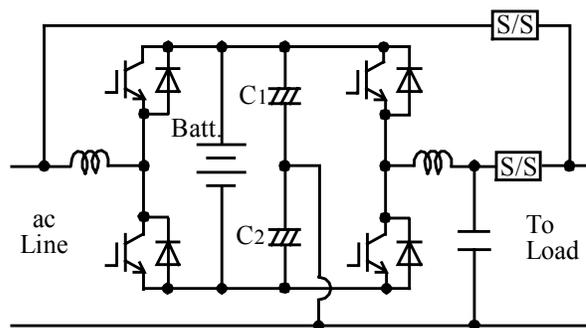


Fig. 1. Single-phase UPS system based on half bridge converters.

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Several schemes have been reported to overcome the high battery voltage issues. One approach is to add a bi-directional chopper circuit for connecting a low voltage battery to the dc bus [4]. The bi-directional chopper steps down the dc bus voltage for charging the battery, or steps up the battery voltage to support the dc bus during ac line outages. A low voltage battery can thus be adapted at the expense of a bi-directional chopper. Moreover, all six switches are exposed to a boosted high dc bus voltage – around 350 V for a 100 V ac line, causing increased voltage stress and switching losses.

In another approach, an auxiliary full-bridge inverter is utilized to connect a low voltage battery to the line input side [5]. Upon detecting ac line failure, The control circuit brings the battery on line by synchronizing the auxiliary inverter with the UPS output voltage. This arrangement requires at least four additional switches and a dedicated battery charger.

Taking advantage of the fact that net power flow in most UPS applications is completely unidirectional, i.e. from ac line to load, new approaches have been proposed to realizing single-phase on-line UPS systems. A single switch boost converter performing ac-dc conversion (during normal operation) or dc-dc conversion (during battery powered operation) is introduced in [6] to replace the half bridge converter in Fig. 1. Combined with a half bridge inverter, this topology maintains the benefits inherent in the half bridge scheme and provides other desirable features such as reduced switch count (only four active switches) and low voltage battery. The drawback of the scheme is that it is incapable of correcting possible capacitors' voltage unbalance during battery powered operation. A new boost converter is proposed in [7] to overcome the drawback of the scheme in [6]. The new converter uses only five active switches and allows full control of the ac line currents, load voltages, battery charge/discharge regulations, and voltage unbalance correction of dc bus capacitors. Moreover, the two switches in the

boost converter have greatly reduced voltage stresses, contributing to decreased switching loss and improved reliability. The system operates with a near unity input power factor, and delivers a high quality sinusoidal voltage waveform to loads. This paper presents a design and performance analysis of an on-line low cost, high performance single-phase UPS system based on the novel converter topology.

## II. DESCRIPTION OF THE SINGLE PHASE UPS SYSTEM

### A. Configuration of the Single Phase UPS

The schematic of the converter for single phase UPS systems is shown in Fig. 2, which mainly consists of an ac-dc or dc-dc boost converter, a half bridge PWM inverter and a step-down chopper to charge the battery. Switches  $S_1$ ,  $S_2$  and inductor  $L_1$  plus diodes  $D_1 \sim D_5$  form an ac-dc boost converter to obtain sinusoidal ac line currents when operating from ac line, or a dc-dc boost converter to support the dc bus voltage from the storage battery during line outages. The step-down chopper consisting of switch  $S_3$ , diodes  $D_6 \sim D_8$ , and inductor  $L_2$  performs the charge control for the storage battery. Switches  $S_4$  and  $S_5$ , capacitors  $C_1$  and  $C_2$  construct a half bridge inverter for supplying loads. It should be mentioned that the three diodes ( $D_1$ ,  $D_2$  and  $D_6$ ) can be eliminated if voltage-controlled switching devices with reverse voltage blocking capability are available, thus further reducing parts count and cost.

Two additional switches,  $S_a$  and  $S_b$ , are used to transfer the input for the boost converter between ac line and storage battery. Either static switches or electromagnetic contacts may be used. In addition, two by-pass switches (S/S) for reverting to ac line in the event of UPS failure or overload are also employed. Static switches are used for realizing minimum transfer time.

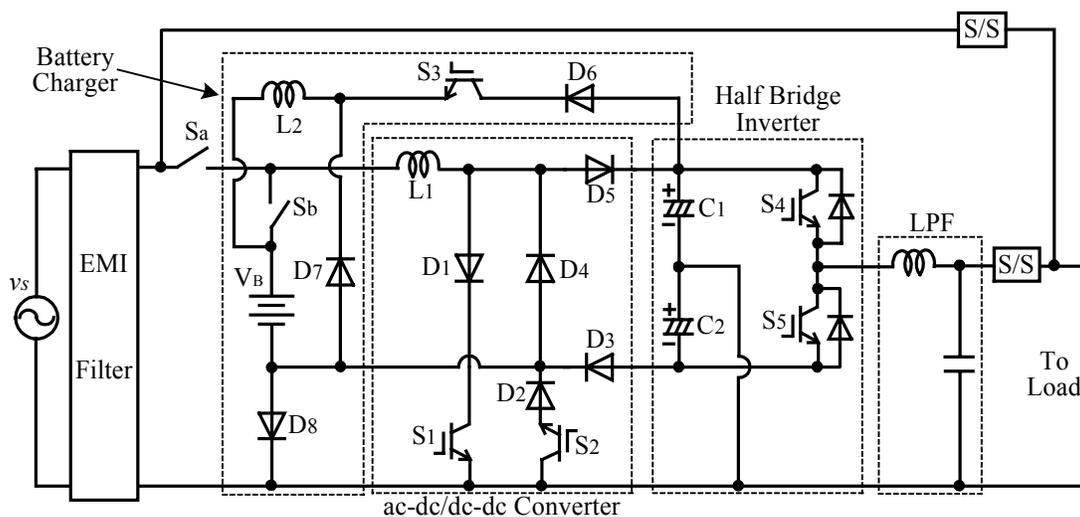


Fig. 2. Schematic of proposed single-phase UPS system.

## B. Boost Converter Operation Modes

The operation of the ac-dc or dc-dc boost converter can be divided into four normal operation modes for operating from ac line and three battery-powered operation modes.

1) *Normal operation modes*: switch  $S_a$  is kept on and  $S_b$  off. The current in the inductor  $L_1$  is forced to follow a sinusoidal template by the PWM control of the ac-dc boost converter while maintaining a constant dc bus voltage. Switch  $S_1$  is used for current regulation during the positive half cycles of the ac line voltage  $v_s$  and switch  $S_2$  is used during the negative half cycles.

If switch  $S_1$  is turned on for positive  $v_s$ , a current is produced in the path of  $v_s \rightarrow L_1 \rightarrow D_1 \rightarrow S_1 \rightarrow v_s$ , storing energy in the inductor  $L_1$  (denoted as normal operation mode 1), ignoring the EMI filter for simplifying the discussion. Then turning off  $S_1$  changes the current path and transfers power from the ac line to dc bus. A current is also provided for charging the upper dc capacitor  $C_1$  through the path of  $v_s \rightarrow L_1 \rightarrow D_5 \rightarrow C_1 \rightarrow v_s$  (normal mode 2). Similarly, for negative  $v_s$  two other operation modes can be established by the control of switch  $S_2$  (identified as normal operation mode 3 with  $S_2$  on or as normal mode 4 with  $S_2$  off). The lower dc capacitor  $C_2$  is charged during mode 4 with a current flowing in the path of  $v_s \rightarrow C_2 \rightarrow D_3 \rightarrow D_4 \rightarrow L_1 \rightarrow v_s$ .

2) *Battery powered operation modes*: Upon identifying failure of the ac line, switch  $S_a$  is turned off and  $S_b$  on, transferring the input from the ac line to the storage battery for the boost converter, which now functions as a dc-dc step-up chopper. To support the dc bus voltage, both switches  $S_1$  and  $S_2$  are first turned on, generating a current through the path of  $V_B \rightarrow L_1 \rightarrow D_1 \rightarrow S_1 \rightarrow S_2 \rightarrow D_2 \rightarrow V_B$  and storing energy in the inductor  $L_1$  (battery powered mode 1). To avoid charging the two dc bus capacitors simultaneously for preventing unbalanced capacitor voltages and to reduce voltage stresses on the switches, it is preferred to turn off only one of the two switches. Selection of which one to turn off depends on which of the two capacitors needs to be charged. To charge the upper capacitor  $C_1$ ,  $S_1$  is turned off (identified as battery powered mode 2). Part of the energy stored in the battery and  $L_1$  is then transferred to the load through the dc bus, and a current for charging the upper dc bus capacitor is produced following the path of  $V_B \rightarrow L_1 \rightarrow D_5 \rightarrow C_1 \rightarrow S_2 \rightarrow D_2 \rightarrow V_B$ . Otherwise,  $S_2$  is turned off for charging the lower capacitor  $C_2$  (denoted as battery powered mode 3). The charging current is produced in the path of  $V_B \rightarrow L_1 \rightarrow D_1 \rightarrow S_1 \rightarrow C_2 \rightarrow D_3 \rightarrow V_B$ . The capability of selectively charging the capacitors is an important feature of the new boost converter since the two capacitor voltages can now be kept well balanced even if a load draws an unbalanced power for the positive and negative half cycles, which may occur during a load transient period.

## C. Battery charge regulation modes

In addition, three modes for battery charge regulation occur simultaneously with the normal operation modes.

The charge regulation of the battery is achieved by the control of switch  $S_3$  during the normal operation modes. There are two possible current paths for charging the battery by turning on  $S_3$ , depending on which normal operation mode is involved. Turning on  $S_3$  during each one of the first three normal operation modes results in a charging current flowing in the path of  $C_1 \rightarrow D_6 \rightarrow S_3 \rightarrow L_2 \rightarrow V_B \rightarrow D_8 \rightarrow C_1$  (charge regulation mode 1). On the other hand, if  $S_3$  is turned on in the normal mode 4, a charging current is provided in the path of  $C_1 \rightarrow D_6 \rightarrow S_3 \rightarrow L_2 \rightarrow V_B \rightarrow D_4 \rightarrow L_1 \rightarrow v_s \rightarrow C_1$  (battery charge regulation mode 2). Then turning off  $S_3$  releases the energy stored in  $L_2$  to the battery (charge regulation mode 3).

This topology provides several advantages over conventional schemes worthy of mentioning. It is apparent that the proposed boost converter possesses no possibility of shoot-through faults, which can happen in half bridge converters. From the above discussion, it is also revealed that voltage stresses on the switches  $S_1$  and  $S_2$  are reduced to half the dc bus voltage, compared again with the case of conventional half bridge converters where all switches are exposed to full dc bus voltage. This feature will reduce the switching losses and improve the reliability. In fact, the ac-dc conversion efficiency can also be improved over half bridge converters despite the additional diodes, as will be shown later.

## III. UNIFIED BOOST CONVERTER CONTROL STRATEGY

A number of control strategies for shaping input current with a boost converter are reported in the literature [8][9][10]. Most of the reported control algorithms are for boost converters with a full-wave rectifier at the front end and thus can not be readily applied to the new converter due to differences in the circuit configuration. In addition, possible voltage unbalance across the dc bus capacitors in a half-bridge inverter must be considered. A carrier based pulse width modulation (PWM) method is adapted for the new boost converter, which shares the triangular carrier with the half-bridge inverter controller. Voltage unbalance correction was initially accomplished with two different control strategies; one for the normal operation modes and the other for the battery powered operation modes [7]. While that approach works very well, it requires additional work on the controller design and implementation. A unified, straightforward control strategy is therefore presented here.

### A. Unified Control Strategy

Considering the fact that only the voltage of one dc bus capacitor can be controlled during either of the positive or negative periods of the line voltage when the converter is powered off a line, it is possible to separate the dc bus voltage

controller so that each capacitor has its own controller, as shown in Fig. 3. Since the two controllers ( $Gv$ ) are identical, it does not require additional design work. More importantly, this approach inherently takes care of the voltage unbalance correction. The same controller also works in battery powered operation modes, thus a unified control is achieved for both the normal and battery powered operations.

A low speed proportional-integral (PI) controller ( $Gv$ ) is used to regulate the dc capacitor voltages. The two PI regulators produce a current reference for the positive and negative half cycles of the sinusoidal templates, respectively. The line voltage ( $v_s$ ) serves as the template for normal operation modes and as does the inverter output voltage ( $v_{ot}$ ) for battery powered operation modes. A multiplexer is used to switch between the two current references according to the signs of the sinusoidal templates.

In the normal modes, the PI-produced references are further multiplied with the sinusoidal template before feeding to the current regulator ( $Gc$ ), which is a proportional controller. In addition, a rectangular signal synchronized with the line voltage is injected into the current reference to help shape the current waveform around zero-crossings of ac line voltage. The output of the current regulator is then compared with a triangular carrier to generate PWM gate signals for the control of the switches  $S_1$  and  $S_2$ .

Upon detection of a power failure, the controller is switched to battery powered operation. The differences of the control systems between the normal and battery powered operation modes are mainly in the gating logic for distributing the PWM signals to the switches. In normal operation modes when  $S_1$  is performing PWM,  $S_2$  is kept off for the positive half cycles of  $v_s$ , and vice versa for the negative half cycles. On the contrary, in the battery powered operations when  $S_1$  is performing PWM,  $S_2$  is kept on for the positive half cycles of  $v_{ot}$ , and vice versa for the negative half cycles. Obviously, the current shaping injection is not required for the battery powered operations.

It should be mentioned that the same gating logic for the battery powered operation could be used for the normal operation since keeping one of the switches on while the other one is doing PWM does not interfere with the operation of the converter, albeit producing additional loss in the associated gate drive circuit. Using the same gating logic can further unify the controller.

### B. Controller Design Considerations

Since the lowest frequency of the dc bus capacitor voltages are the same as the line voltage frequency, the PI controller ( $Gv$ ) should have a large time constant to produce a constant current reference. Otherwise, a varying current reference will increase the current distortion. In contrast, the response of the current controller ( $Gc$ ) needs be as fast as possible to force the input current to follow the sinusoidal voltage wave.

Unlike the half-bridge converter shown in Fig. 1, the dc bus capacitors in the proposed boost converter do not participate in the current boosting phase when the switch is on. Consequently, the switch has to be kept conducting so that there is sufficient voltage available around the zero crossings of the ac line voltage for shaping the current waveform. To accomplish this, the gain of the current regulator must be very large since the current error is nearly zero around the zero crossings. Unfortunately, this high gain controller will make the system unstable because the ripple components of the current and other noises originating in the control circuits will be amplified to a level that can not be ignored. A wave shaping compensation signal is therefore injected into the current reference to overcome the high gain related problems. The signal is a rectangular wave derived from the zero-crossings of  $v_s$ , and is added to the current reference after passing a gain element  $kc$  as shown in the control block diagram. Assuming unity amplitude of the rectangular wave,  $kc$  is determined by

$$kc = \frac{M_{\max} V_{tri}}{k_{Gc}}$$

where  $M_{\max}$ ,  $V_{tri}$  and  $k_{Gc}$  are the maximum modulation index, the amplitude of the triangular carrier wave and the gain of the current controller, respectively. The purpose of  $kc$  is to guarantee that the current controller will produce the maximum duty ratio around the zero-crossings.

### C. Simulation Results

A 1 kVA UPS system is designed to demonstrate the performance described in detail in the following section. Extensive computer simulation is carried out using a detailed circuit simulator to help design the controller for the UPS system.

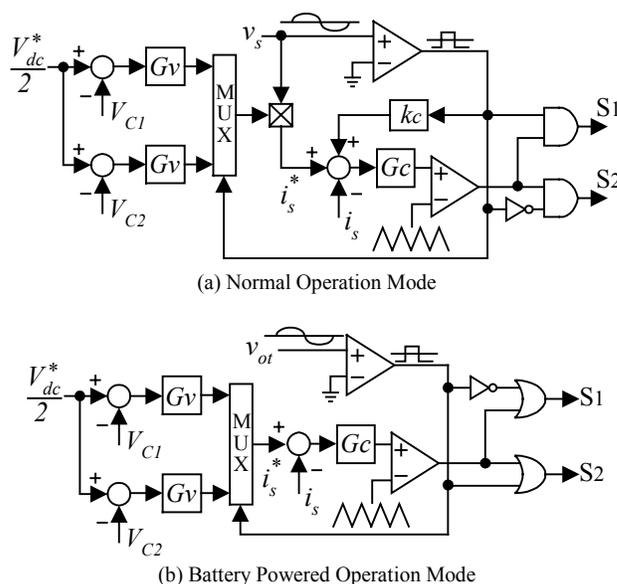
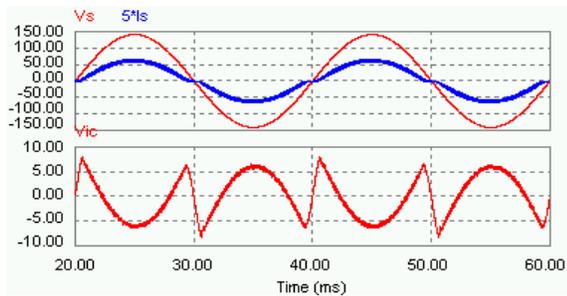
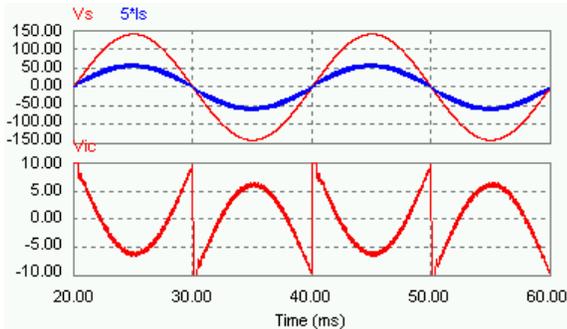


Fig. 3. ac-dc/dc-dc boost converter control block diagrams.

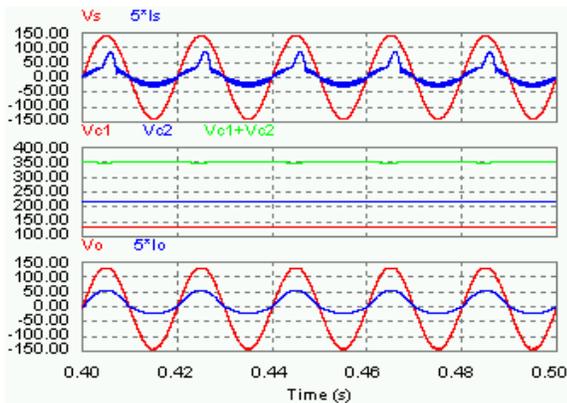


(a) Without wave shaping compensation

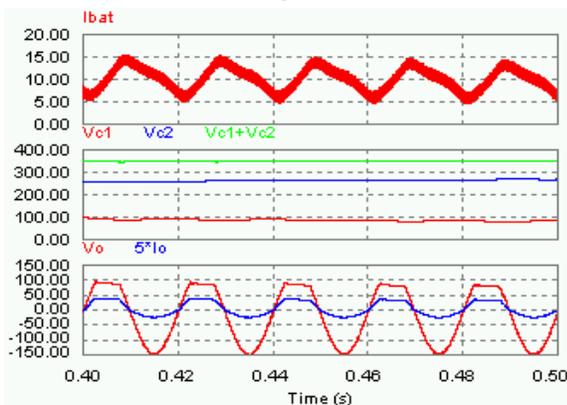


(b) With wave shaping compensation

Fig. 4. Simulated input current waveform improvement. ( $V_s$ : line voltage,  $I_s$ : input current,  $V_{ic}$ : current controller output)

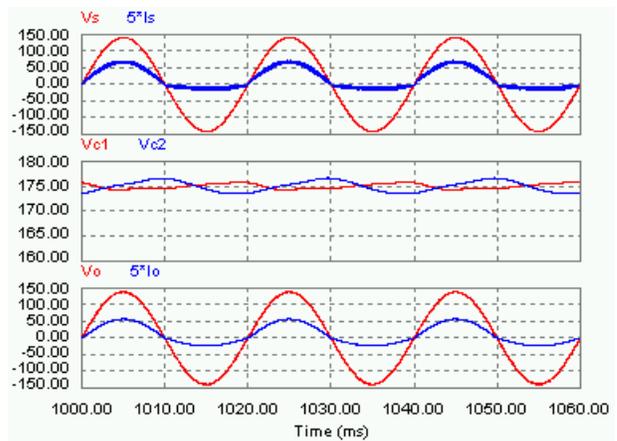


(a) Normal operation mode

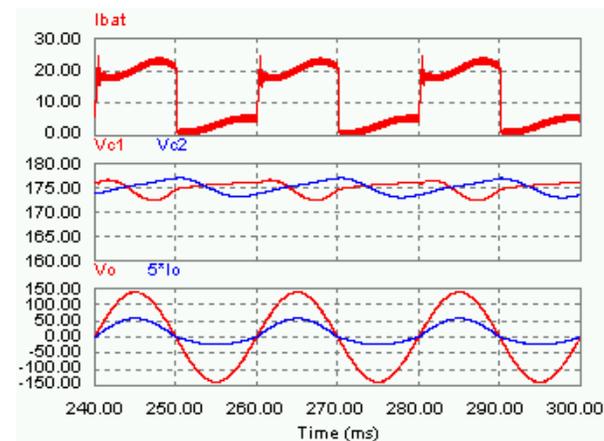


(b) Battery powered operation mode

Fig. 5. Unbalanced dc bus capacitor voltages for an unbalanced load without unbalance correction. ( $V_s$ : line voltage,  $I_s$ : input current,  $V_{c1}$ : upper capacitor voltage,  $V_{c2}$ : lower capacitor voltage,  $I_{bat}$ : battery current,  $V_o$ ,  $I_o$ : output voltage and current)



(a) Normal operation mode



(b) Battery powered operation mode

Fig. 6. Balanced dc bus capacitor voltages for an unbalanced load with unbalance correction. ( $V_s$ : line voltage,  $I_s$ : input current,  $V_{c1}$ : upper capacitor voltage,  $V_{c2}$ : lower capacitor voltage,  $I_{bat}$ : battery current,  $V_o$ ,  $I_o$ : output voltage and current)

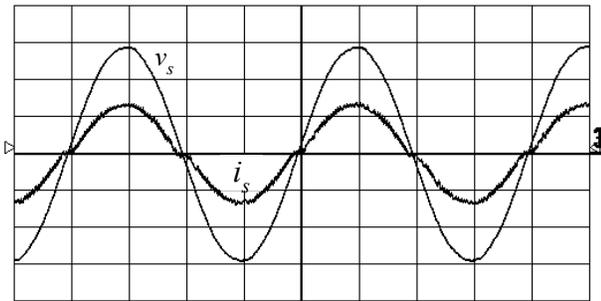
Fig. 4 shows the input voltage and current waveforms. Without injecting the current shaping compensation signal, the input current can not follow the input voltage around the zero crossings as indicated by the flat segments on the current waveform in (a). These segments are eliminated when the compensation signal is injected. The current controller output,  $V_{ic}$ , is also depicted in the figure to show the effectiveness of the current shaping compensation scheme.

Fig. 5 and 6 show the waveforms for both the normal and battery powered operations when an unbalanced load is connected to the inverter. When a single dc bus voltage controller is incorporated, the voltages across the upper and lower dc bus capacitors are unbalanced although the whole dc bus voltage can be maintained, as shown in Fig. 5. While the inverter can produce a balanced voltage in the normal operation modes, this output voltage collapses if powered from the battery because the lower capacitor voltage drops below the required peak output voltage. With the unified controller, the capacitors' voltages are kept balanced regardless of the unbalanced load as shown in Fig. 6.

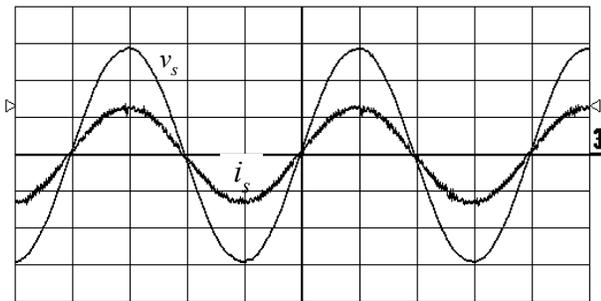
#### IV. A 1 kW UPS DESIGN EXAMPLE AND EXPERIMENTAL RESULTS

A 1 kVA UPS systems has been designed with consideration of cost, efficiency, and complexity. IGBTs were used at a switching frequency of 18 kHz, and a battery bank with a rated voltage of 48 V was employed to demonstrate operation performances at ac line outages. The dc bus voltage was set at 360V to guarantee a high power factor for the specified range of input line voltages (100Vrms, +10%, -15%). Selection of the inductance of  $L_1$  was based on the ripple requirements when operating from the low voltage battery since it produces higher current ripple than the normal operation modes.

Fig. 7 shows input current waveforms with the associated line voltage before and after using the wave-shaping compensation at a rated load power. While a zero-current flat zone around the zero-crossings can be observed in the current waveform without the compensation as shown in figure 7 (a), it is replaced by a sinusoidal current after compensation, confirming the efficacy of the wave-shaping compensation technique. Analysis of the spectra (not shown here) revealed that the lower order harmonic components are significantly reduced with the compensation. Consequently, the total harmonic distortion (THD) is decreased from 7.1 % to 1.6 %.



(a) Without compensation (THD=7.1%)



(b) With compensation (THD=1.6%)

Fig. 7. Input current and its spectrum. Time scale: 5ms/div

$v_s$ : input voltage (50V/div),  $i_s$ : input current (10A/div)

Fig. 8 gives a detailed comparison of measured THD and input power factor (pf) versus output power. The THD is greatly reduced to below 5.0 % for load power over 150 W by the use of the wave-shaping compensation technique. It can be seen that the amount of improvement on THD and pf become larger as output power decreases, which is a favorable

feature for UPSs that operate with loads drawing much lower power than the rated UPS capacity most of the time.

Fig. 9 depicts a comparison of measured overall efficiency at resistive loads between the new UPS system and a conventional scheme using a half bridge converter at the ac-dc power conversion stage. While the maximum efficiency with resistive load is 87.1 % for the conventional system, it is increased to 87.7 % for the proposed one. Again, it can be seen that the efficiency gains more improvement as load power decreases. This can be explained by considering the weight of switching loss against conduction loss. Since it becomes higher as load power decreases, and so is the improvement on efficiency.

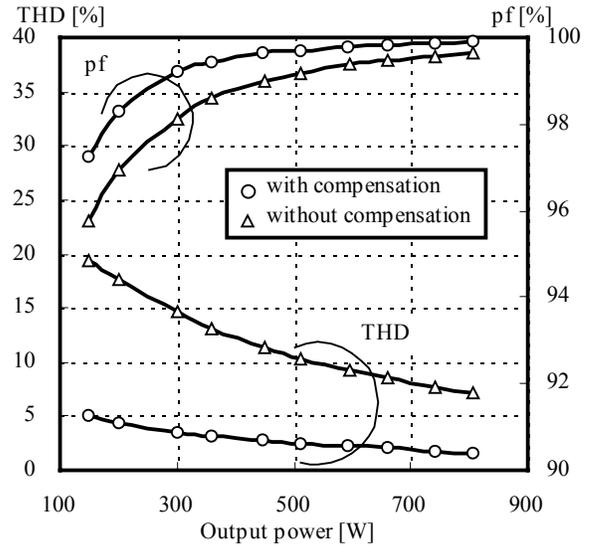


Fig. 8. Measured THD and pf vs. output power.

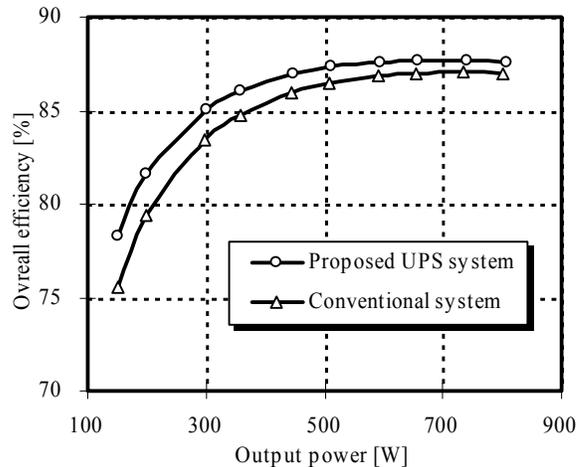


Fig. 9. Comparison of measured efficiency vs. output power.

To demonstrate the voltage balancing capability for dc bus capacitors, typical waveforms of output voltage, output current and dc bus capacitor voltages for an unbalanced load are

given in Fig. 10, where (a) is for normal operation and (b) is for battery powered operation. It can be seen that even though the load draws different currents for positive and negative half cycles; voltages across the upper and lower capacitor are well balanced, and thus a balanced output voltage is obtained.

### V. CONCLUSIONS

The advantages of the new converter topology for UPS applications over the conventional schemes based on the half-bridge converter for ac-dc power conversion can be summarized as follows;

- Fewer active switches,
- Capability of voltage balancing control for the dc bus capacitors,
- Reduced voltage stress on the switches in the boost converter,
- Improved efficiency and reliability.

The new UPS system also has other desirable features including sinusoidal ac line currents with near unity power factor, a common neutral connection, a high quality sinusoidal load voltage even with non-linear load, and a low voltage storage battery. Since the cost of diodes is much lower than that of switching devices like IGBTs, the cost penalty of the increased number of diodes can be offset by the reduced number of active switches in the proposed converter.

The unified control strategy is able to streamline the controller design and implementation. High performances of the proposed scheme is clearly demonstrated by simulation and experimental results.

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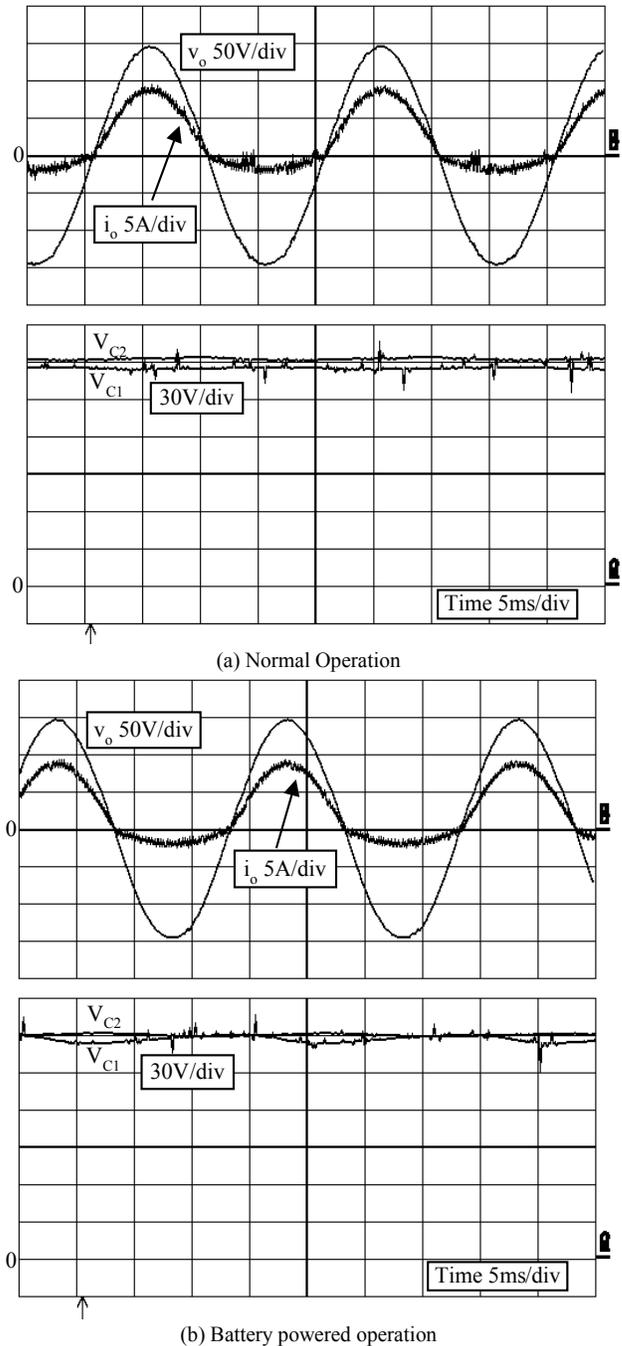


Fig. 10. Typical waveforms for an unbalanced load.