Development of high-efficiency commercial-ready Si solar cells for cost-effective PV

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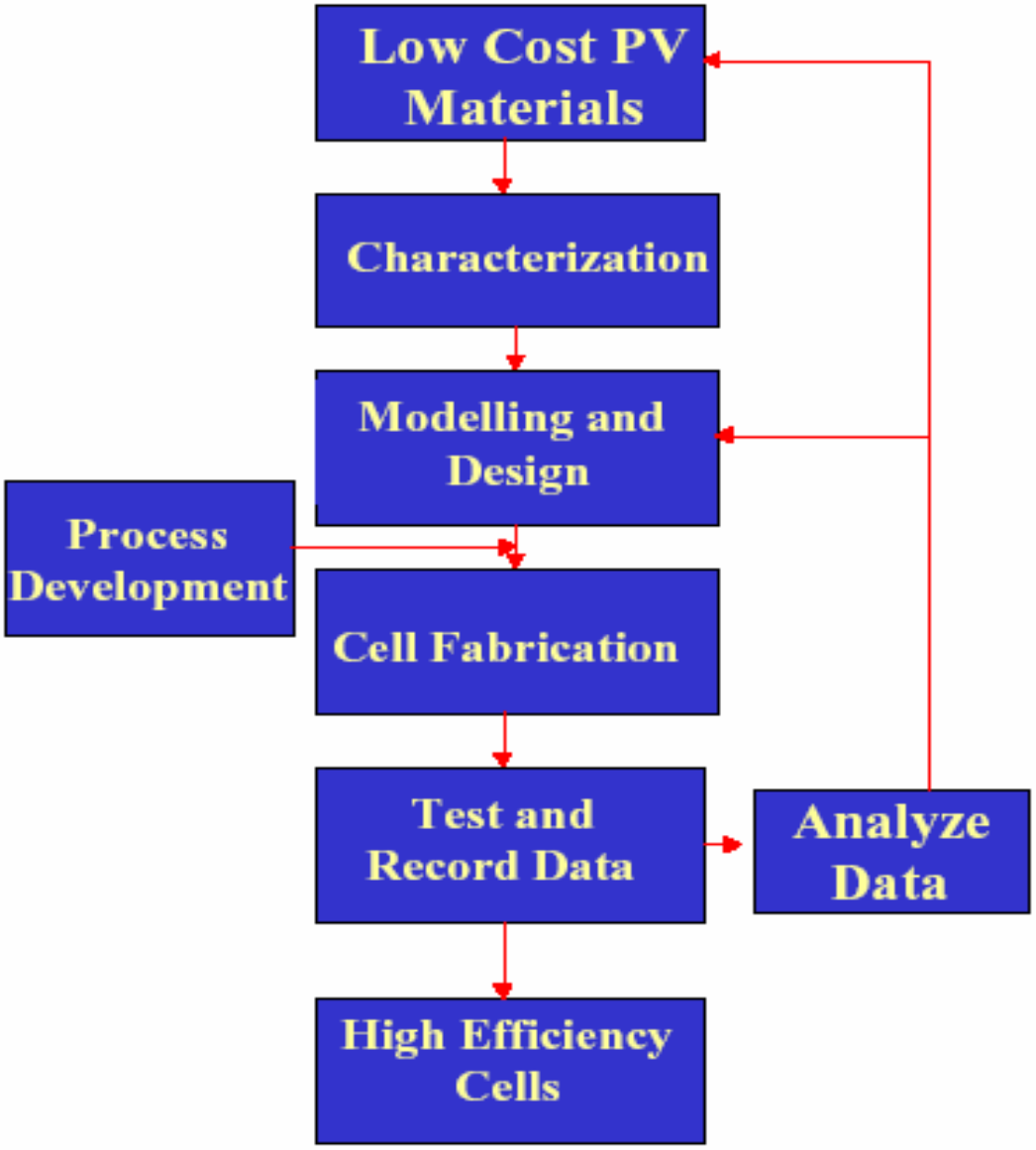
University Center of Excellence for Photovoltaic Research and Education
Georgia Tech

Mission of UCEP

- To improve the science and technology of advanced photovoltaic devices
- To reduce the cost of PV generated electricity
- To design and fabricate record high efficiency solar cells on low-cost materials
- To develop manufacturable low-cost high-performance technologies for next generation silicon solar cells
- To provide training and enrich the educational experience of students
- To maintain a leadership position and give the United States a competitive edge in PV through high quality research and education

Approach to Low-Cost High-Efficiency Cells



Solar Cell Fabrication Facilities At Georgia Tech

UCEP

- Class 100-1000 Clean Room and Cleaning Hoods
- Solid Source (P_2O_5) Phosphorus Diffusion Furnace
- Spin-on source Phosphorus Diffusion Furnace
- Boron Diffusion Furnace (BBr_3)
- Al Drive-in Furnaces
- Oxidation Furnaces
- Forming Gas Annealing Furnaces
- Belt Furnace with Tungsten-Halogen Lamps
- Custom-built RTP/Belt Furnace with UV and Tungsten-Halogen lamps
- Plasma Enhanced Chemical Vapor Deposition of SiN and SiOx
- Single Wafer Rapid Thermal Anneal Furnaces (RTA)

- Metal Evaporator (Ti, Pd, Ag)
- Metal Evaporator (Au, Al)
- Dielectric Evaporator for ZnS/MgF_2 AR coatings
- Silver Plating
- Photolithography Area and Accessories
- Spinners
- Baked Ovens
- Mask Aligners
- Chemical and Porous silicon Surface Texturing
- Wafer Thinning
- Lapping and Polishing
- Reactive Ion Etcher (IRE)
- Screen Printers (Ag, Al, P)
- Screen Printer with Optical Alignment

Materials and Device Characterization Facilities At Georgia Tech

Instrument	Function
Automated Dark & Light I-V	Solar cell parameters, cell efficiency, and cell diagnostics
Light and Dark Spectral Response and IQE	IQE, diffusion length and surface recombination velocity
Reflectivity Measurement	Reflectance as a function c wavelength
Photoconductance Lifetime Tester	Minority carrier lifetime as a function of injection level
DLTS	Detection of traps and determining parameters (E_T, N_T, σ) due to impurities and defects.
LBIC	Defect density, spectral response mapping in semiconductor materials and devices
EBIC	Electrical activity of defects
FTIR	Detection of impurities such as O, B, Al and H in Si and GaAs.
SIMS	Doping and impurity profiles
Electrical Doping Profiler	Doping concentration profile

Instrument	Function
Hall Measurements	Carrier mobility, bulk dopant concentration, conductivity type and dopant energy levels
Photoluminescence	Characterization of shallow levels, bandgap, and stress
TEM, SEM, X-ray Topography	Defect and microstructural analysis
Auger and ESCA	For chemical analysis
C-V, C-t	For interface state density, insulator charges and generation lifetime in MOS capacitors
Curve Tracer	For analyzing the IV characteristics of Silicon devices
Four Point Probe	For measuring conductivity type, resistivity, and sheet residence
I-V-T Tester	For determining carrier transport mechanism defect centers responsible for leakage current.
Positron Annihilation (PAS)	Defects in Semiconductors

PV Design, Analysis and Simulation Capabilities at Georgia Tech

UCEP

13 Device models

Models	Analysis
Dessis	2-D device modeling
PC1D	1-D solar cell design and performance prediction
Sunrays and PV optics	Optical ray tracing
Arcoat	Anti-reflectance coating design program
S-model	Impact of diffusion profile and surface passivation on saturation current density
Hydrodynamic	Multidimensional solutions to the semiconductor equations
Lifetime	Carrier lifetime in silicon as a function of material and defect parameters

Models	Analysis
Grid	Design and optimization of solar cell contact
Grid Design	Design and optimization of solar cell contacts
SRV	Computers effective surface recombination velocity
IQE	Internal quantum efficiency, diffusion length and surface recombination velocity
J_o	Reverse saturation current density from PCD measurements
PCD	Computes carrier lifetime parameters from PCD measurements

6 PV systems models

Models	Analysis
Sizing	Design and modeling of PV system
PV Form	Design and performance of PV systems
PC Cad	Design and performance of PV systems
Size PV	Design of PV systems
PV Design Pro	Design and performance of PV systems
GT PV Sim	Design and performance of PV systems

3 PV manufacturing cost models

Models	Analysis
E-Cost	Cost of electricity/system
M-Cost 1	Manufacturing cost of module (Excel)
M-Cost 2	Manufacturing cost of module (MatLab)

Capabilities for commercial-size (≥149 cm^2) solar cells

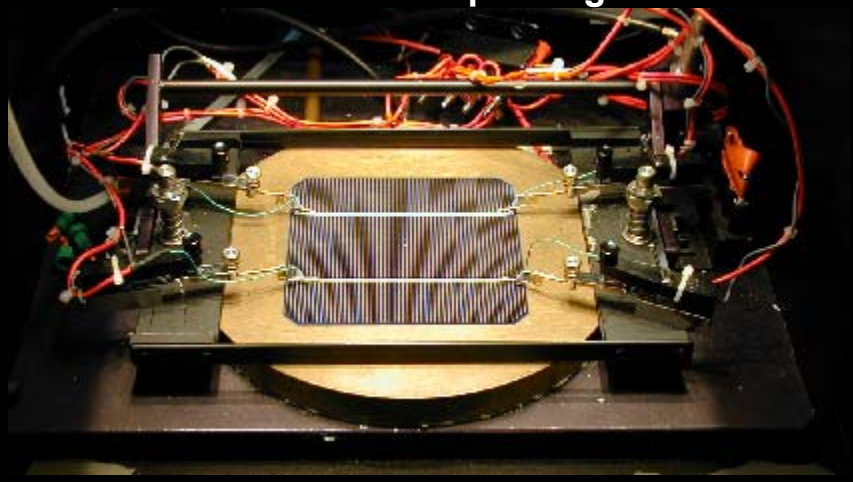
tube furnace diffusion

PECVD SiN_x deposition

front & back contact screen printing

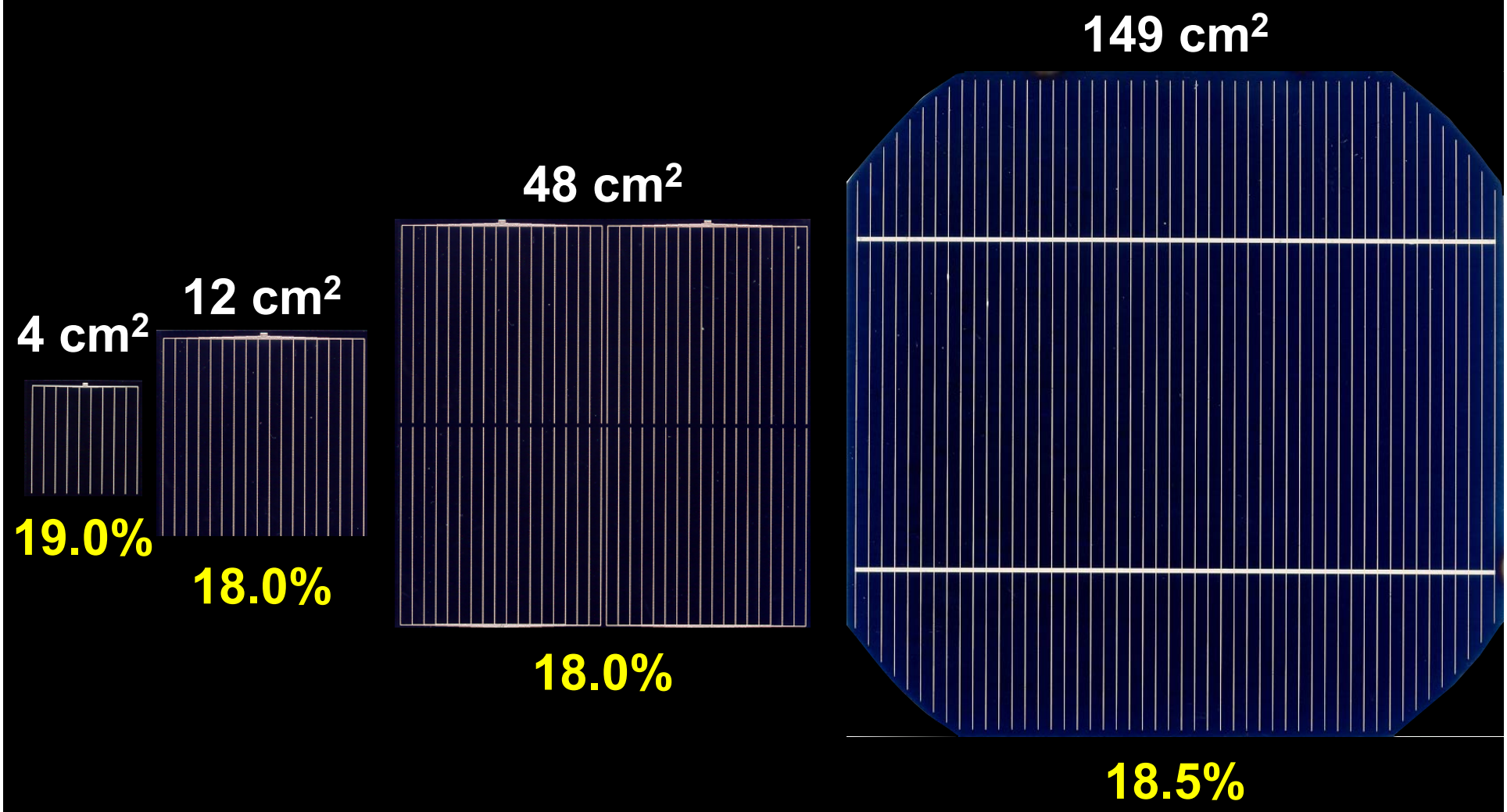
paste drying

front & back contact firing

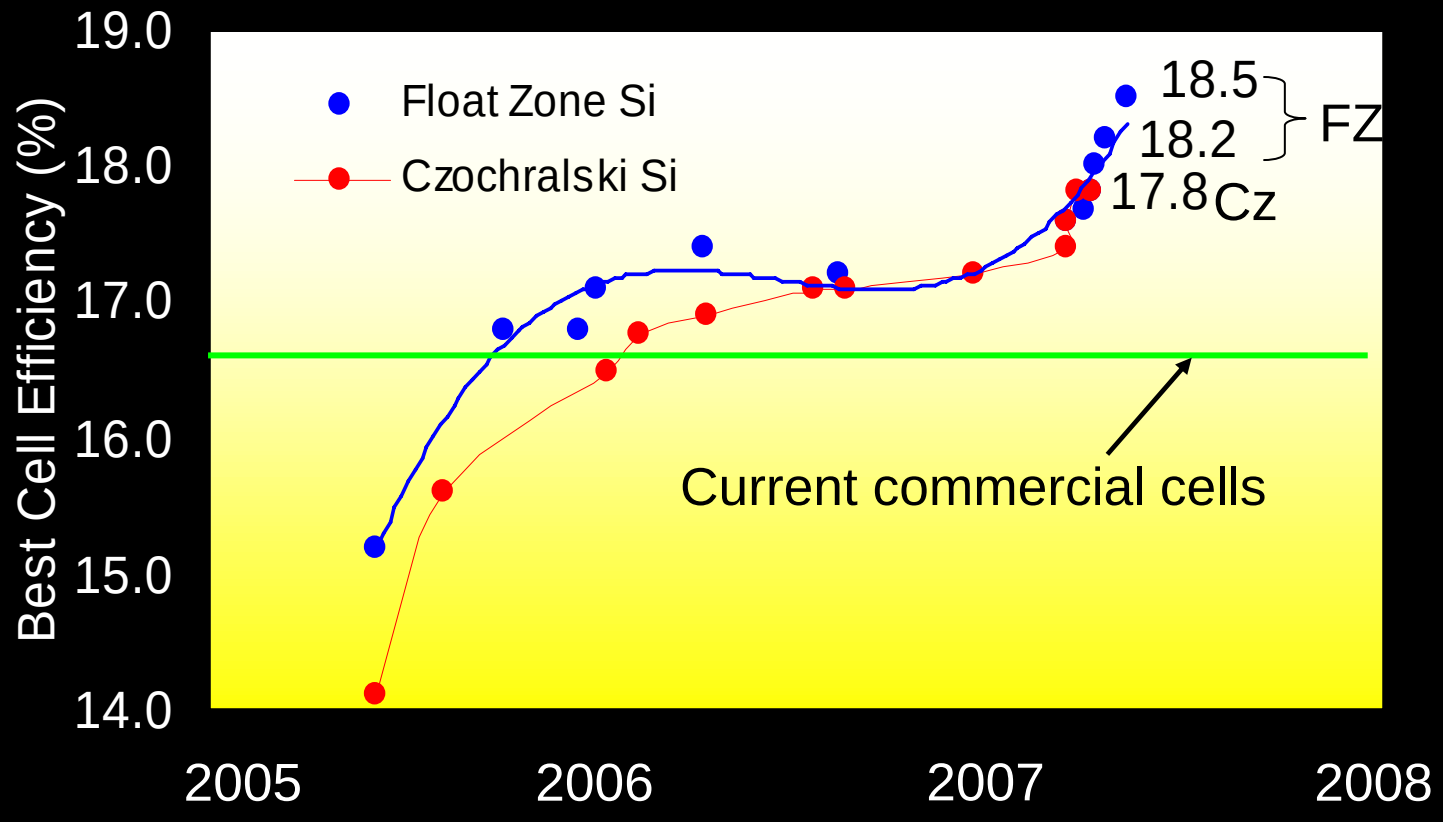


Cell testing

Evolution of Cell Area with New Processing Equipment at Georgia Tech



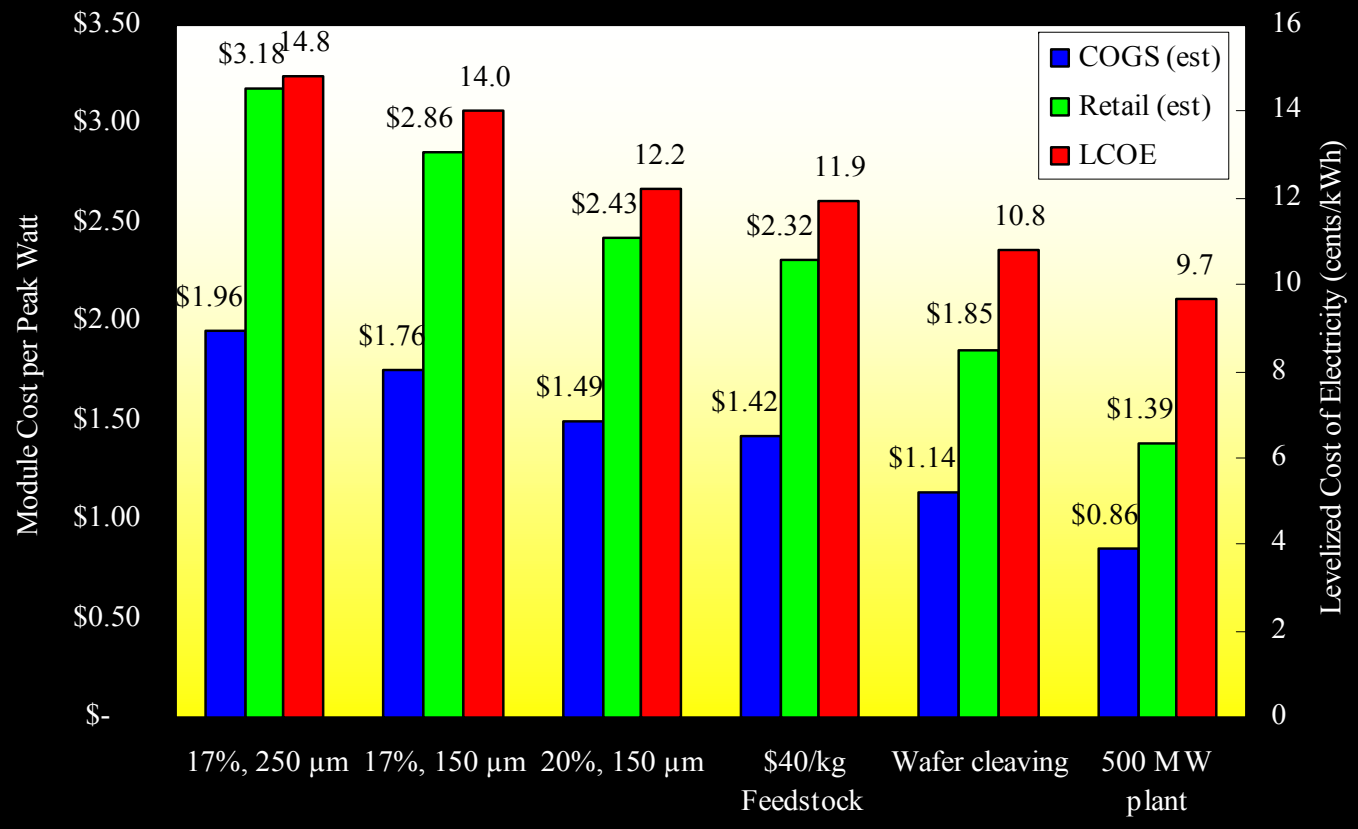
Progress of commercial-scale cells at Georgia Tech



Developed a contact firing scheme to:

- increase the emitter sheet resistance from 40 to 80 Ω/sq.
- form high-quality contacts
- achieve cell efficiencies of 17.8% on B-doped Cz and 18.5% on FZ Si.

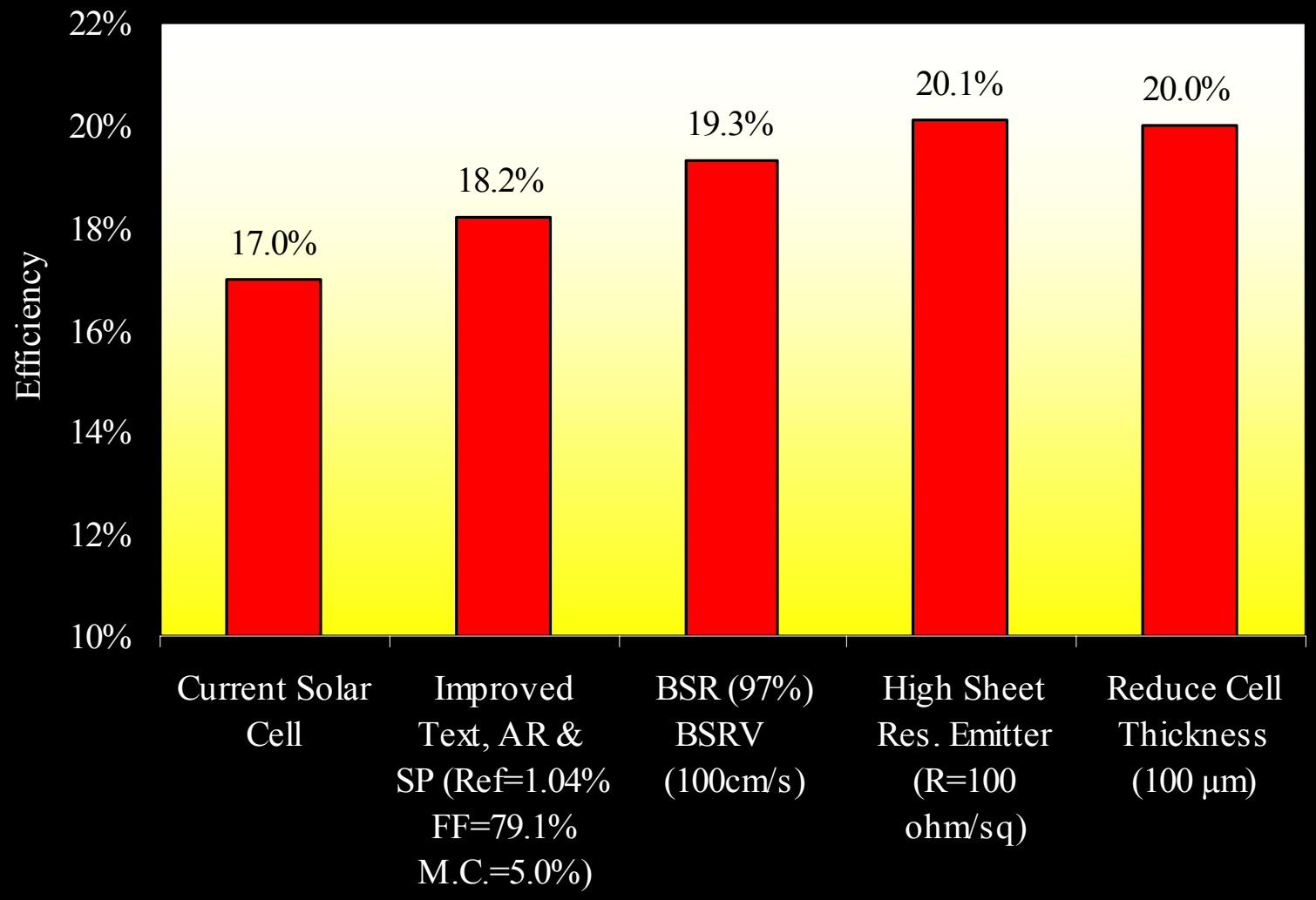
Roadmap to cost-effective PV using high-efficiency thin c-Si solar cells



2015 DOE estimates for BOS costs

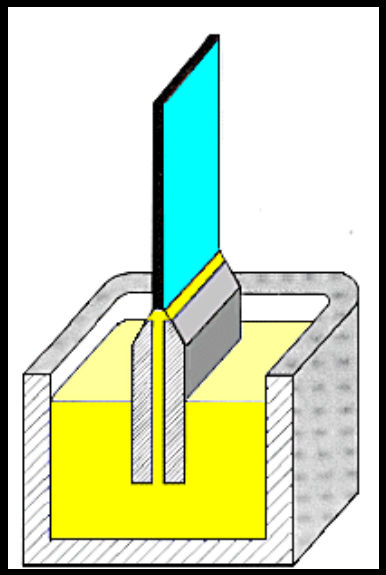
BOS Component	Price ($/W)
Inverter	0.30
Direct BOS	0.33
Installation	0.42
Indirect Costs	1.00
Total	**2.05**

Roadmap to 20%-efficient thin c-Si solar cells

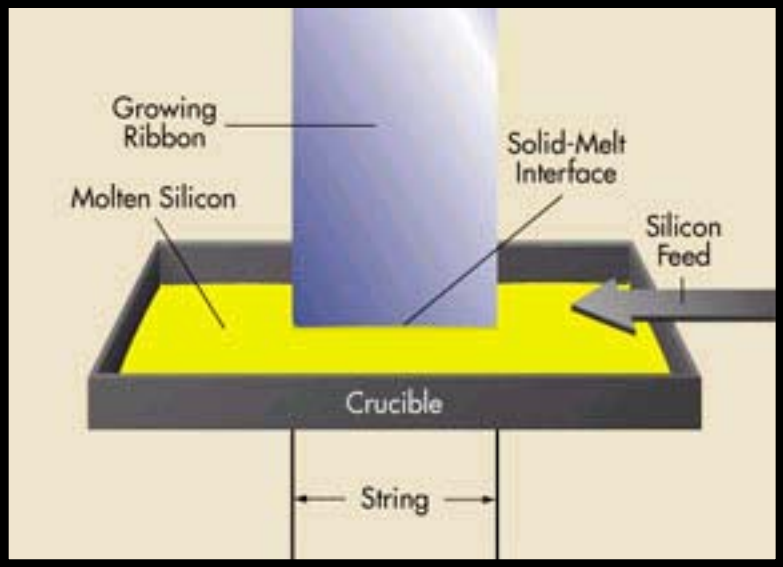


Ribbon Silicon Materials for Commercial PV Applications

EFG Si (SCHOTT Solar)



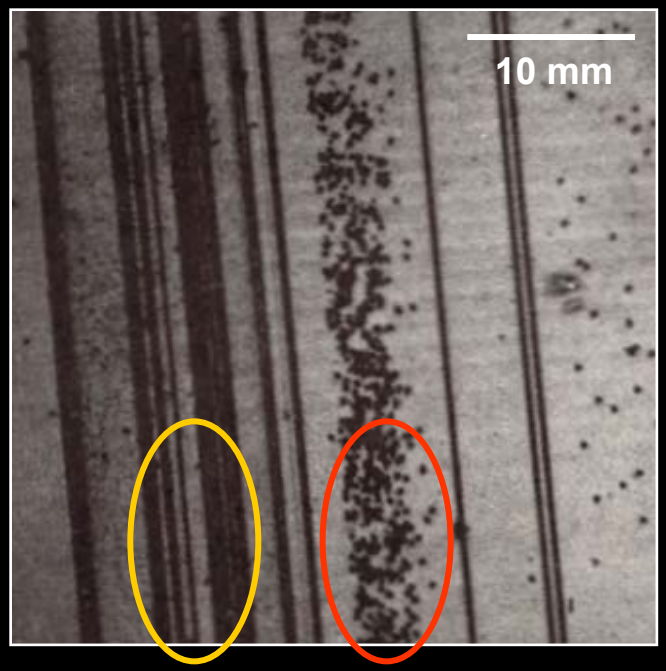
String Ribbon Si (Evergreen Solar)



- Continuous crystal growth
- No silicon losses associated with wafer slicing

PV-Grade Crystalline Ribbon Si Materials

Defects in EFG Si*



Twin boundaries Dislocations

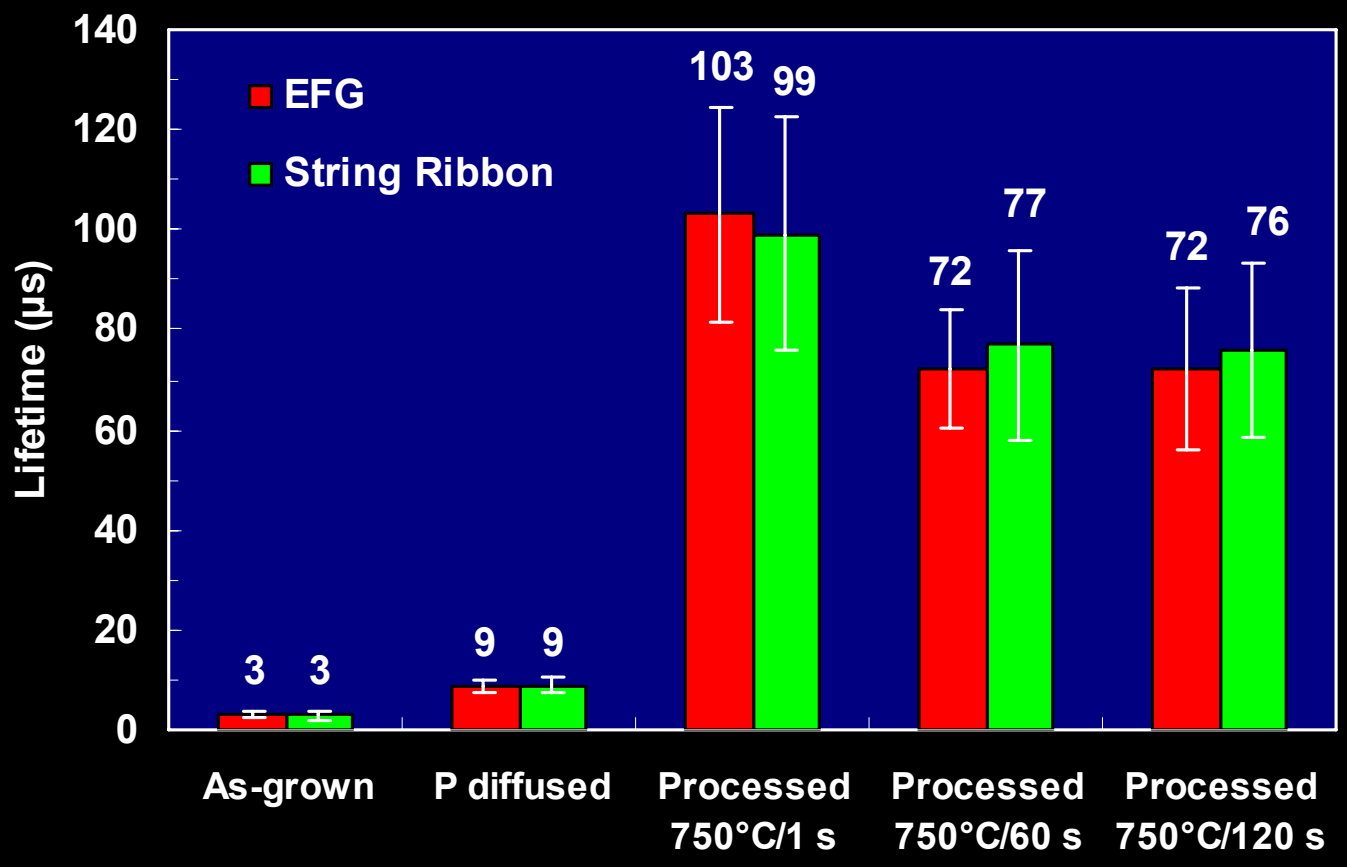
Recombination sites

Characteristics**

Material	Carbon (cm^{-3})	Oxygen (cm^{-3})	Metal Conc.	Dislocations (cm^{-2})
Cz	$0.5\sim2.5\times10^{17}$	$0.1\sim2.0\times10^{18}$	Low	500
Cast	$< 5.0\times10^{17}$	$< 2.5\times10^{17}$	Med	1.0×10^{5}
EFG	10^{18}	$2.4\sim4.0\times10^{17}$	High	$< 1.0\times10^{6}$
String Ribbon	4.0×10^{17}	$< 5.0\times10^{16}$	High	5.0×10^{5}

* K.V. Ravi, *Imperfections and Impurities in Semiconductor Silicon*, 1981
**R.O. Bell and J.P. Kalejs, J. Mater. Res., 1998

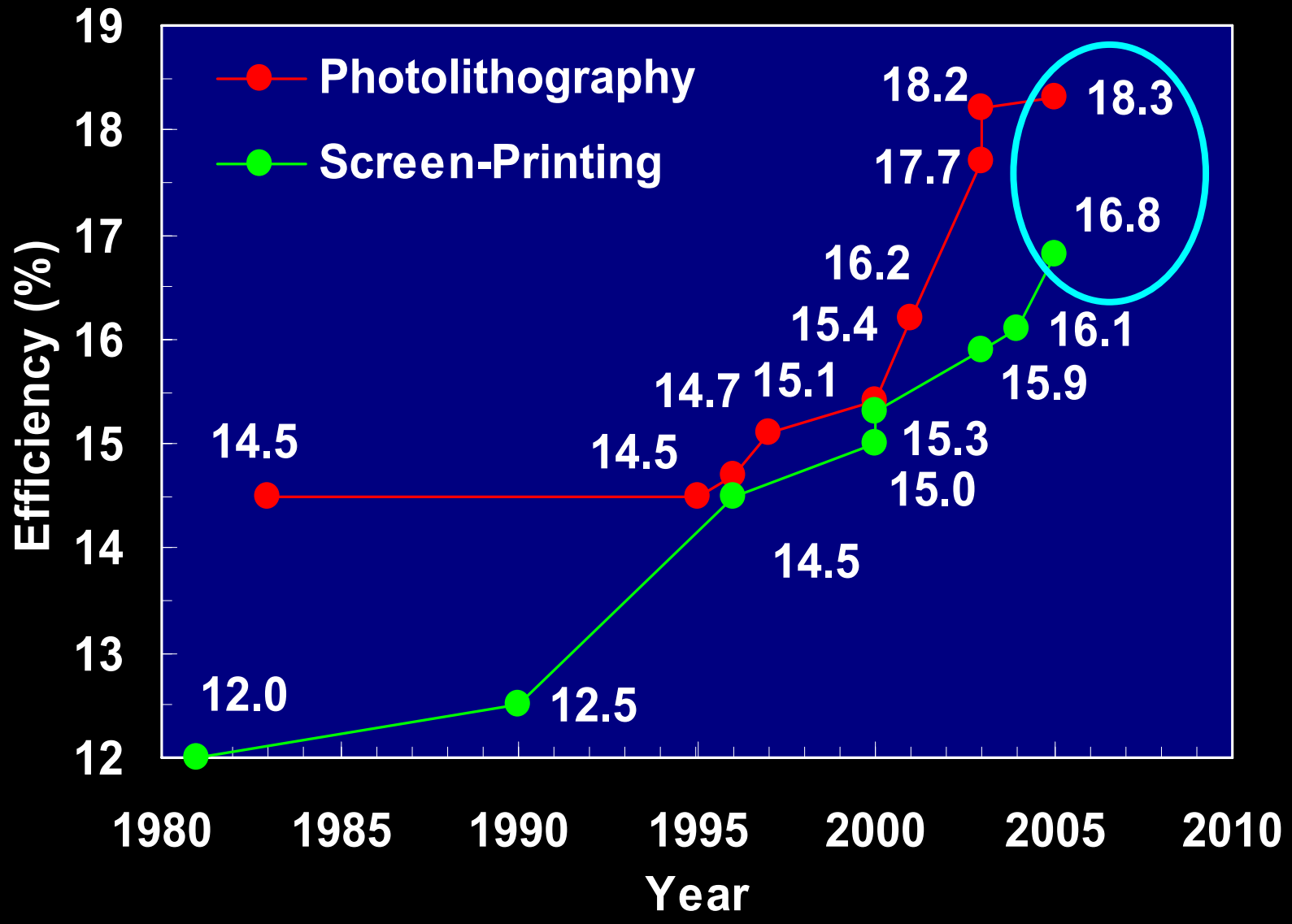
Carrier Lifetime Measurements Before/After Cell Processing



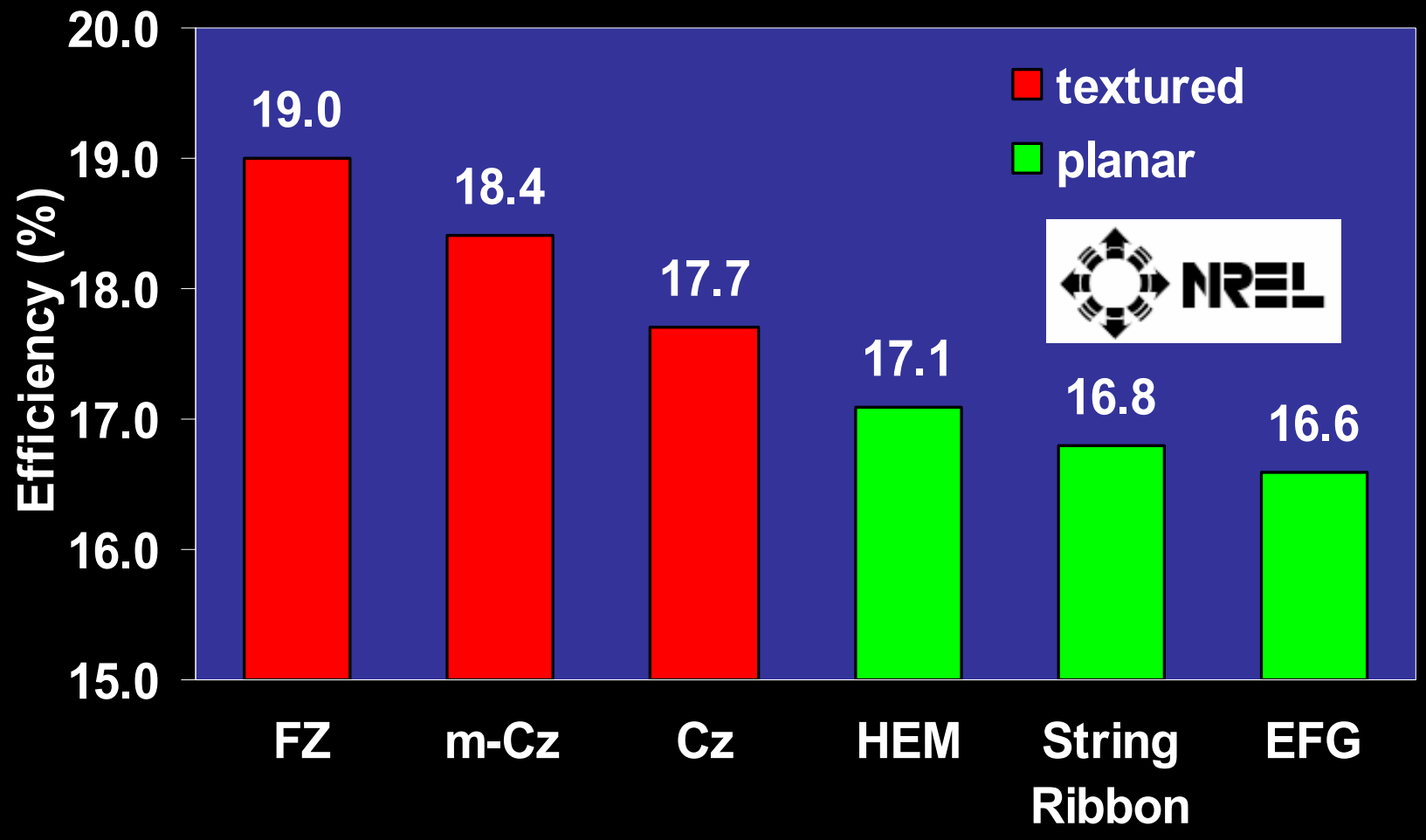
Cell processing

- P diffusion
- PECVD SiN
- Al back contact
- RTP firing

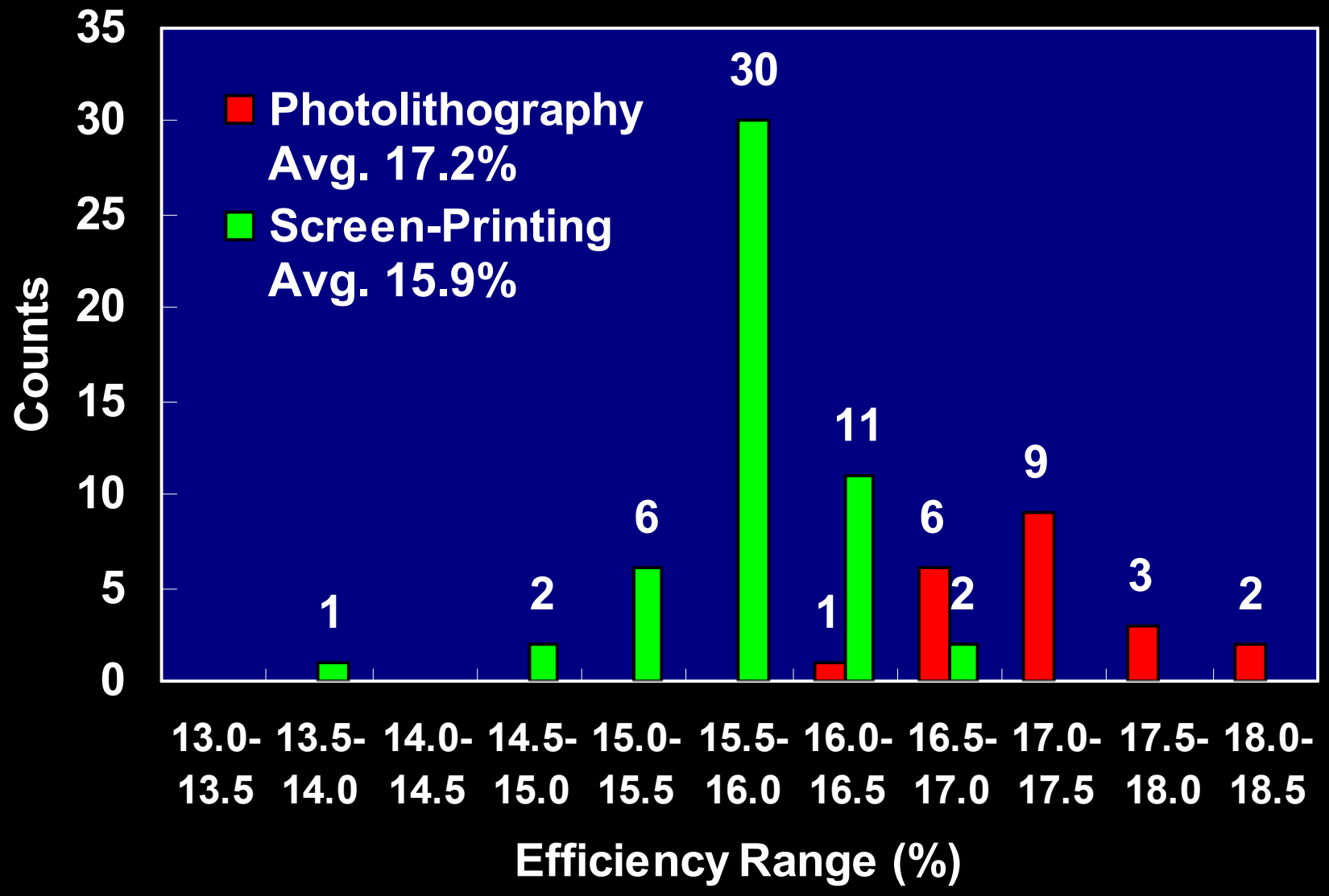
Competition and Progress of Ribbon Si Solar Cell Performance



Record High Efficiency 4 cm^2 Screen-printed cells with Co-fired Contacts and SiN ARC

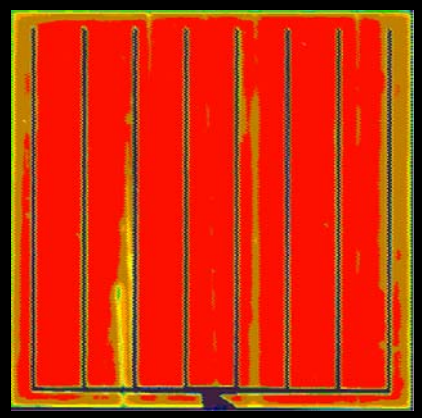


Efficiency Histogram of String Ribbon Si Cells Fabricated in This Study

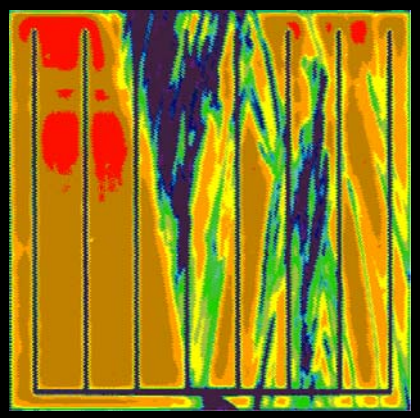


LBIC Analysis of High-, Mid-, and Low-Efficiency String Ribbon Si Solar Cells

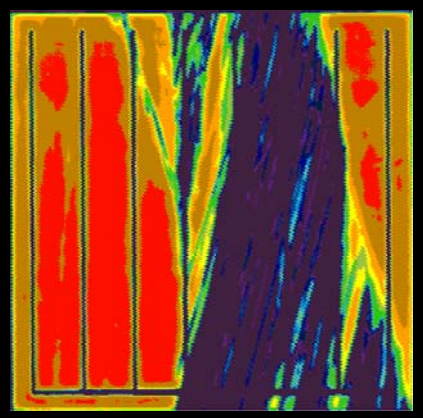
LBIC scans



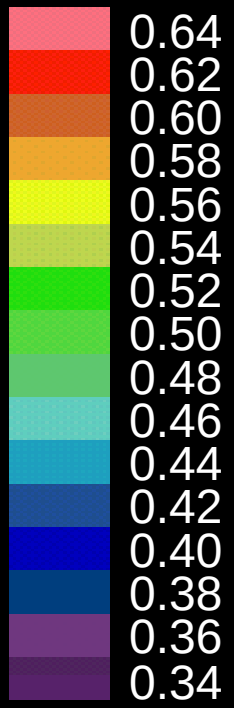
Cell 4
Eff. = 15.9%
Voc = 616 mV
LBIC = 0.568 A/W



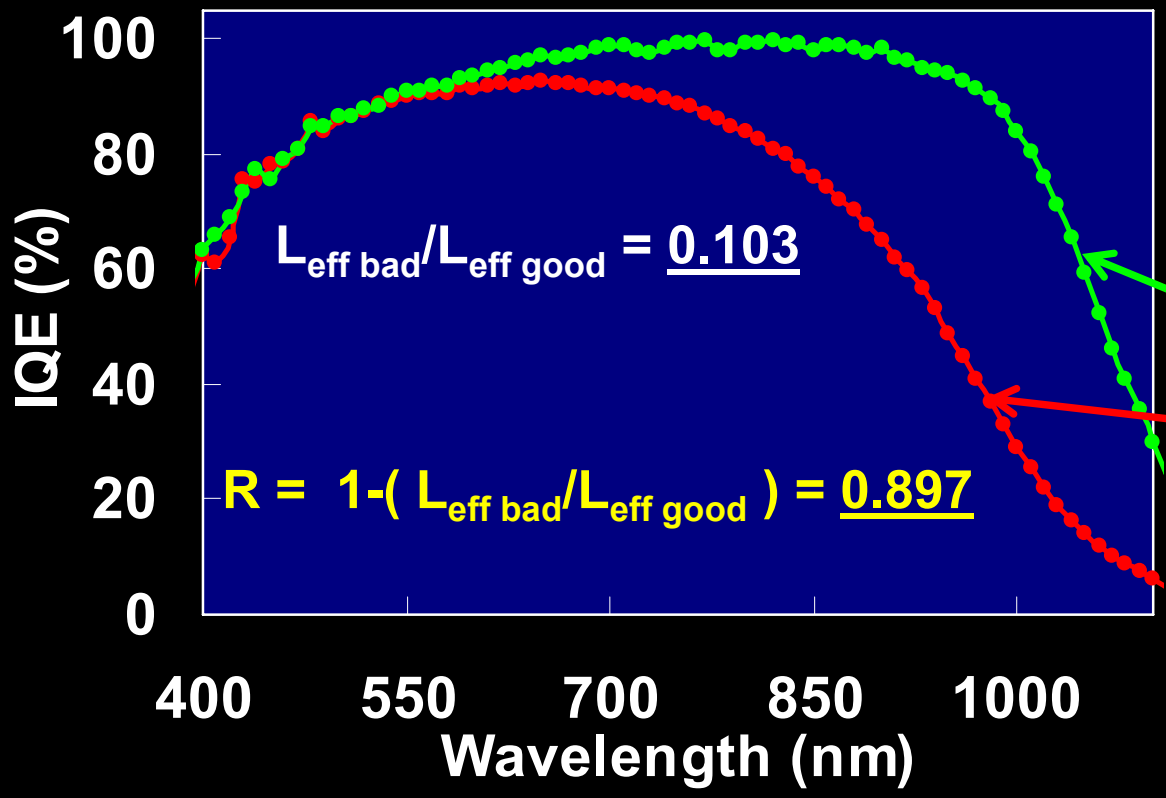
Cell 6
Eff. = 15.0%
Voc = 592 mV
LBIC = 0.504 A/W



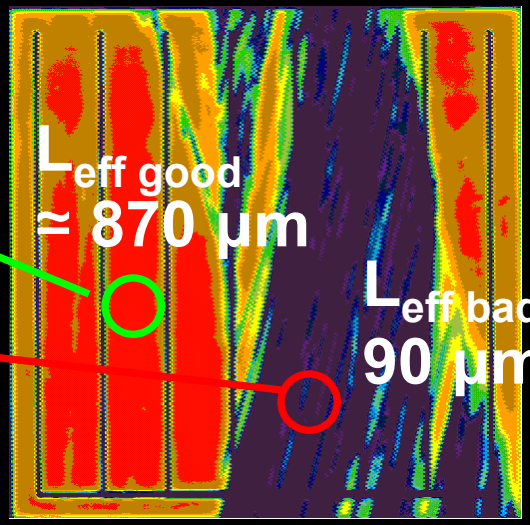
Cell 9
Eff. = 14.1%
Voc = 578 mV
LBIC = 0.454 A/W



IQE Analysis on Low-Efficiency String Ribbon Si Cell



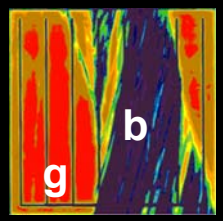
LBIC Scan (980 nm)



$$V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{SC}}{J_0} + 1 \right)$$

$$J_{ob} = \frac{q n_i^2 D_n}{N_B L_{eff}}$$

LBIC Scans

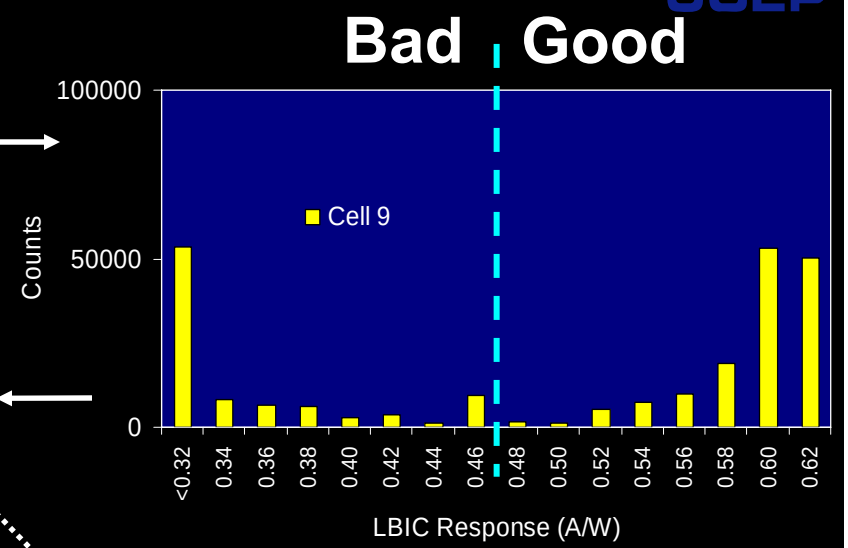


Local IQE (g&b)

Image Magick

PC1D
L_{eff} (g&b)

Area Fraction
(g&b)



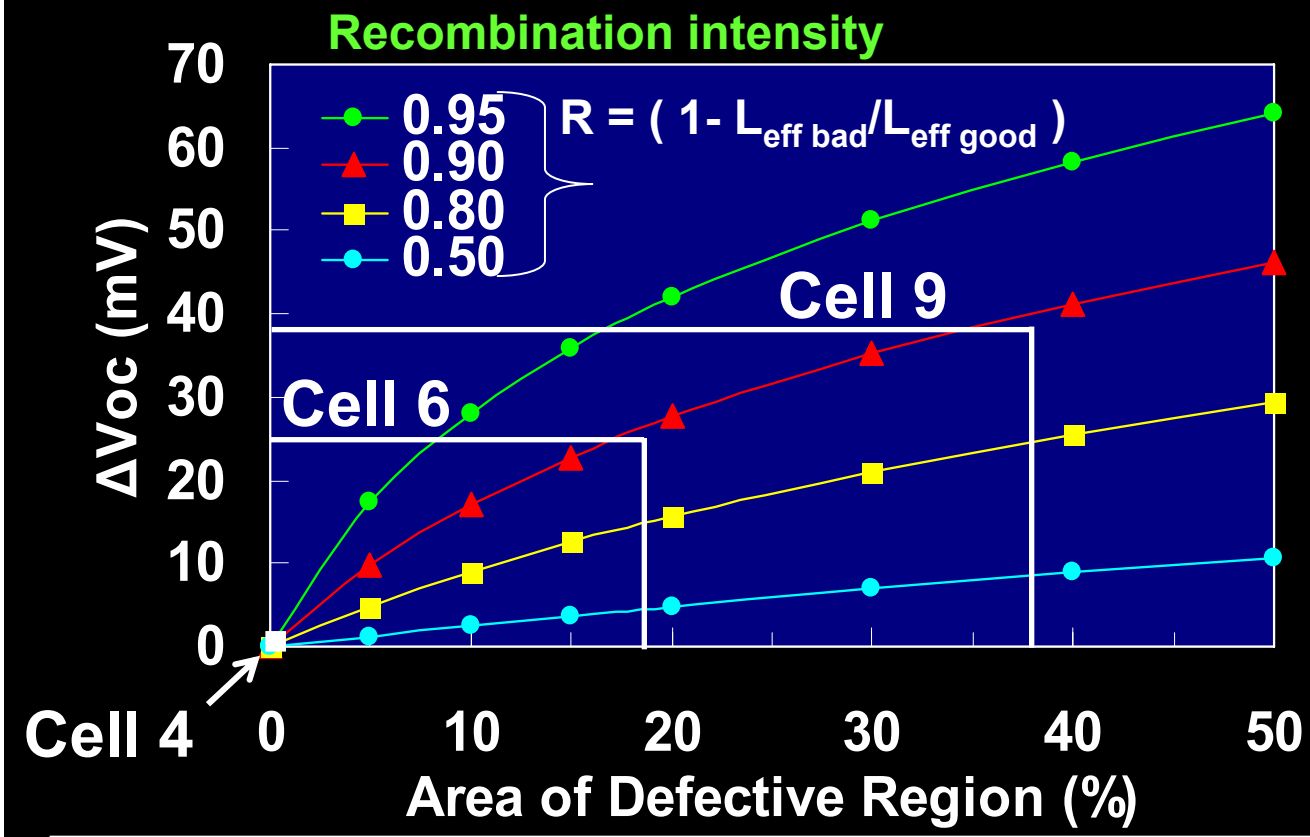
$$L_{eu}^{-1} = \sum_{i=1}^{n} (L_{eff,i}^{-1} \times A_i)$$

$$A_j = \frac{\sum_{i=1}^{N} B_i}{\sum_{i=1}^{T} B_i}$$

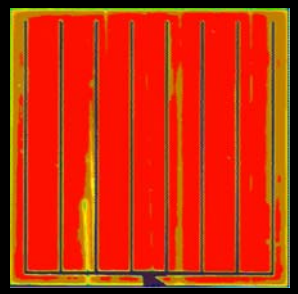
$$\Delta V_{OC} = \frac{nkT}{q} \ln\left(\frac{J_{SC,good}}{J_{SC,eu}} \cdot \frac{L_{eff,good}}{L_{eu}} \right)$$

Comparison with measured ΔV_{OC}

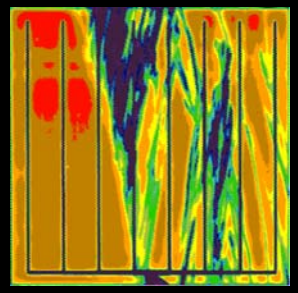
Loss in V_{OC} due to Material Inhomogeneity in String Ribbon Si Cells



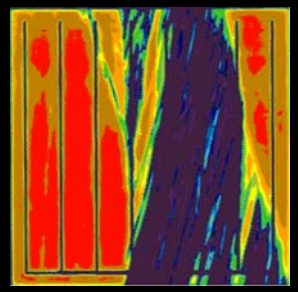
ID	Voc (mV)	Measured ΔVoc (mV)	Modeled ΔVoc (mV)
Cell 4	616	NA	NA
Cell 6	592	24	25
Cell 9	578	38	39



Cell 4



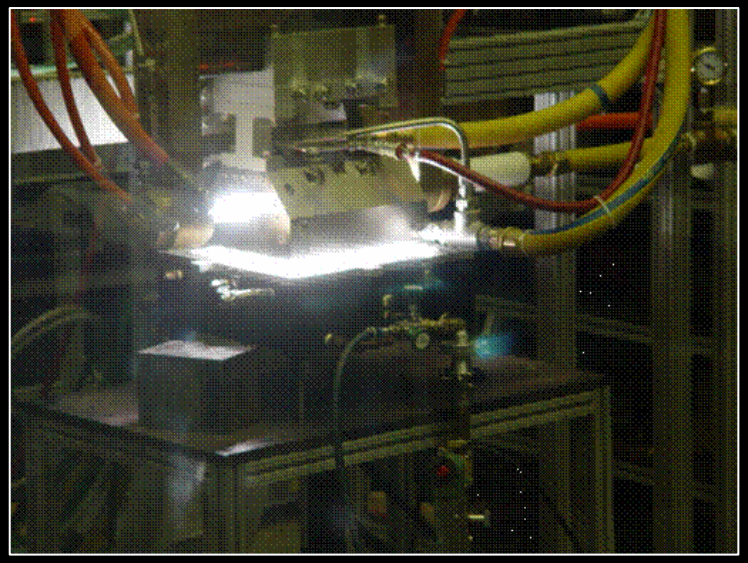
Cell 6

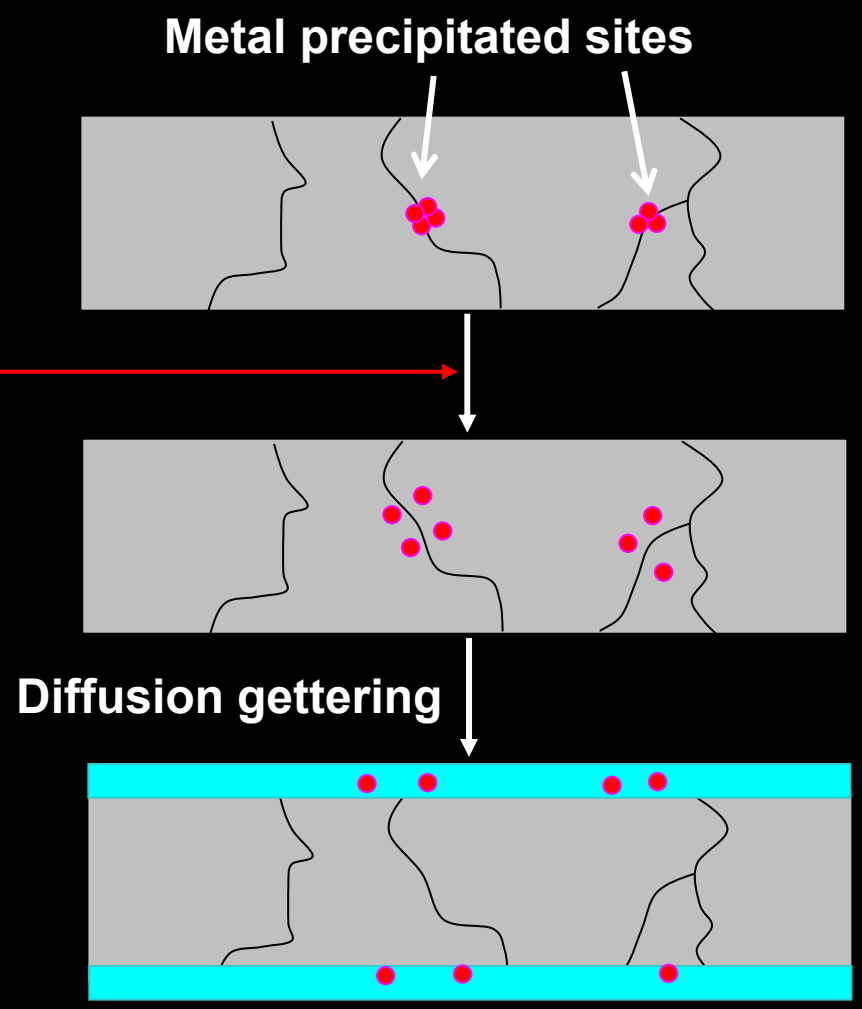


Cell 9

New technologies to mitigate the recombination intensity of defective regions

Pulse Heat Treatment

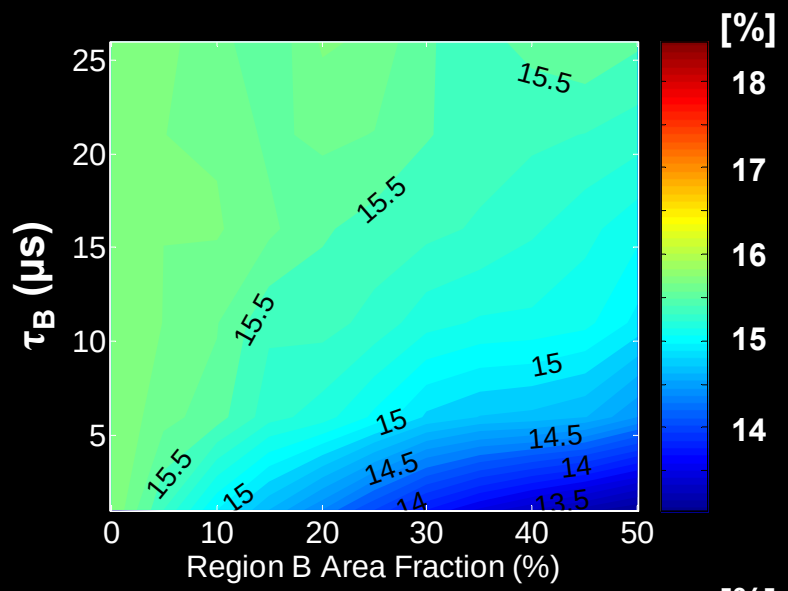


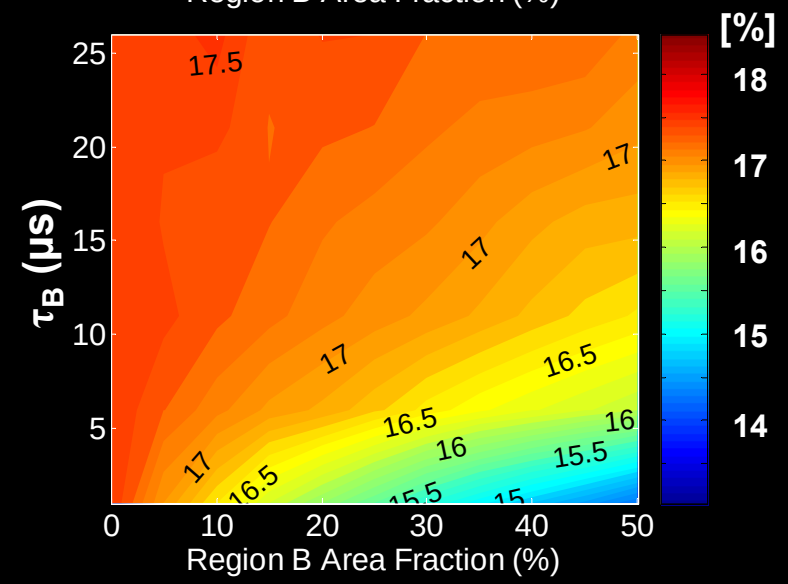


In collaboration with

OAK RIDGE NATIONAL LABORATORY
U. S. DEPARTMENT OF ENERGY

Roadmap to >17%-Efficient Ribbon Si Cells





Current Status

Resistivity: 3.0 Ωcm
Surface: Planar
Emitter: 45 Ω/sq.
Thickness: 300 µm
BSRV: 250 cm/s
BSR: 55%

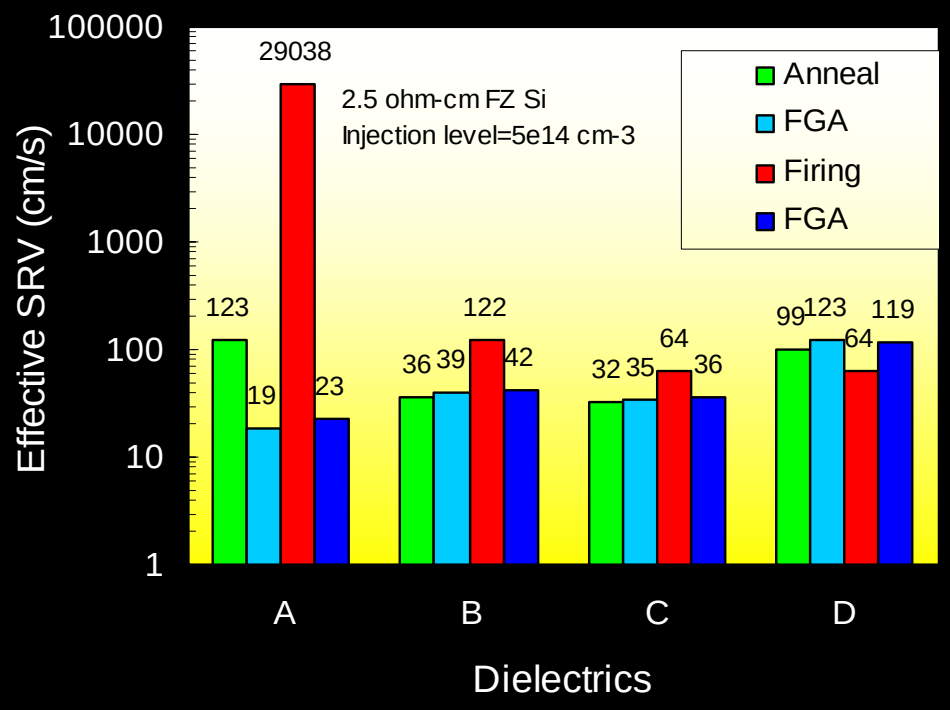
Future Design

Resistivity: 1.3 Ωcm
Surface: Planar
Emitter: 100 Ω/sq.
Thickness: 100 µm
BSRV: 100 cm/s
BSR: 90%

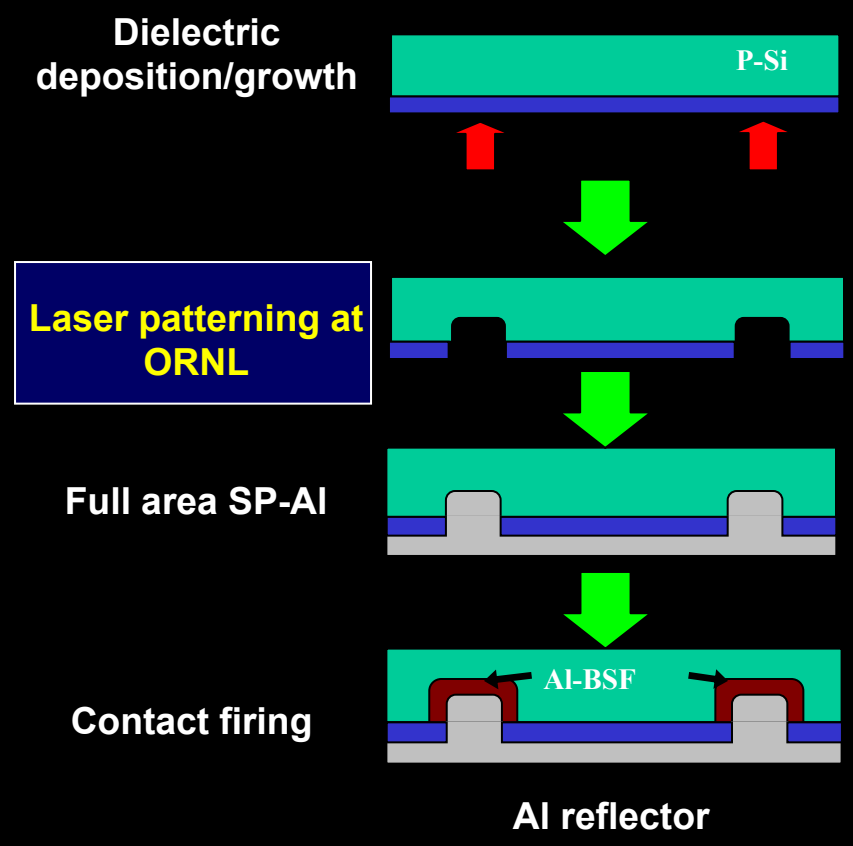
FF: 0.770-0.775
Ag grid: 6.0%
τ_{avg}=100 µs

High-quality surface passivation and local back contacts using low-cost processing

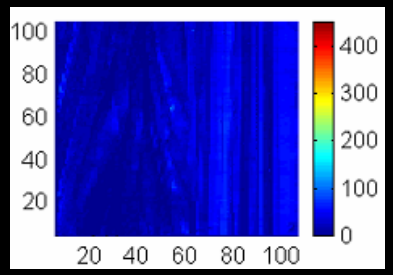
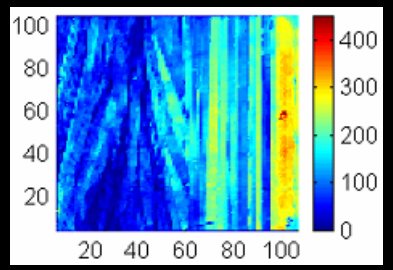
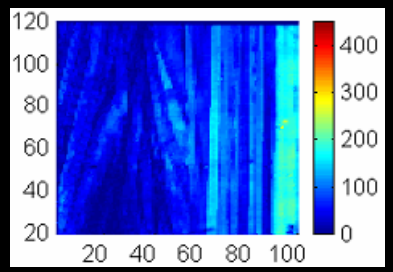
Surface recombination velocity for different spin-on dielectrics



Back contact formation using laser patterning



Photoluminescence Scans on EFG Si Before/After RTP Anneal

Process Sequence	PL mapping	I_{bb} (avg.)
P, SiN_x, and Al SP		25
RTP 750°C/1 s		123
RTP 750°C/120 s		65

25 cm^2 EFG Si, 3.0 Ωcm, 300 μm thick