Hardware Optimization of a DSSS Receiver Using Simulink® Model

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ABSTRACT

A Simulink® model for Direct Sequence Spread Spectrum (DSSS) receiver is presented. Using data-path size as an additional parameter in the model blocks made it possible to do the hardware optimization of the receiver on the block-by-block basis. The effect of the round-off errors to the bit-error rate (BER) of the receiver is quantified for each block in the model. Different functional parts of the receiver, such as analog-to-digital converter (ADC), digital down-converter (DDC), matched filter, are shown to have different sensitivity to the data-path size. Using multivariable optimization, one can use the model to minimize the hardware implementation with respect to the BER.

Keywords

Digital down-converter, matched filter, analog-to-digital converter round-off error.

1. INTRODUCTION

Substantial amount of work has been published in literature regarding the round-off error and its influence to different signal processing algorithms [1], [2], [3]. In many cases, it was possible to do analytical description of the effects of the round-off errors to a particular algorithm. One such case is the effect of the round-off error of the filer taps to the sideband attenuation of a digital filter [4]. However, it would be very difficult to describe analytically how the round-off error of a low-pass filter used in a DSSS receiver affects the receiver BER. Using a model for the receiver, one can easily determine sensitivity of the receiver BER to different datapath sizes in the receiver. Thus, a minimum hardware implementation can be determined for a given performance degradation. In this work, a DSSS receiver is optimized with respect to the datapath size of various functional parts of the receiver. Varying datapath size, the bit error rate (BER) for the entire receiver was recorded using Simulink® models.

2. DSSS RECEIVER ARCHITECTURE

The receiver architecture shown in Figure 1 represents a simplified DSSS architecture where a synchronous reception is assumed. The main parts of the receiver are intermediate frequency (IF) ADC, DDC, image rejection low-pass filter (LPF), and the matched filter in the form of the spread spectrum correlator. The input to the receiver is a binary phase shift keying (BPSK) IF signal sampled by the ADC and then processed by the DDC to generate the baseband signal. The low-pass filter is used to remove the image generated during the DDC. The output of the LPF is downsampled, and sent to the correlator where the spreading code is removed from the data waveform. The pulse shaping used in this simulation is the IJF shaping proposed by Feher [5].

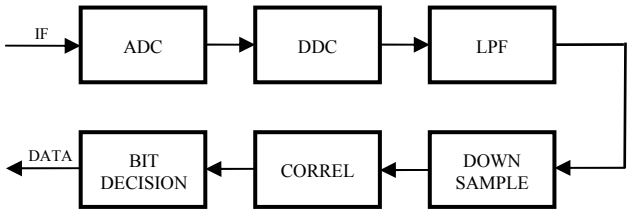

Figure 1. DSSS receiver block diagram

3. SIMULATION MODEL

Main challenge in obtaining BER via simulation is that a large number of iterations needed to achieve a sufficient error statistics. In this work, several measures and assumptions were made to reduce the simulation time. The spreading was done using a 63-length MLS code with chip rate set to 1 MHz, while IF frequency was 10 MHz. The 24 MHz sampling frequency is conservitably higher than the Nyquist rate for the 10 MHz IF signal. The frequency and the phase of the numerically controlled oscillator (NCO) in the DDC was set to match the received IF carrier exactly. The low-pass filter used for image rejection was designed as an equiripple finite impulse response (FIR) filter with minimum order for a given sideband attenuation and the width of the transition band. To further reduce

computation complexity, downsampling was applied to the filtered baseband signal prior to the correlator. Also, instead of the sliding correlator, a single-point correlator was implemented. The phase of the spreading code in the receiver was adjusted so that the single correlation point corresponded to the correlation peak. The bit detection was done by checking the sign bit of the correlator output. The following datapath parameters were used in the simulation:

- ADC resolution
- DDC datapath size
- LPF order
- LPF tap resolution
- LPF arithmetic resolution
- Correlator time resolution in samples per chip
- Correlator datapath size

In order to quantify the influence of one parameter, all other parameters are set close to an ideal value. The baseline in the simulation was established by setting all the datapath sizes to 10, the filter order to 41, and the correlator samples per bit to 24. An AWGN channel was used in the simulation with -10dB signal-to-noise ratio (SNR). With 18dB of processing gain, the SNR at the receiver input was 8dB so that the corresponding BER was 0.5*10e-3 [6]. Each of the datapath sizes was varied in the range from 3 to 10. The number of samples per chip had the values of 2, 3, 4, 6, 8, 12, and the order of the filter was 11, 21, 31, and 41. The number of bits in each simulation was 10e5.

To further increase the simulation speed, Simulink® frames were used instead of the sample-based simulation. The frames were sized to correspond to a bit worth of samples, i.e. 24x63 in this particular case. Increase of the simulation speed was due to Simulink®'s matrix-oriented signal processing. Also, all the custom-built simulation blocks in the model were made using C-MEX S-Functions that execute much faster than the M-file S-Functions. Figure 2 shows the model used in the simulation.

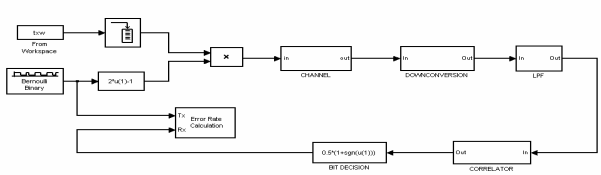

Figure 2. Simulation model

After implementation of all above mentioned techniques, the model was able to run in less than 10 minutes for 100,000 bits.

4. SIMULATION RESULTS

Results of the simulation are presented in a set of figures below, where a figure shows dependence of BER on a single parameter while the other parameters are kept constant. Figure 3 shows BER versus both the ADC resolution and the DDC datapath size. The other datapath sizes are 10, 8, and 6 respectively. The correlator time resolution is 2 samples per chip, and the low-pass filter order is 41. As the figure shows, the performance of the receiver starts to degrade significantly for ADC/DDC resolution below 5 when all other datapath sizes are 10, and below 7 when the other datapath sizes decrease.

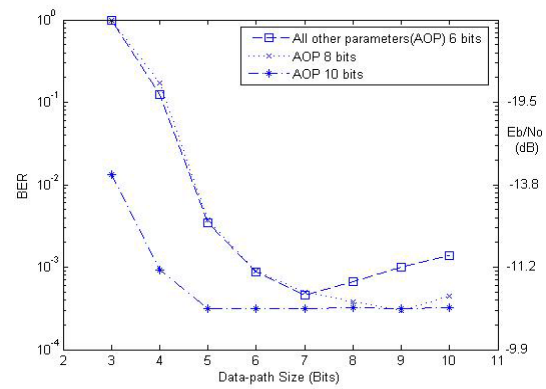

Figure 3. BER versus ADC/DDC resolution

In Figure 4, BER versus low-pass filter datapath size shows that the receiver performance is relatively insensitive to the round-off error in the filter. The sensitivity to the filter order is more pronounced as shown in Figure 5.

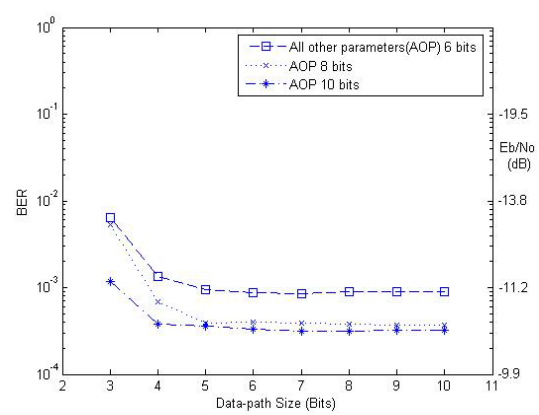

Figure 4. BER versus LPF datapath size

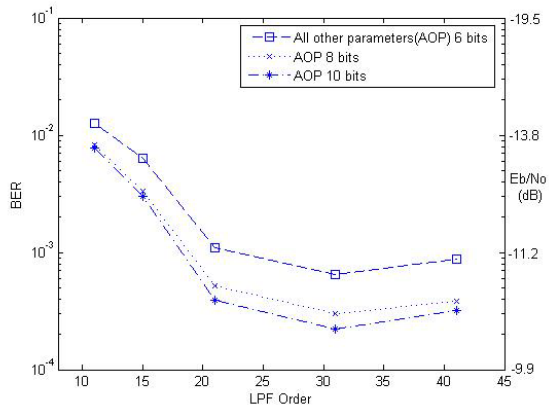

Figure 5. BER versus LPF order

Figure 6 shows that the BER is almost insensitive to the resolution of the filter taps.

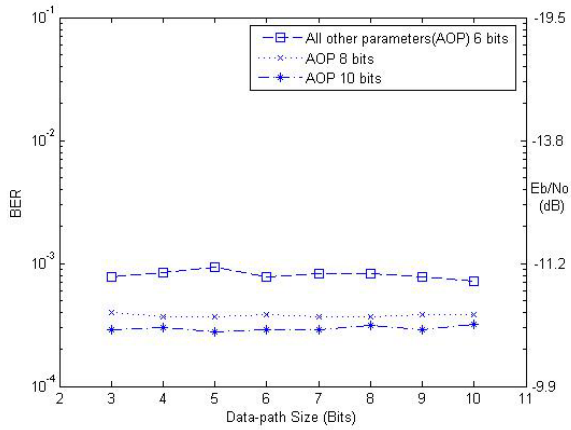

Figure 6. BER versus LPF tap resolution

To simulate how the size of the correlator affects the BER, two parameters were used. These were the correlator length defined as spreading code length times the number of samples per chip, and the correlator height defined as the datapath size. As Figure 7 shows, the BER is quite insensitive to the correlator length, while sensitive to the correlator height as shown in Figure 8.

Using the simulation results presented in Figure 3 through Figure 8, one can determine a set of minimum values for the parameters so that the DSSS receiver implementation size is minimized for a given implementation loss. Figure 9 shows one of the possible solution where the correlator length needs to be more than 4 to achieve a less than 1dB implementation loss. The other datapath sizes in that case are 10, the number of samples per chip is 2, and the LPF order is 41. Another possible solution for the same implementation loss was found by trying different sets of parameters. That solution includes a 6-bit ADC, a 6-bit

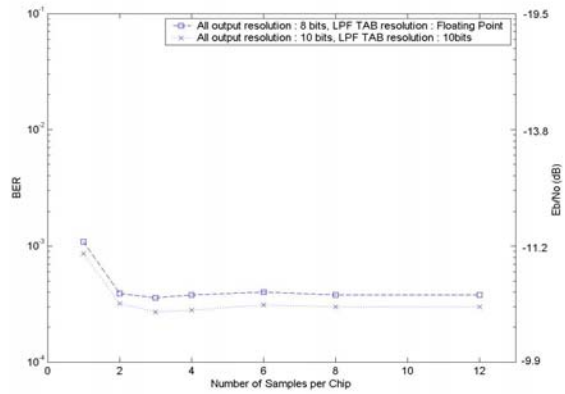

Figure 7. BER versus the correlator length

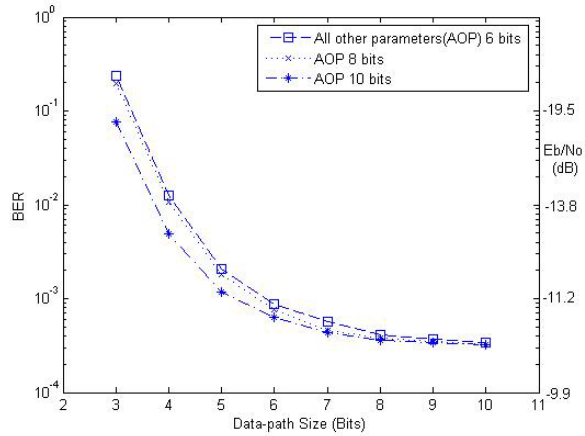

Figure 8. BER versus correlator height

DDC, a 21-order low-pass filter with 3-bit tap resolution and 5-bit arithmetic, a 2-bit per chip correlator with 6-bit arithmetic. However, to find an absolute minimum one needs to assign weights to each parameter corresponding to their contribution to the implementation area, and then implement a multivariable constrained optimization. Similarly, one can optimize the receiver with respect to the power by weighting the above parameters according to their individual contribution to the total receiver power.

5. CONCLUSIONS

In this paper, a Simulink® model was designed to determine BER sensitivity to the datapath size in various parts of the DSSS receiver. The model was optimized for the speed by using frames as well as the C-Mex S-Finctions for custom Simulink® blocks. The model was then used to

determine the minimum-hardware architecture for a given performance degradation. The minimum datapath sizes

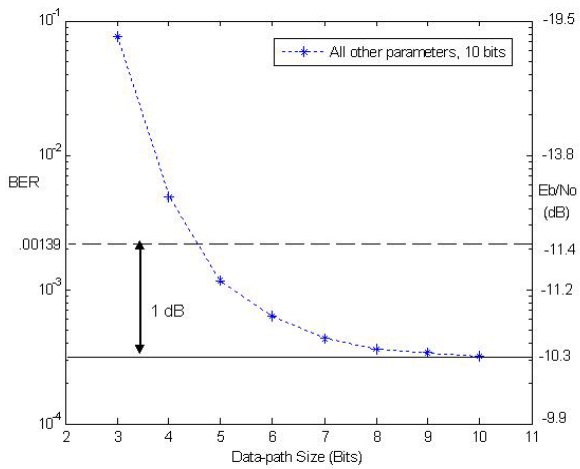

Figure 9. BER versus correlator height

were chosen independently for each of the receiver blocks assuming that their individual contributions to the overall implementation area were equal. A more realistic model would take into account different area-per-bit or power-per-bit contributions for each block of the receiver.

6. REFERENCES

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