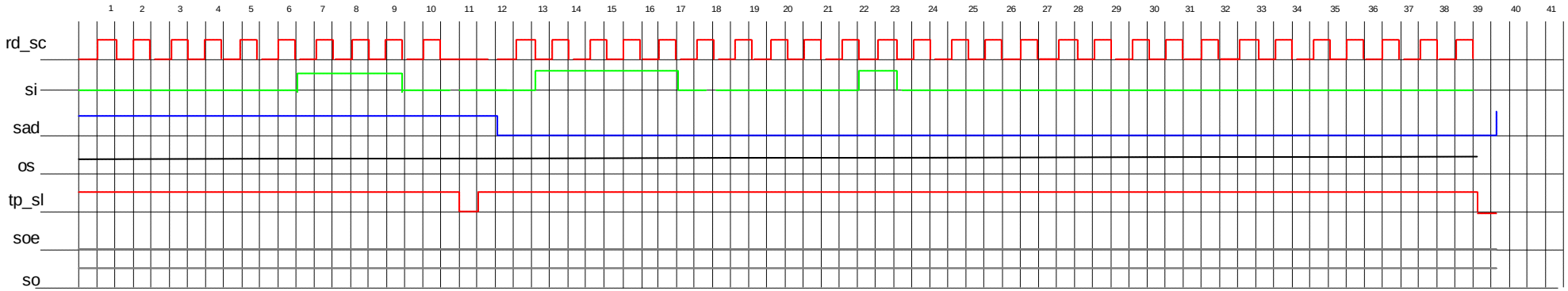
FIGURE 4.0: Operating mode Test for Amplitude and Attenuator

Test 4: Load CR3 for all channels enabled, MUX disabled, Vfb set to '30' on DAC



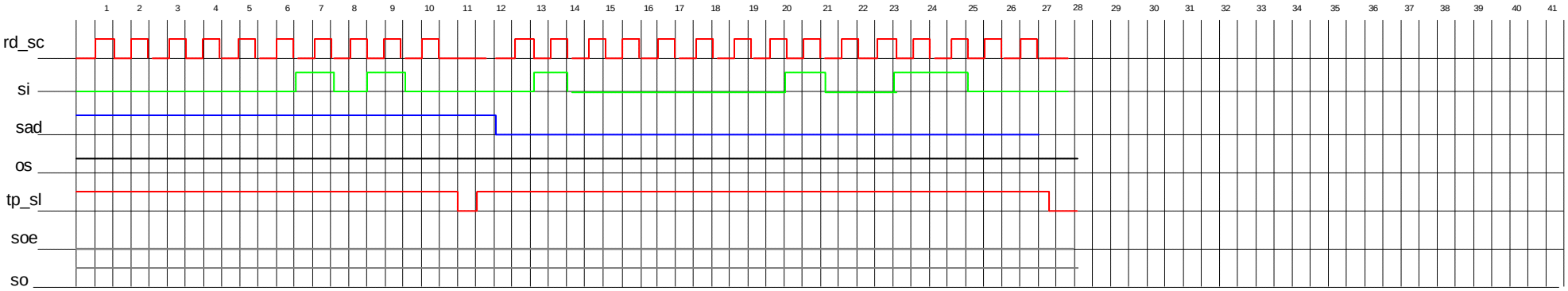
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

CR3 Register contents =

D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	M 5	M 4	M 3	M 2	M 1	F 6	F 5	F 4	F 3	F 2	F 1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

Figure 4.1: All channels pulsed at 2 fC input charge (test amplitude DAC = 2), 3 fC threshold (threshold DAC=50), Att=1(00b)in CR2 register



Address Register contents =

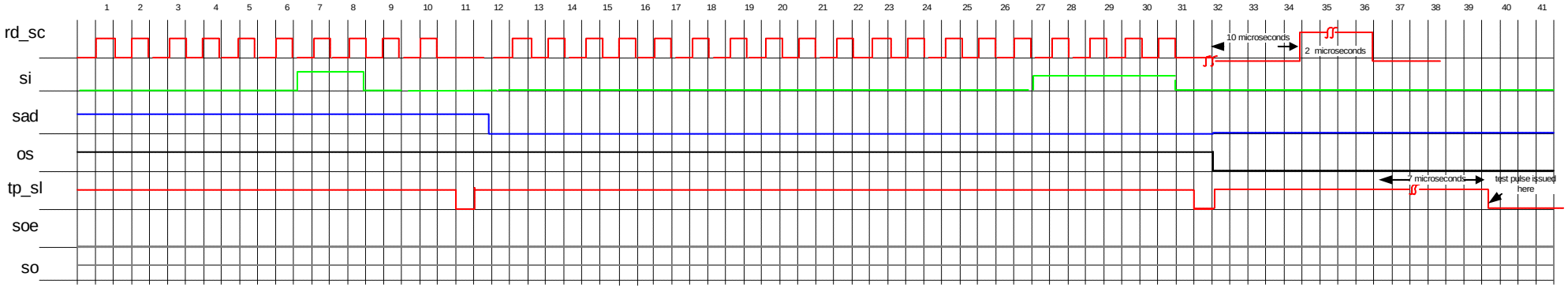
R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

CR2 Register contents =

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	1	0	0	1	0	0	0	0	0	0	1	0

FIGURE 4.1.a: Operating mode Test 4.1 for channels 1-4

Test 4.1a: Load CR1 for channels 1-4 pulsed, and steepest leakage slope



Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

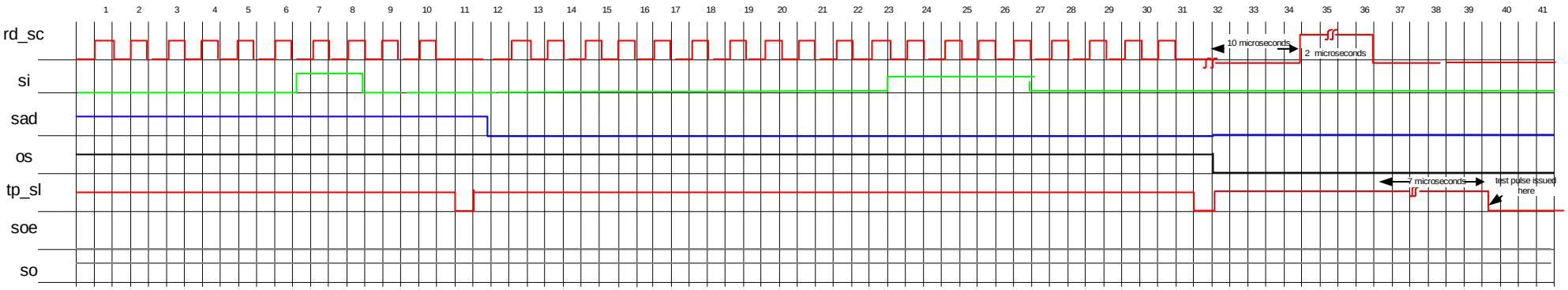
No outputs must fire.

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FIGURE 4.1.b: Operating mode Test 4.1 for channels 5-8

Test 4.1b: Load CR1 for channels 5-8 pulsed, and steepest leakage slope



Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

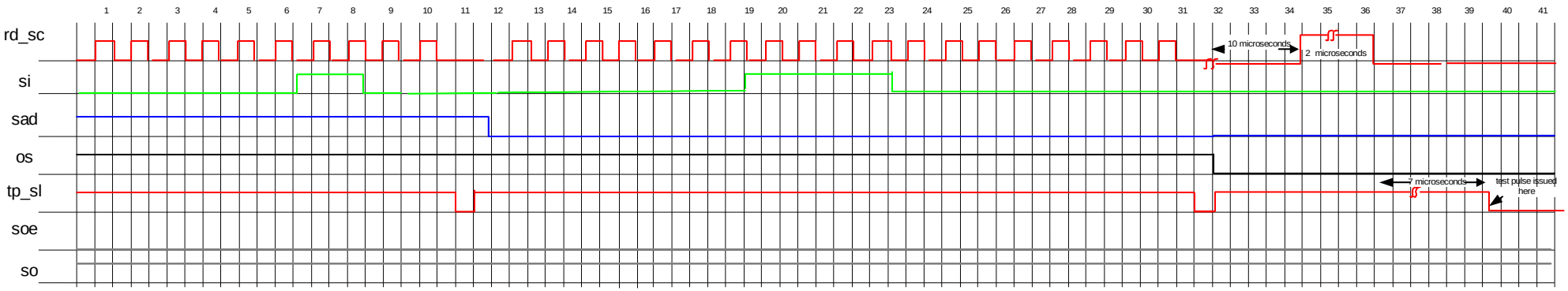
No outputs must fire.

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

FIGURE 4.1.c: Operating mode Test 4.1 for channels 9-12

Test 4.1c: Load CR1 for channels 9-12 pulsed, and steepest leakage slope



Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

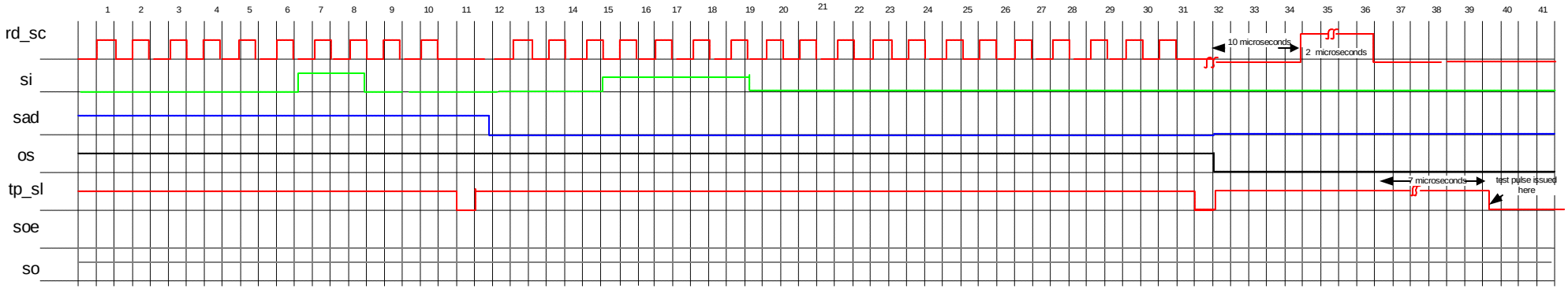
No outputs must fire.

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

FIGURE 4.1.d: Operating mode Test 4.1 for channels 13-16

Test 4.1d: Load CR1 for channels 13-16 pulsed, and steepest leakage slope



Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

No outputs must fire.

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0