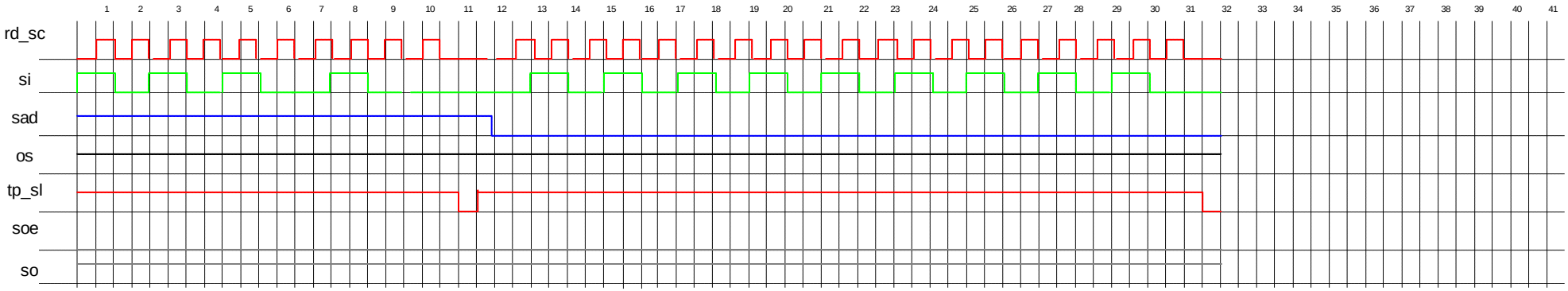
FIGURE 3A: Write to and Read back CR1 even bits

Test 3a: Write '1's to CR1 even bits



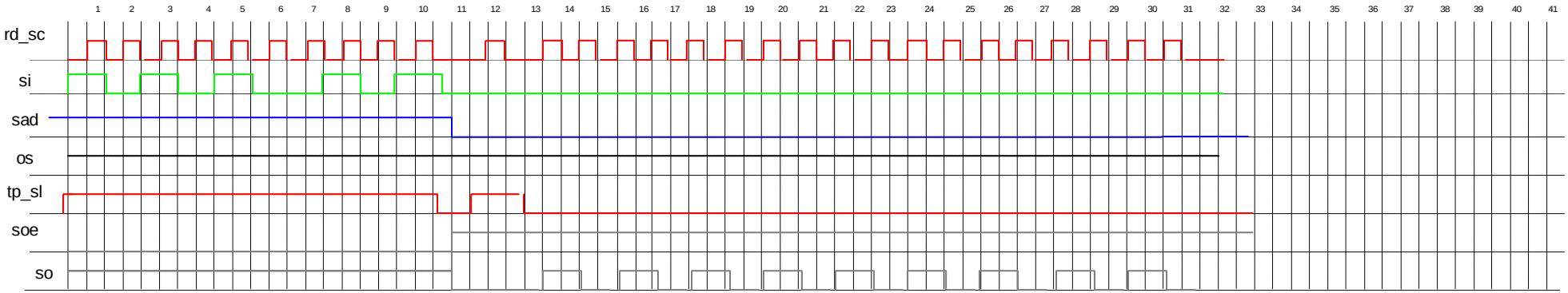
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	1	0	1	0	1

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Readback '1's from CR1 even bits



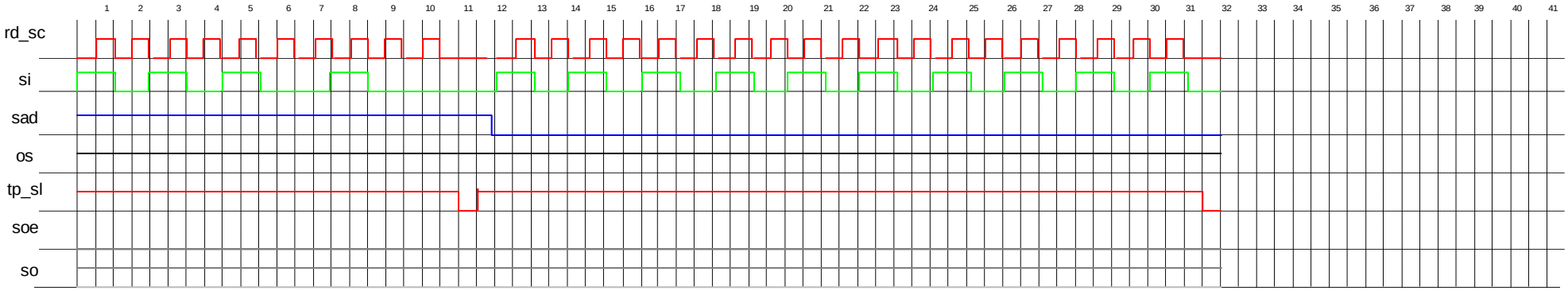
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	0	1	0	0	1	0	1	0	1

CR1 Register contents will be serially output through SO pin

FIGURE 3B: Write to and Read back CR1 odd bits

Test 3b: Write '1's to CR1 odd bits



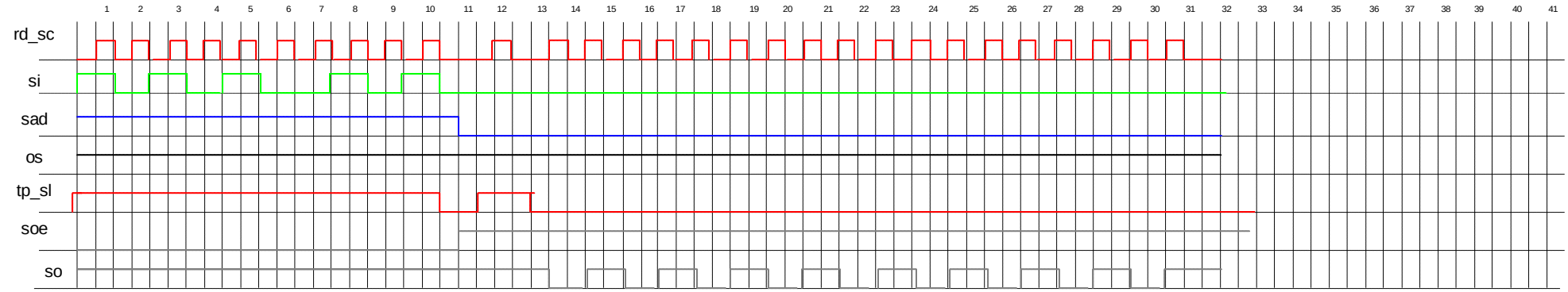
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	1	0	1	0	1

CR1 Register contents =

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Readback '1's from CR1 odd bits



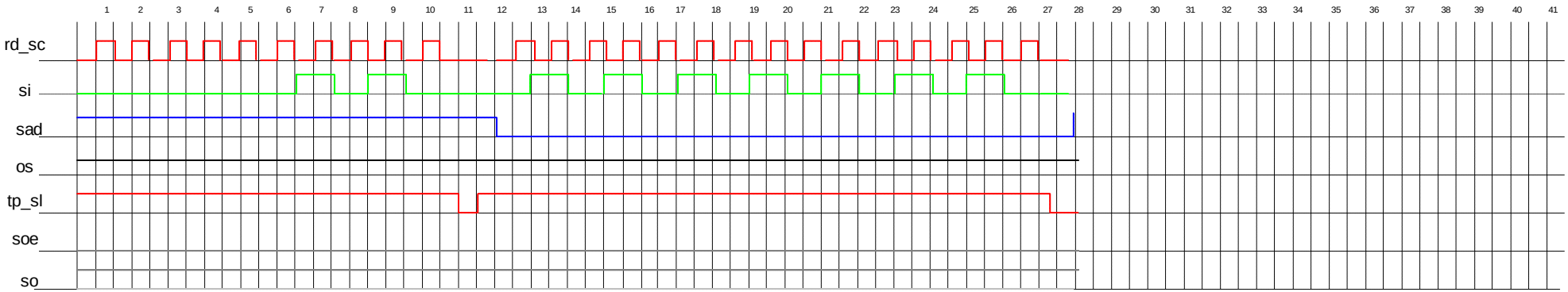
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	0	1	0	0	1	0	1	0	1

CR1 Register contents will be serially output through SO pin

FIGURE 3C: Write to and Read back CR2 even bits

Test 3c: Write '1's to CR2 even bits



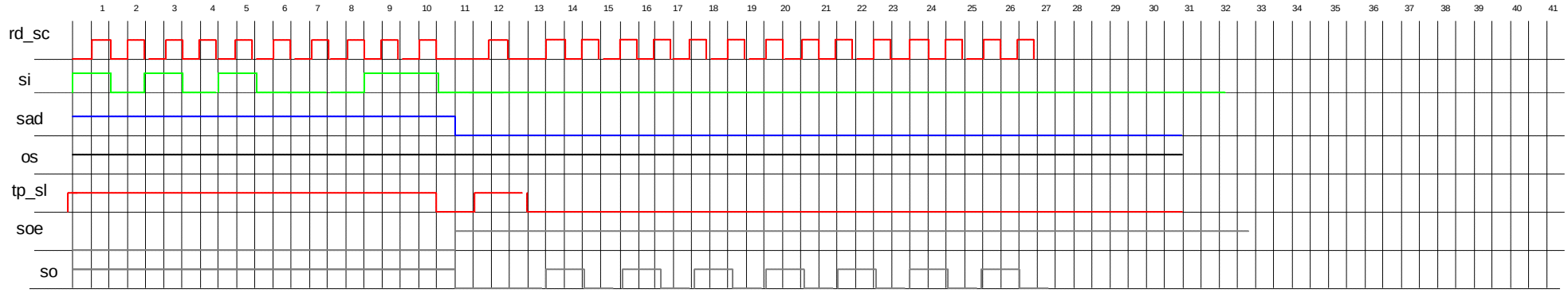
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

CR2 Register contents =

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Readback '1's from CR2 even bits



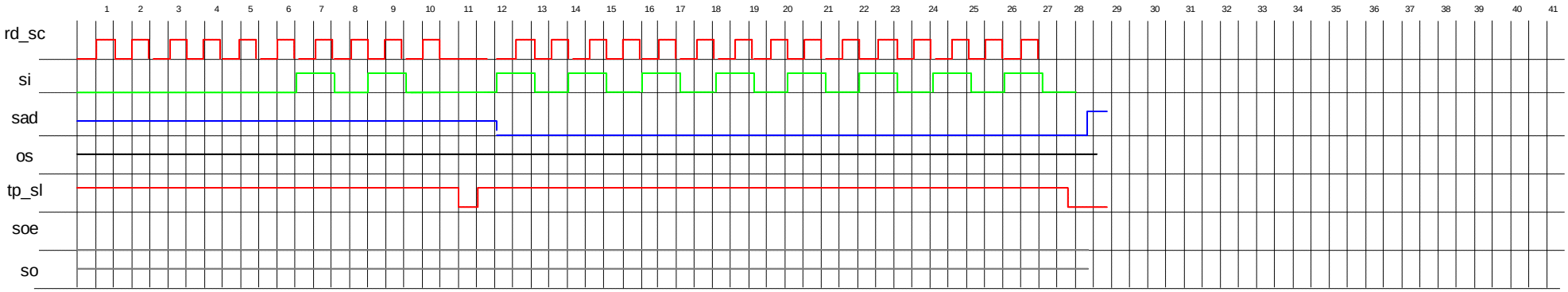
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	1	0	1	0	1

CR2 Register contents will be serially output through SO pin

FIGURE 3D: Write to and Read back CR2 odd bits

Test 3d: Write '1's to CR2 odd bits



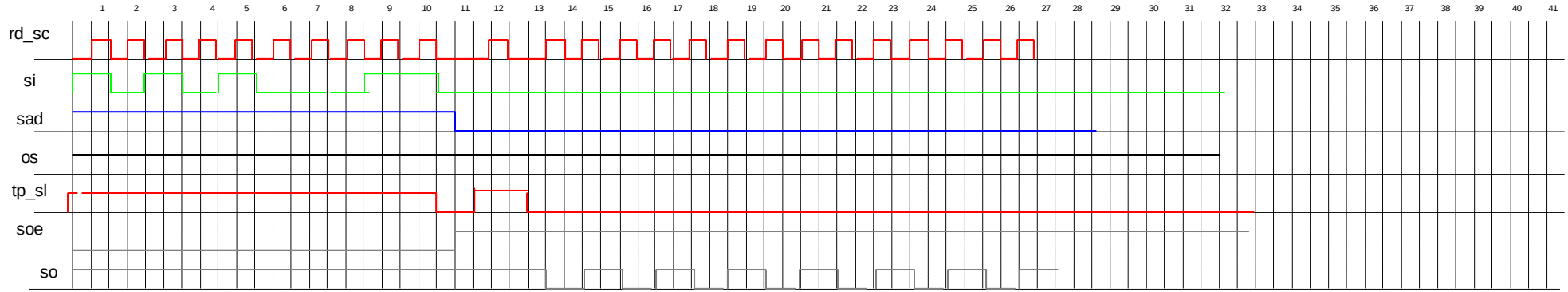
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

CR2 Register contents =

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Readback '1's from CR2 odd bits



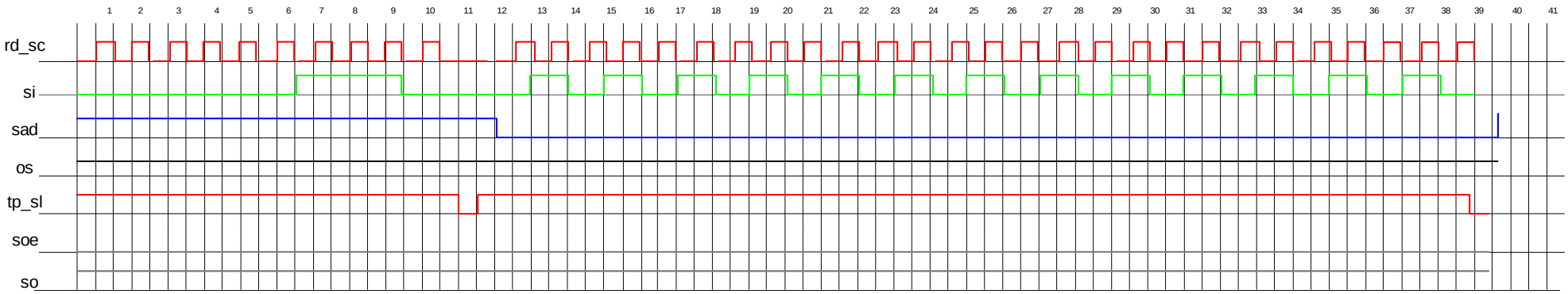
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	1	0	1	0	1

CR2 Register contents will be serially output through SO pin

FIGURE 3E: Write to and Read back CR3 even bits

Test 3e: Write '1's to CR3 even bits



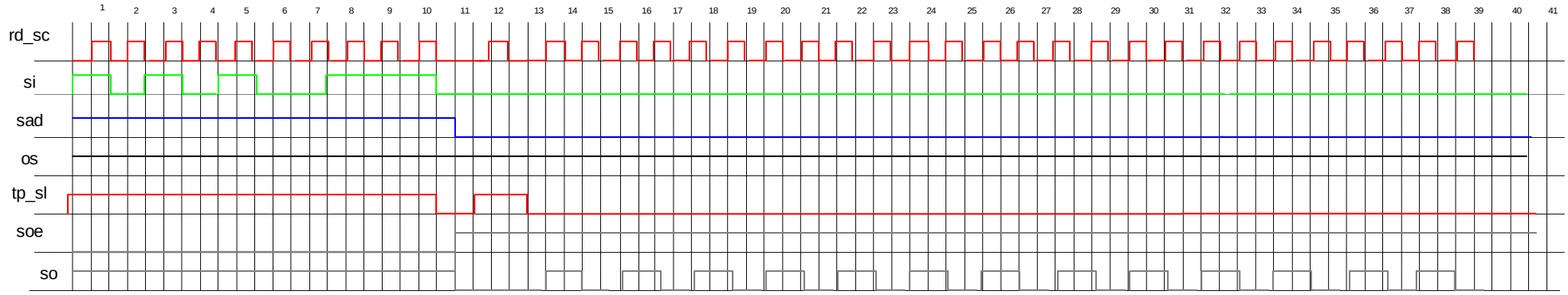
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

CR3 Register contents =

D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	M 5	M 4	M 3	M 2	M 1	F 6	F 5	F 4	F 3	F 2	F 1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Readback '1's from CR3 even bits



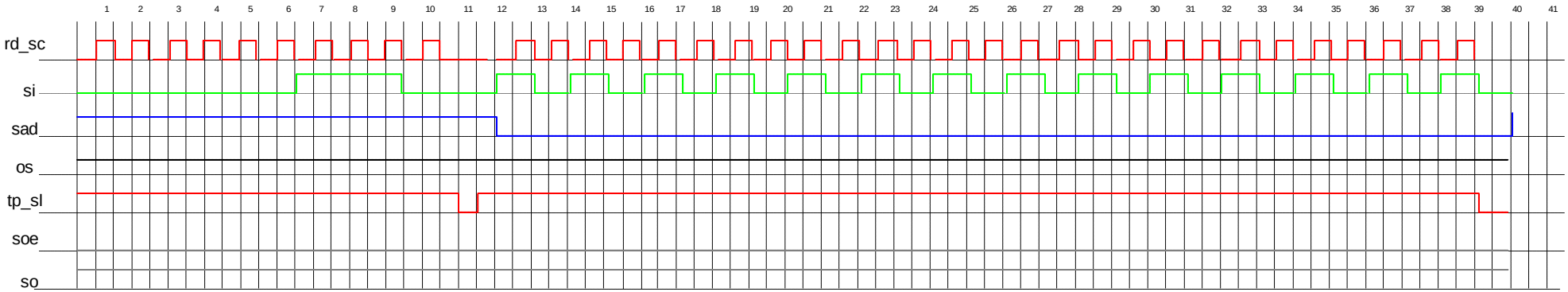
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	1	0	0	1	0	1	0	1

CR3 Register contents will be serially output through SO pin

FIGURE 3F: Write to and Read back CR3 odd bits

Test 3f: Write '1's to CR3 odd bits



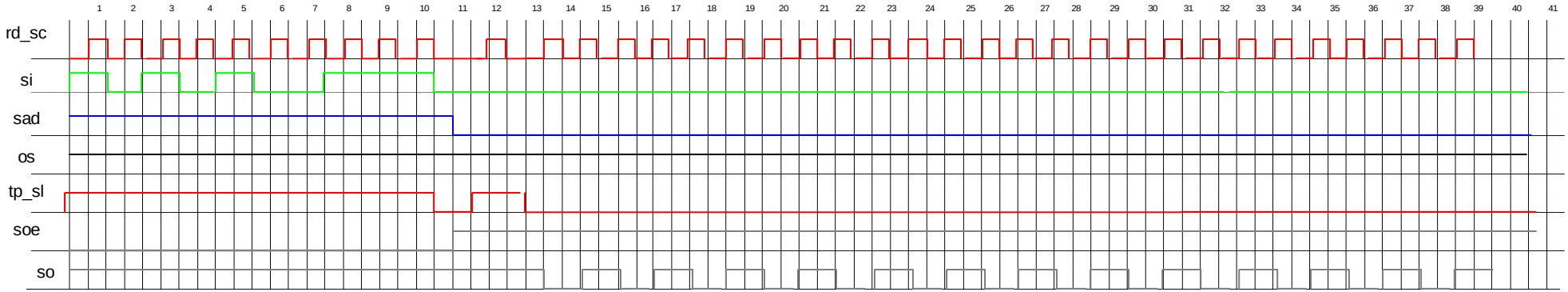
Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

CR3 Register contents =

D 16	D 15	D 14	D 13	D 12	D 11	D 10	D 9	D 8	D 7	D 6	D 5	D 4	D 3	D 2	D 1	M 5	M 4	M 3	M 2	M 1	F 6	F 5	F 4	F 3	F 2	F 1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Readback '1's from CR3 odd bits



Address Register contents =

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	1	0	0	1	0	1	0	1

CR3 Register contents will be serially output through SO pin