TGL98.V2 SERIAL DATA BITS

TGLD SERIAL ADDRESS REGISTER

msb									lsb
R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0

RW	0= write to TGLD registers; 1= read from TGLD registers
R1	Register address MSB; 00=no register, 01=CR1, 10=CR2, 11=CR3
R0	Register address LSB; 00=no register, 01=CR1, 10=CR2, 11=CR3
A6	TGLD Address BROADCAST bit
A5	MSB TGLD Address bit
A4	5SB TGLD Address bit
A3	4SB TGLD Address bit
A2	3SB TGLD Address bit
A1	2SB TGLD Address bit
A0	LSB TGLD Address bit

CR1: TEST PATTERN AND DECAY SLOPE COMPENSATION CONTROL REGISTER

msb																		lsb
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1

T1	0=diasable test pulse, 1 = enable test pulse, channel 1
T2	0=diasable test pulse, 1 = enable test pulse, channel 2
T3	0=diasable test pulse, 1 = enable test pulse, channel 3
T4	0=diasable test pulse, 1 = enable test pulse, channel 4
T5	0=diasable test pulse, 1 = enable test pulse, channel 5
T6	0=diasable test pulse, 1 = enable test pulse, channel 6
T7	0=diasable test pulse, 1 = enable test pulse, channel 7
T8	0=diasable test pulse, 1 = enable test pulse, channel 8
T9	0=diasable test pulse, 1 = enable test pulse, channel 9
T10	0=diasable test pulse, 1 = enable test pulse, channel 10
T11	0=diasable test pulse, 1 = enable test pulse, channel 11
T12	0=diasable test pulse, 1 = enable test pulse, channel 12
T13	0=diasable test pulse, 1 = enable test pulse, channel 13
T14	0=diasable test pulse, 1 = enable test pulse, channel 14
T15	0=diasable test pulse, 1 = enable test pulse, channel 15
T16	0=diasable test pulse, 1 = enable test pulse, channel 16
DS3	MSB, preamp decay slope MUX decoder, 111 = no decay
DS2	2SB, preamp decay slope MUX decoder,
DS1	LSB, preamp decay slope MUX decoder, 000 = max decay

CR2: ATTENUATOR, DISCRIMINATOR, THRESHOLD, TEST AMPLITUDE CONTROL REGISTER

msb														lsb
At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1

At2	MSB, C-R attenuator; 00=no atten, 01=1/3 atten,10=1/9 atten
At1	LSB, C-R attenuator; 00=no atten, 01=1/3 atten,10=1/9 atten
Vt6	MSB Discriminator voltage threshold DAC input; 111111 = min threshold
Vt5	5SB Discriminator voltage threshold DAC input
Vt4	4SB Discriminator voltage threshold DAC input
Vt3	3SB Discriminator voltage threshold DAC input
Vt2	2SB Discriminator voltage threshold DAC input
Vt1	LSB Discriminator voltage threshold DAC input
Ta7	MSB Test Pulse Amplitude DAC input; 1111111 = 127 fC
Ta6	6SB Test Pulse Amplitude DAC input
Ta5	5SB Test Pulse Amplitude DAC input
Ta4	4SB Test Pulse Amplitude DAC input
Ta3	3SB Test Pulse Amplitude DAC input
Ta2	2SB Test Pulse Amplitude DAC input
Ta1	LSB Test Pulse Amplitude DAC input

CR3: CHANNEL DISABLE, MUX AND FEEDBACK VOLTAGE CONTROL REGISTER

msb																									lsb
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1

D16	MSB, channel 16, 0=enable, 1 = disable
D15 - D2	15SB - 2SB, channel15 - channel 2, 0=enable, 1 = disable
D1	LSB, channel 1
M5	MUX enable/disable bit, 0=enable, 1=disable
M4	MSB, mux address; 1111 = channel 16 select
M3	3SB, mux address
M2	2SB, mux address
M1	LSB, mux address; 0000 = channel 1 select
F6	MSB, Vfb DAC, 11111 = 0.6v
F5	5SB, Vfb DAC
F4	4SB, Vfb DAC
F3	3SB, Vfb DAC
F2	2SB, Vfb DAC
F1	LSB, Vfb DAC, 00000 = 2.58V

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EXAMPLE SERIAL DATA INPUT FOR LOADING ALL THREE REGISTERS OF A TGL98.v2 (TGLD1) CHIP ON A ROC

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	1	0	1

CR1: TEST PATTERN CONTROL REGISTER (msb → lsb)

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	1	0	1

CR2: ATTEN., THRESHOLD, TEST AMP. CONTROL REGISTER (msb → lsb)

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

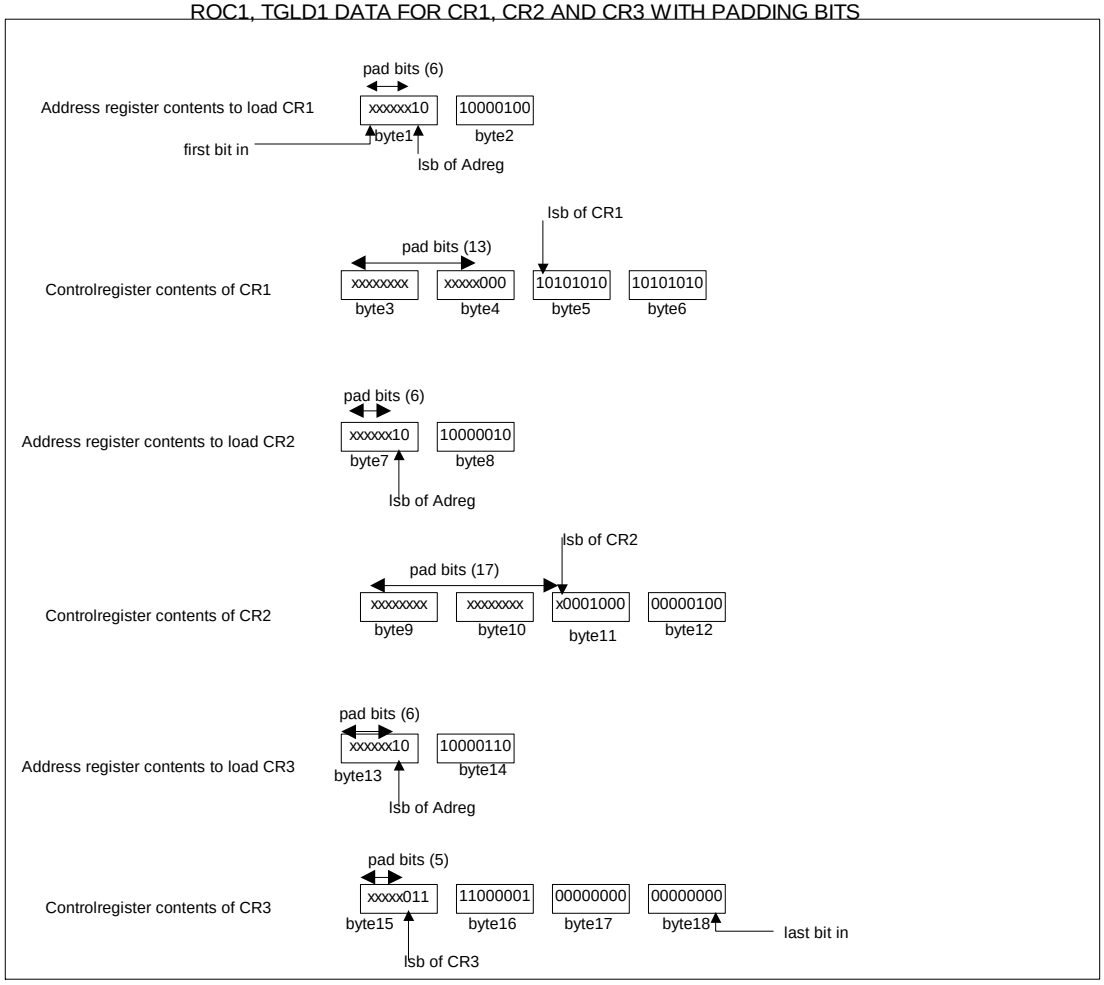
TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	1	0	1

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER (msb → lsb)

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3 WITH PADDING BITS



SERIAL STRING DATA FOR LOADING REGISTERS CR1, CR2 AND CR3 CONSECUTIVELY FOR TGLD1 IN ROC1 FOR THIS EXAMPLE IS:

XXXXXX10 10000100 XXXXXXXX XXXXX000 10101010 10101010 XXXXXX10 10000010 XXXXXXXX XXXXXXXX X0001000 00000100 XXXXXX10 10000110 XXXXX011 11000001 00000000 00000000

FIRST BIT IN ↑ ↑ LAST BIT

SERIAL DATA INPUT FOR LOADING ALL THREE TGLDs (TGLD1, TGLD2 AND TGLD3) OF 1 ROC

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	1	0	1

CR1: TEST PATTERN CONTROL REGISTER (msb → lsb)

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	1	0	1

CR2: ATTEN., THRESHOLD, TEST AMP. CONTROL REGISTER (msb → lsb)

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	1	0	1

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER (msb → lsb)

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

ROC1, TGLD2 DATA FOR CR1, CR2 AND CR3

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	1	1	0

CR1: TEST PATTERN CONTROL REGISTER (msb → lsb)

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	1	1	0

CR2: ATTEN., THRESHOLD, TEST AMP. CONTROL REGISTER (msb → lsb)

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	1	1	0

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER (msb → lsb)

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

ROC1, TGLD3 DATA FOR CR1, CR2 AND CR3

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	1	1	1

CR1: TEST PATTERN CONTROL REGISTER (msb → lsb)

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	1	1	1

CR2: ATTEN., THRESHOLD, TEST AMP. CONTROL REGISTER (msb → lsb)

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	1	1	1

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER (msb → lsb)

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3

xxxxxx10	10000100		
xxxxxxxx	xxxxx000	10101010	10101010
xxxxxx10	10000010		
xxxxxxxx	xxxxxxxx	x0001000	00000100
xxxxxx10	10000110		
xxxxx011	11000001	00000000	00000000

ROC1, TGLD2 DATA FOR CR1, CR2 AND CR3

xxxxxx01	10000100		
xxxxxxxx	xxxxx000	10101010	10101010
xxxxxx01	10000010		
xxxxxxxx	xxxxxxxx	x0001000	00000100
xxxxxx01	10000110		
xxxxx011	11000001	00000000	00000000

ROC1, TGLD3 DATA FOR CR1, CR2 AND CR3

xxxxxx11	10000100		
xxxxxxxx	xxxxx000	10101010	10101010
xxxxxx11	10000010		
xxxxxxxx	xxxxxxxx	x0001000	00000100
xxxxxx11	10000110		
xxxxx011	11000001	00000000	00000000

DATA PACKET FOR 1 ROW OF PC SECTOR (9 ROCS)
Note: All 27 chips are loaded for test pulse even channels,decay slope = steepest setting,atten = 0; threshold = ~5fC, test charge =~8fC, all channels enabled, mux disabled, feedback voltage = 1.5v

ROC1, TGLD1, TGLD2 and TGLD3

xxxxxx10	10000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	10000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	10000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	10000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	10000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	10000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	10000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	10000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	10000110			
xxxxx011	11000001	00000000	00000000	CR3

ROC2, TGLD1, TGLD2 and TGLD3

xxxxxx10	01000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	01000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	01000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	01000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	01000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	01000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	01000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	01000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	01000110			
xxxxx011	11000001	00000000	00000000	CR3

ROC3, TGLD1, TGLD2 and TGLD3

xxxxxx10	11000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	11000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	11000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	11000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	11000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	11000110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	11000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	11000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	11000110			
xxxxx011	11000001	00000000	00000000	CR3

ROC4, TGLD1, TGLD2 and TGLD3

xxxxxx10	00100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	00100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	00100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	00100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	00100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	00100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	00100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	00100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	00100110			
xxxxx011	11000001	00000000	00000000	CR3

ROC5, TGLD1, TGLD2 and TGLD3

xxxxxx10	10100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	10100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	10100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	10100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	10100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	10100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	10100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	10100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	10100110			
xxxxx011	11000001	00000000	00000000	CR3

ROC6, TGLD1, TGLD2 and TGLD3

xxxxxx10	01100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	01100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	01100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	01100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	01100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	01100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	01000100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	01000010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	01000110			
xxxxx011	11000001	00000000	00000000	CR3

ROC7, TGLD1, TGLD2 and TGLD3

xxxxxx10	11100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	11100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	11100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	11100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	11100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	11100110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	11100100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	11100010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	11100110			
xxxxx011	11000001	00000000	00000000	CR3

ROC8, TGLD1, TGLD2 and TGLD3

xxxxxx10	00010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	00010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	00010110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	00010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	00010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	00010110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	00010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	00010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	00010110			
xxxxx011	11000001	00000000	00000000	CR3

ROC9, TGLD1, TGLD2 and TGLD3

xxxxxx10	10010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx10	10010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx10	10010110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx01	10010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx01	10010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx01	10010110			
xxxxx011	11000001	00000000	00000000	CR3
xxxxxx11	10010100			
xxxxxxxx	xxxxx000	10101010	10101010	CR1
xxxxxx11	10010010			
xxxxxxxx	xxxxxxxx	x0001000	00000100	CR2
xxxxxx11	10010110			
xxxxx011	11000001	00000000	00000000	CR3

SERIAL DATA FOR LOADING 1 ROW OF 9 ROCS with 3 TGL98.V2 CHIPS ON EACH ROC

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