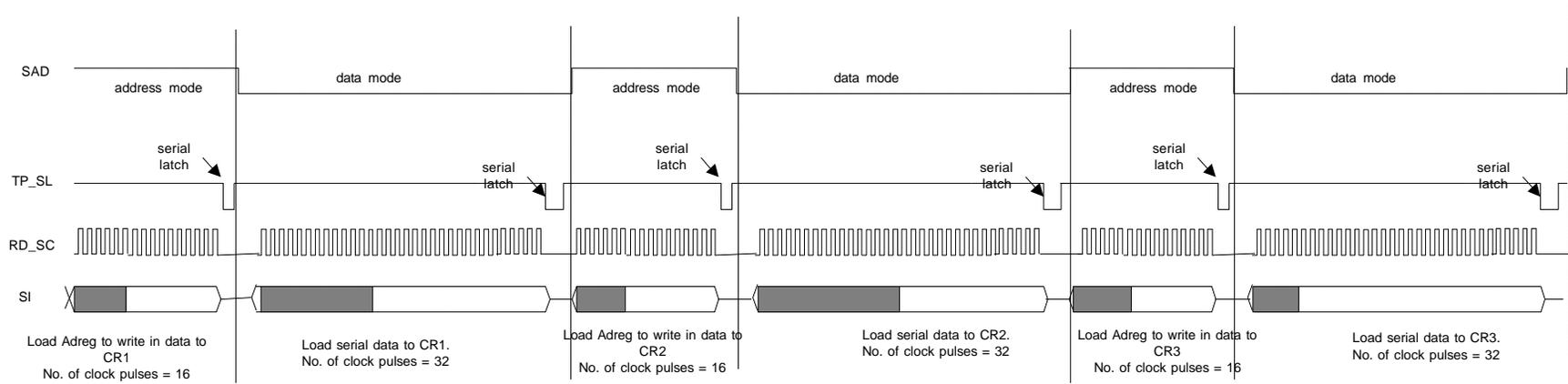


TIMING DIAGRAM FOR SERIAL DATA DOWNLOAD INTO ALL 3 REGISTERS OF A TGL98.V2 CHIP



TIMING DIAGRAM FOR SERIAL DATA UPLOAD FROM ALL 3 REGISTERS OF A TGL98.V2 CHIP

