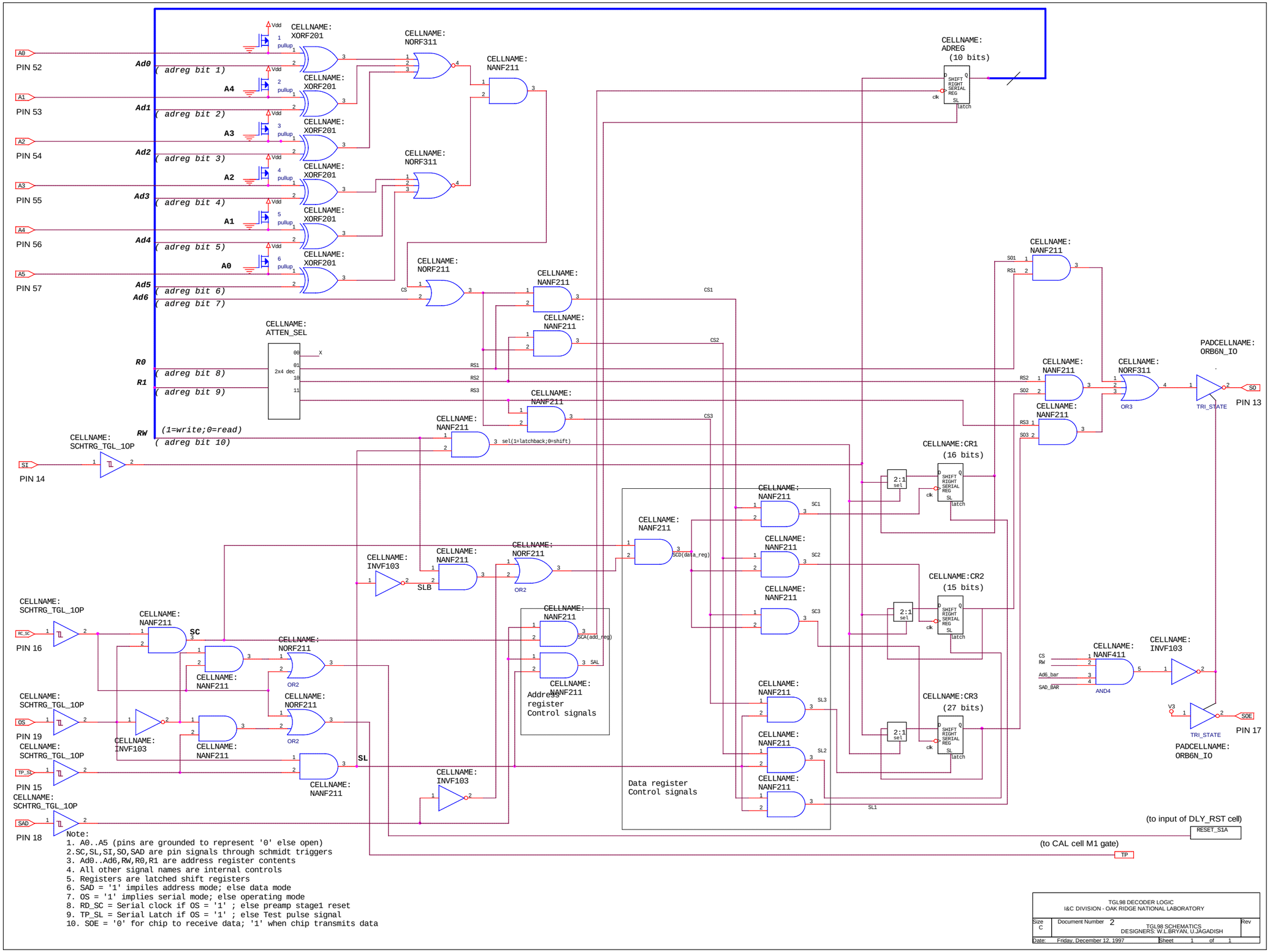

Note:
1. A0..A5 (pins are grounded to represent '0' else open)
2.SC,SL,SI,SO,SAD are pin signals through schmidt triggers
3. Ad0..Ad6,RW,R0,R1 are address register contents
4. All other signal names are internal controls
5. Registers are latched shift registers
6. SAD = '1' impiles address mode; else data mode
7. OS = '1' implies serial mode; else operating mode
8. RD_SC = Serial clock if OS = '1' ; else preamp stage1 reset
9. TP_SL = Serial Latch if OS = '1' ; else Test pulse signal
10. SOE = '0' for chip to receive data; '1' when chip transmits data

TGL98 DECODER LOGIC
I&C DIVISION - OAK RIDGE NATIONAL LABORATORY

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