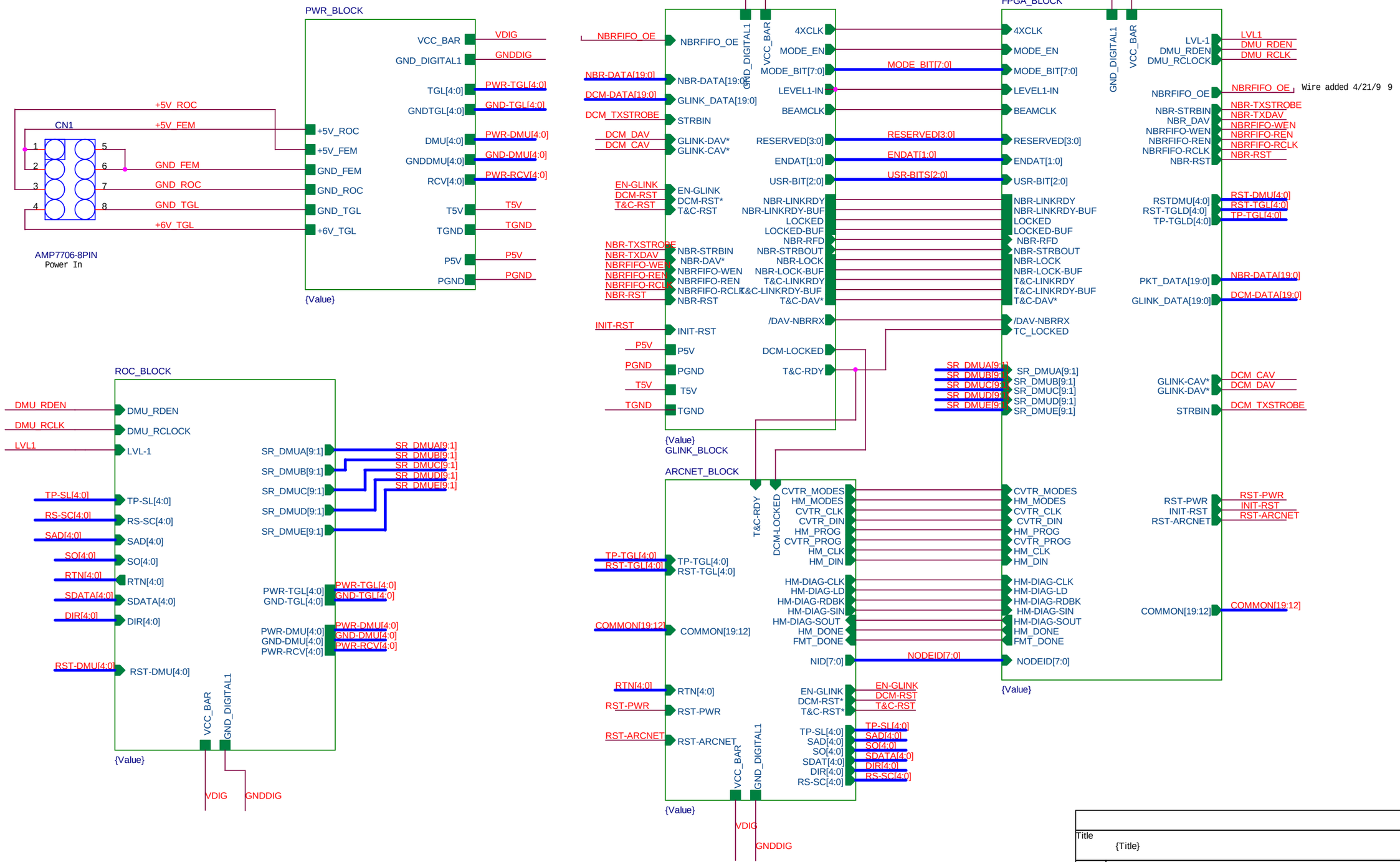
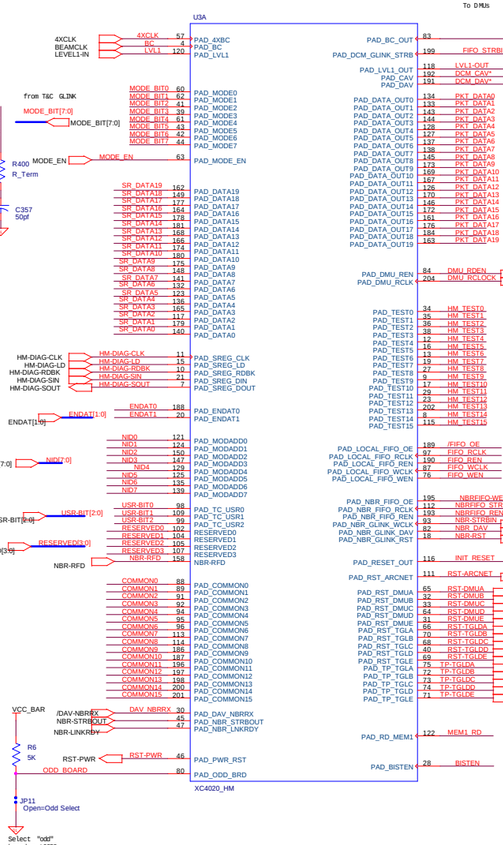
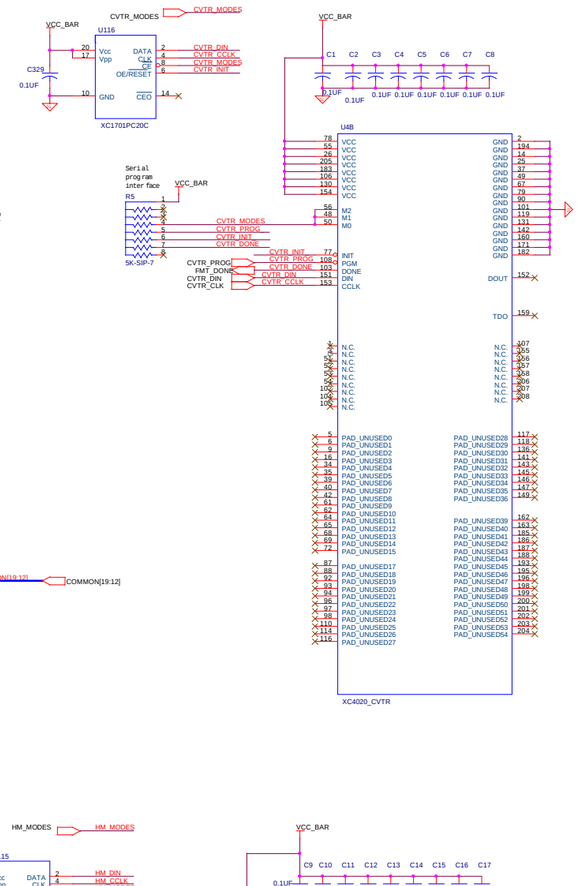

PWR_BLOCK
VCC_BAR
GND_DIGITAL1
TGL[4:0]
GNDTGL[4:0]
DMU[4:0]
GNDDMU[4:0]
RCV[4:0]
T5V
TGND
P5V
PGND
+5V_ROC
+5V_FEM
GND_FEM
GND_ROC
GND_TGL
+6V_TGL
VDIG
GNDDIG
PWR-TGL[4:0]
GND-TGL[4:0]
PWR-DMU[4:0]
GND-DMU[4:0]
PWR-RCV[4:0]
{Value}
CN1
AMP7706-8PIN
Power In
ROC_BLOCK
DMU_RDEN
DMU_RCLOCK
LVL-1
TP-SL[4:0]
RS-SC[4:0]
SAD[4:0]
SO[4:0]
RTN[4:0]
SDATA[4:0]
DIR[4:0]
RST-DMU[4:0]
SR_DMUA[9:1]
SR_DMUB[9:1]
SR_DMUC[9:1]
SR_DMUD[9:1]
SR_DMUE[9:1]
GLINK_BLOCK
NBRFIFO_OE
NBR-DATA[19:0]
GLINK_DATA[19:0]
STRBIN
GLINK-DAV*
GLINK-CAV*
EN-GLINK
DCM-RST*
T&C-RST
NBR-STRBIN
NBR-DAV*
NBRFIFO-WEN
NBRFIFO-REN
NBRFIFO-RCLK
NBR-RST
INIT-RST
4XCLK
MODE_EN
MODE_BIT[7:0]
LEVEL1-IN
BEAMCLK
RESERVED[3:0]
ENDAT[1:0]
USR-BIT[2:0]
NBR-LINKRDY
NBR-LINKRDY-BUF
LOCKED
LOCKED-BUF
NBR-RFD
NBR-STRBOUT
NBR-LOCK
NBR-LOCK-BUF
T&C-LINKRDY
T&C-LINKRDY-BUF
T&C-DAV*
/DAV-NBRRX
DCM-LOCKED
T&C-RDY
{Value}
ARCNET_BLOCK
T&C-RDY
DCM-LOCKED
CVTR_MODES
HM_MODES
CVTR_CLK
CVTR_DIN
HM_PROG
CVTR_PROG
HM_CLK
HM_DIN
TP-TGL[4:0]
RST-TGL[4:0]
COMMON[19:12]
HM-DIAG-CLK
HM-DIAG-LD
HM-DIAG-RDBK
HM-DIAG-SIN
HM-DIAG-SOUT
HM_DONE
FMT_DONE
NID[7:0]
RTN[4:0]
RST-PWR
RST-ARCNET
TP-SL[4:0]
SAD[4:0]
SO[4:0]
SDAT[4:0]
DIR[4:0]
RS-SC[4:0]
{Value}
FPGA_BLOCK
4XCLK
MODE_EN
MODE_BIT[7:0]
LEVEL1-IN
BEAMCLK
RESERVED[3:0]
ENDAT[1:0]
USR-BIT[2:0]
NBR-LINKRDY
NBR-LINKRDY-BUF
LOCKED
LOCKED-BUF
NBR-RFD
NBR-STRBOUT
NBR-LOCK
NBR-LOCK-BUF
T&C-LINKRDY
T&C-LINKRDY-BUF
T&C-DAV*
/DAV-NBRRX
TC_LOCKED
SR_DMUA[9:1]
SR_DMUB[9:1]
SR_DMUC[9:1]
SR_DMUD[9:1]
SR_DMUE[9:1]
CVTR_MODES
HM_MODES
CVTR_CLK
CVTR_DIN
HM_PROG
CVTR_PROG
HM_CLK
HM_DIN
HM-DIAG-CLK
HM-DIAG-LD
HM-DIAG-RDBK
HM-DIAG-SIN
HM-DIAG-SOUT
HM_DONE
FMT_DONE
NODEID[7:0]
{Value}
LVL-1
DMU_RDEN
DMU_RCLOCK
NBRFIFO_OE
NBR-STRBIN
NBR_DAV
NBRFIFO-WEN
NBRFIFO-REN
NBRFIFO-RCLK
NBR-RST
RSTDMU[4:0]
RST-TGLD[4:0]
TP-TGLD[4:0]
PKT_DATA[19:0]
GLINK_DATA[19:0]
GLINK-CAV*
GLINK-DAV*
STRBIN
RST-PWR
INIT-RST
RST-ARCNET
COMMON[19:12]
LVL1
DMU_RDEN
DMU_RCLK
NBRFIFO_OE
Wire added 4/21/9 9
NBR-TXSTROBE
NBR-TXDAV
NBRFIFO-WEN
NBRFIFO-REN
NBRFIFO-RCLK
NBR-RST
RST-DMU[4:0]
RST-TGL[4:0]
TP-TGL[4:0]
NBR-DATA[19:0]
DCM-DATA[19:0]
DCM_CAV
DCM_DAV
DCM_TXSTROBE
RST-PWR
INIT-RST
RST-ARCNET
COMMON[19:12]
Title
{Title}
Size
B
Document Number
{Doc}
Rev
{RevCode}
Date:
Wednesday, April 21, 1999
Sheet
1
of
6

RST-POWERUP resets the registers for the mode control section.

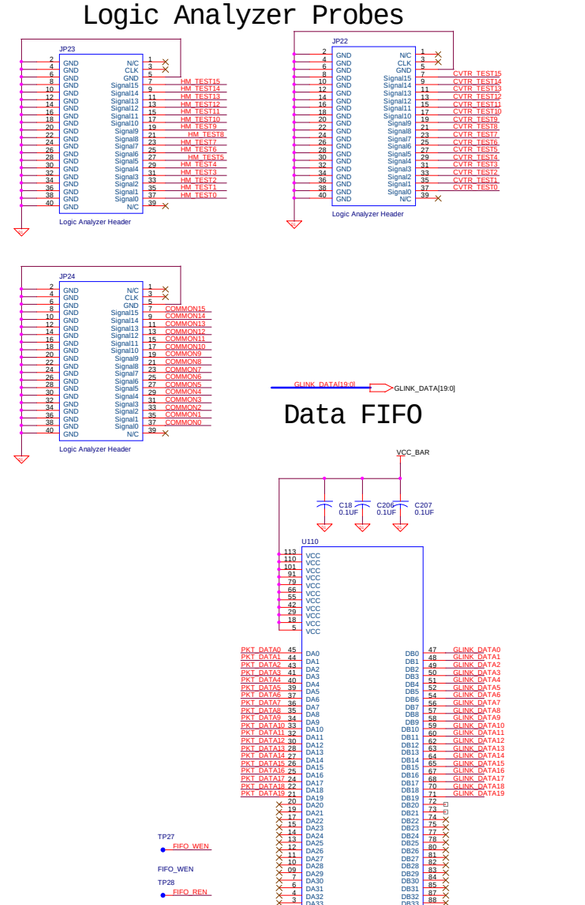
HEAP MANAGER



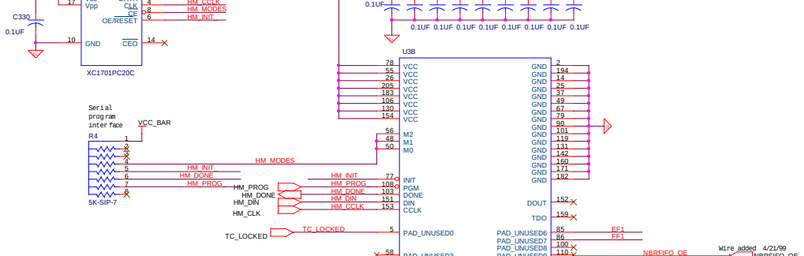
SERIAL to PARALLEL

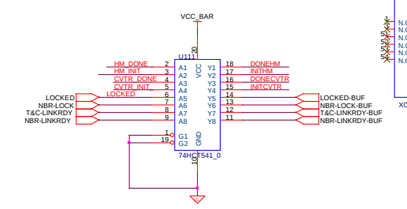


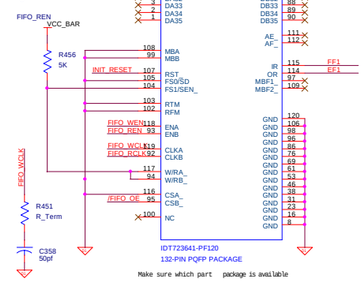
Logic Analyzer Probes



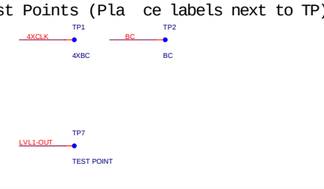
Data FIFO



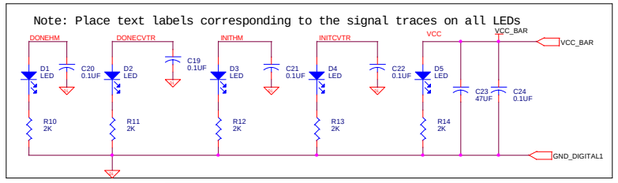




Other Test Points (Pla ce labels next to TP)



Note: Place text labels corresponding to the signal traces on all LEDs



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REV	MF	DESCRIPTION OR MEMO NO. REVISION OR I SSUE PURPOSE	FILE DATE	BY	ENGR	APVD
					APPROVALS	

TOLERA NCES UNLESS OTHERWI SE SPECIFIED
FRACT IONS
XX DEC IMALS
XXX DEC IMALS
ANGLES
BREAK SHA RP EDGES MAX.
FINI SH RMS

DRAWN BY	
DRAWING CHECK	
ENGIN EER	M. C. SM ITH 1/8/9
APPRO VED	
DRAWING A PPROVALS	DATE

PRINTED CIRCUIT BOARD — REFERENCE DRAWINGS

SKF-9 70-2 R1 — NUMBER

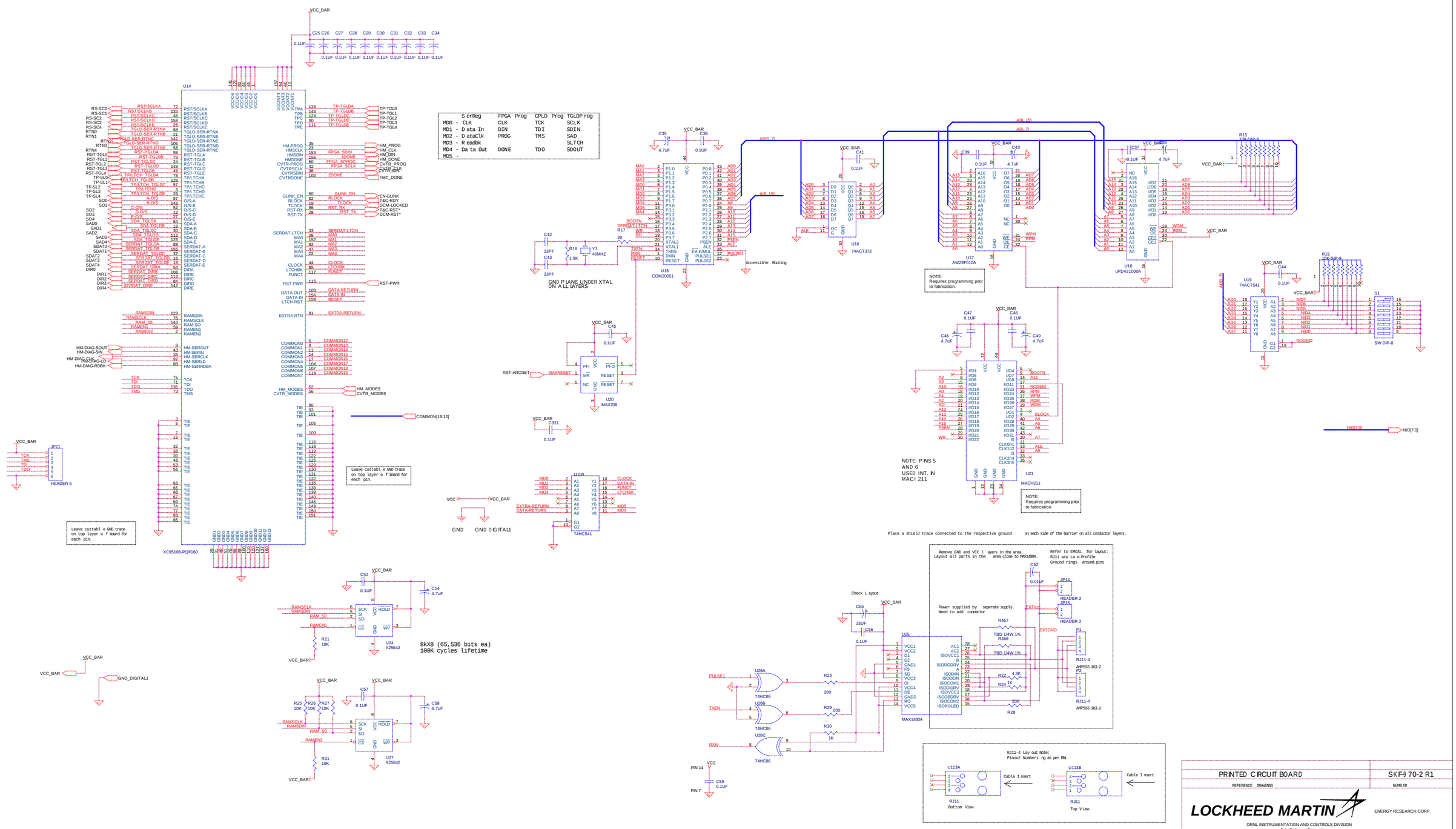
LOCKHEED MARTIN — ENERGY RESEARCH CORP.

ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee

PADS H EAP MANAGER (NUMBERS) SC EMATIC

FILE DATE	FILE P OINT	BLDG	SHT.	OF	TYPE
	HC-1 EC-1	3500	5	5	SD

SCALE	ID		REV
NTS	I & C	SKF-9 70-1	1


U14
XC95108-PQF160
U15
COM20051
U16
uPD431000A
U17
AM29F010A
U18
74ACT373
U19
74ACT541
U20
MAX708
U21
MACH211
U24
X25642
U27
X25642
U25
MAX1480A
U109
74HC541
JP21
HEADER 6
S1
SW DIP-8
R15
10K-SIP-9
R19
10K-SIP-9
Y1
40MHZ
Accessible Routing
GND PLANE UNDER XTAL
ON ALL LAYERS
NOTE:
Requires programming prior
to fabrication.
NOTE: PINS 5
AND 6
USED INT. IN
MACH 211
Leave cuttable GND trace
on top layer of board for
each pin.
8kX8 (65,536 bits ea)
100K cycles lifetime
Place a shield trace connected to the respective ground on each side of the barrier on all conductor layers.
Remove GND and VCC layers in the area.
Layout all parts in the area close to MAX1480A.
Refer to EMCAL for layout:
RJ11 are Low Profile
Ground rings around pins
Power supplied by seperate supply.
Need to add connector
Check Layout
RJ11-4 Lay out Note:
Pinout Numbering as per BNL
Cable Insert
RJ11
Bottom View
Top View
NOTE:
11,880 TGLD bits / FEM
178,096 FPGA bits / XC4010
19,598 CPLD bits/ XC95108 (10K cycles lifetime)
(or 12,960est. CPLD bits/ XC95144
or 26,390 CPLD bits/ XC95216)
PRINTED CIRCUIT BOARD
SKF-9 70-2 R1
REFERENCE DRAWINGS
NUMBER
LOCKHEED MARTIN
ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee
PADS ARCNET SCHEMATIC
PHENIX
TYPE
SD
FILE DATE
FILE POINT
MC-1 EC-1
BLDG
3500
SHT.
1
OF
5
SCALE
NTS
ID
I & C
SKF-9 70-1
REV
1
TOLERANCES
UNLESS OTHERWISE SPECIFIED
DRAWN BY
DRAWING CHECK
ENGINEER
M. C. SMITH
APPROVED
DRAWING APPROVALS
DATE
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REVISION OR ISSUE PURPOSE
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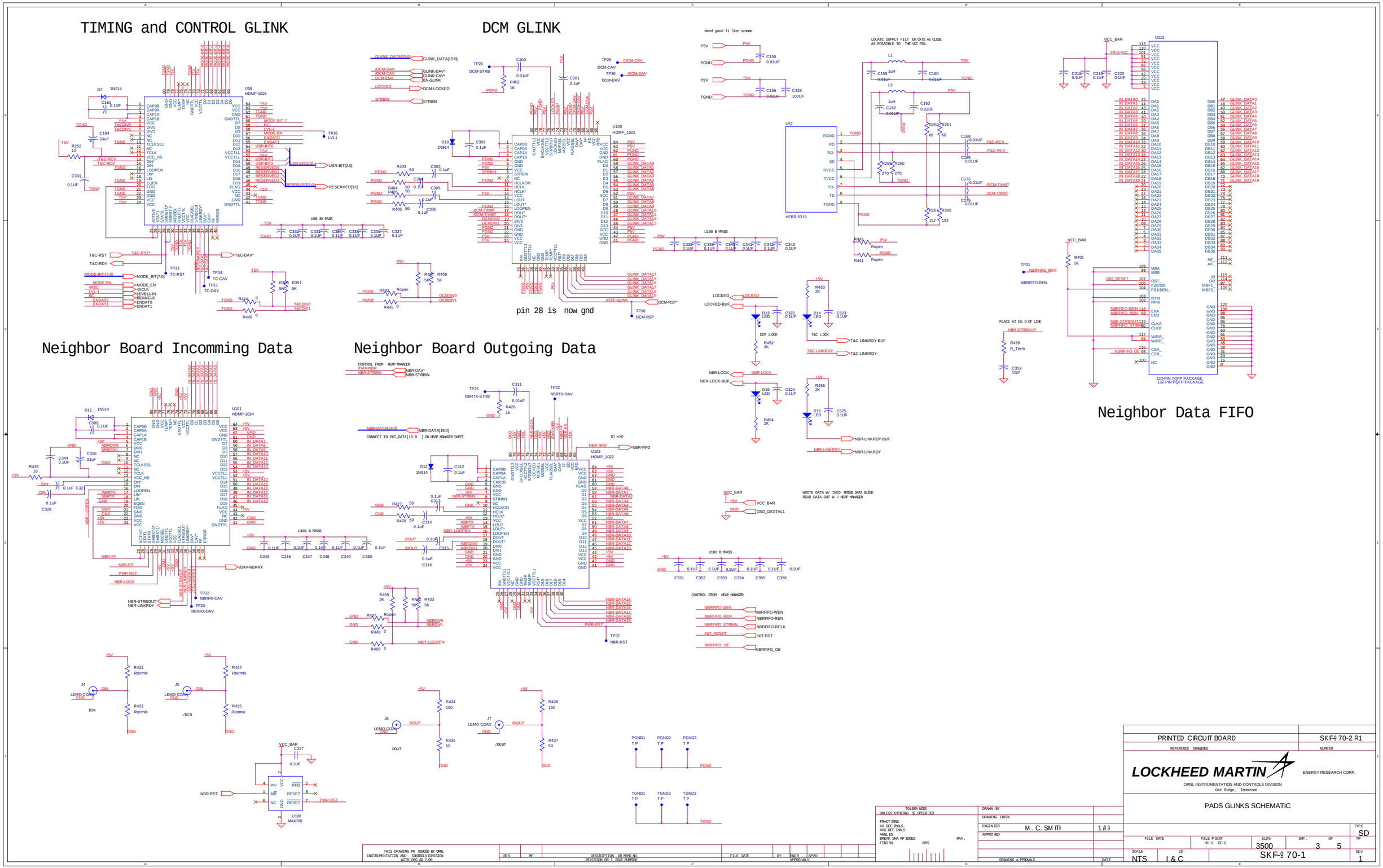
TIMING and CONTROL GLINK
DCM GLINK
Neighbor Board Incomming Data
Neighbor Board Outgoing Data
Neighbor Data FIFO
pin 28 is now gnd
U56 HDMP-1024
U100 HDMP_1022
U101 HDMP-1024
U102 HDMP_1022
U57 HFBR-5315
U112
U108 MAX708
PRINTED CIRCUIT BOARD
SKF-970-2 R1
REFERENCE DRAWINGS
NUMBER
LOCKHEED MARTIN
ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee
PADS GLINKS SCHEMATIC
DRAWN BY
DRAWING CHECK
ENGINEER
APPROVED
DRAWING APPROVALS
DATE
TOLERANCES
UNLESS OTHERWISE SPECIFIED
FRACTIONS
XX DECIMALS
XXX DECIMALS
ANGLES
BREAK SHARP EDGES
FINISH
RMS
MAX.
M. C. SMITH
TYPE
SD
FILE DATE
FILE POINT
BLDG
SHT.
OF
MF
3500
3
5
SCALE
NTS
ID
I & C
SKF-970-1
REV
1
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DESCRIPTION OR MEMO NO.
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FILE DATE
BY
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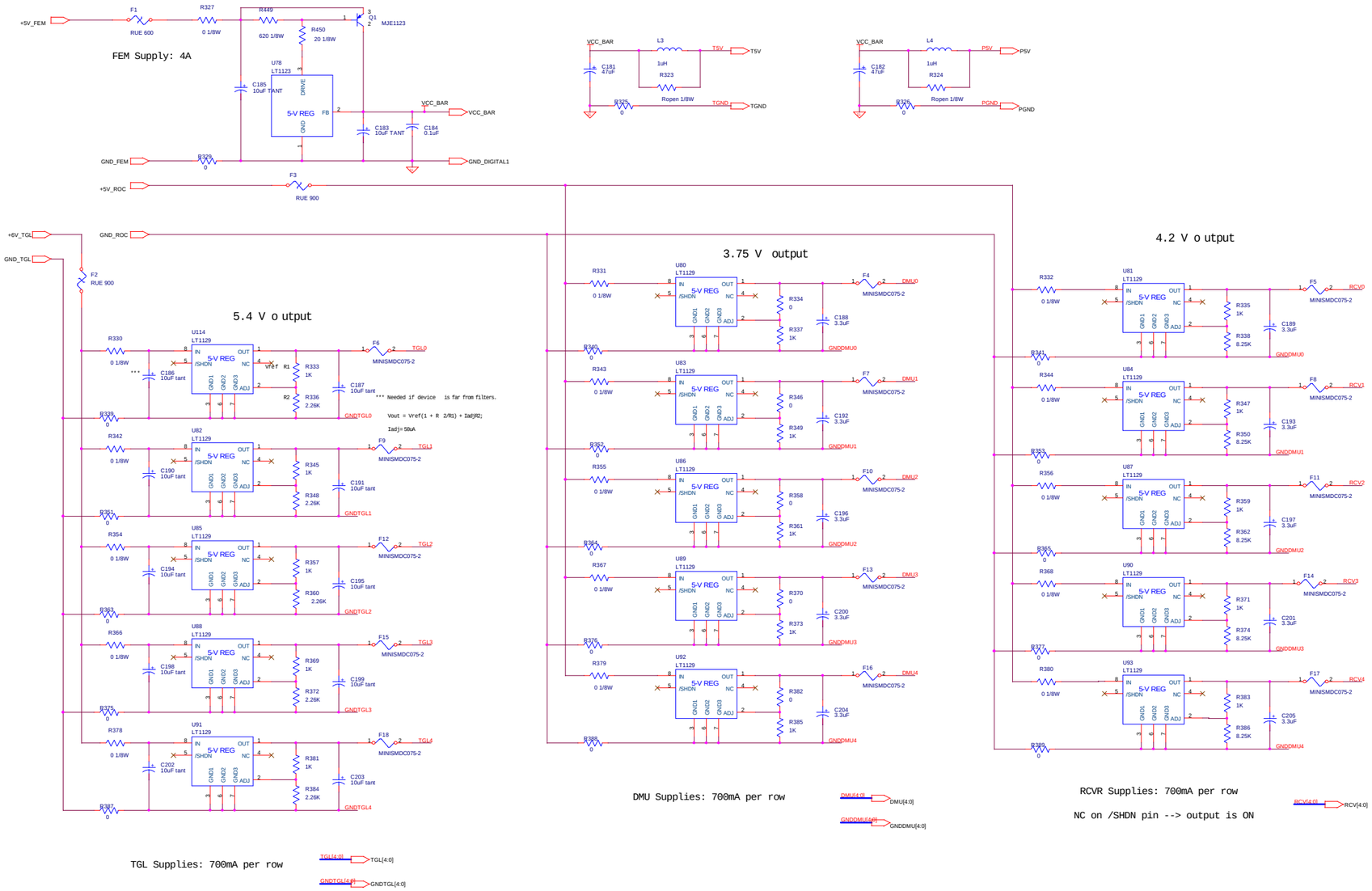
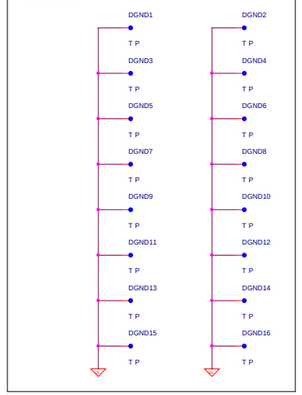
APPROVALS



GROUND TES T POINTS

NOTE: SPREAD E VENLY AROUND BOARD



Vout = 3.75 (1+R1/ R2) + 150nA * R1

PRINTED CIRCUIT BOARD	SKF-9 70-2 R1
REFERENCE DRAWINGS	NUMBER

LOCKHEED MARTIN ENERGY RESEARCH CORP.

ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee

PADS POWER SCHEMATIC

PHENIX

FILE DATE	FILE POINT	BLDG	SHT.	OF	TYPE
	HC-1 EC-1	3500	4	5	SD

SCALE	ID		REV
NTS	I & C	SKF-9 70-1	1

TOLERA NCES UNLESS OTHERWI SE SPECIFIED
FRACT IONS
XX DEC IMALS
XXX DEC IMALS
ANGLES
BREAK SHA RP EDGES MAX.
FINI SH RMS

DRAWN BY
DRAWING CHECK
ENGIN EER M. C. SM ITH 1/9/9
APPRO VED
DRAWING A PPROVALS DATE

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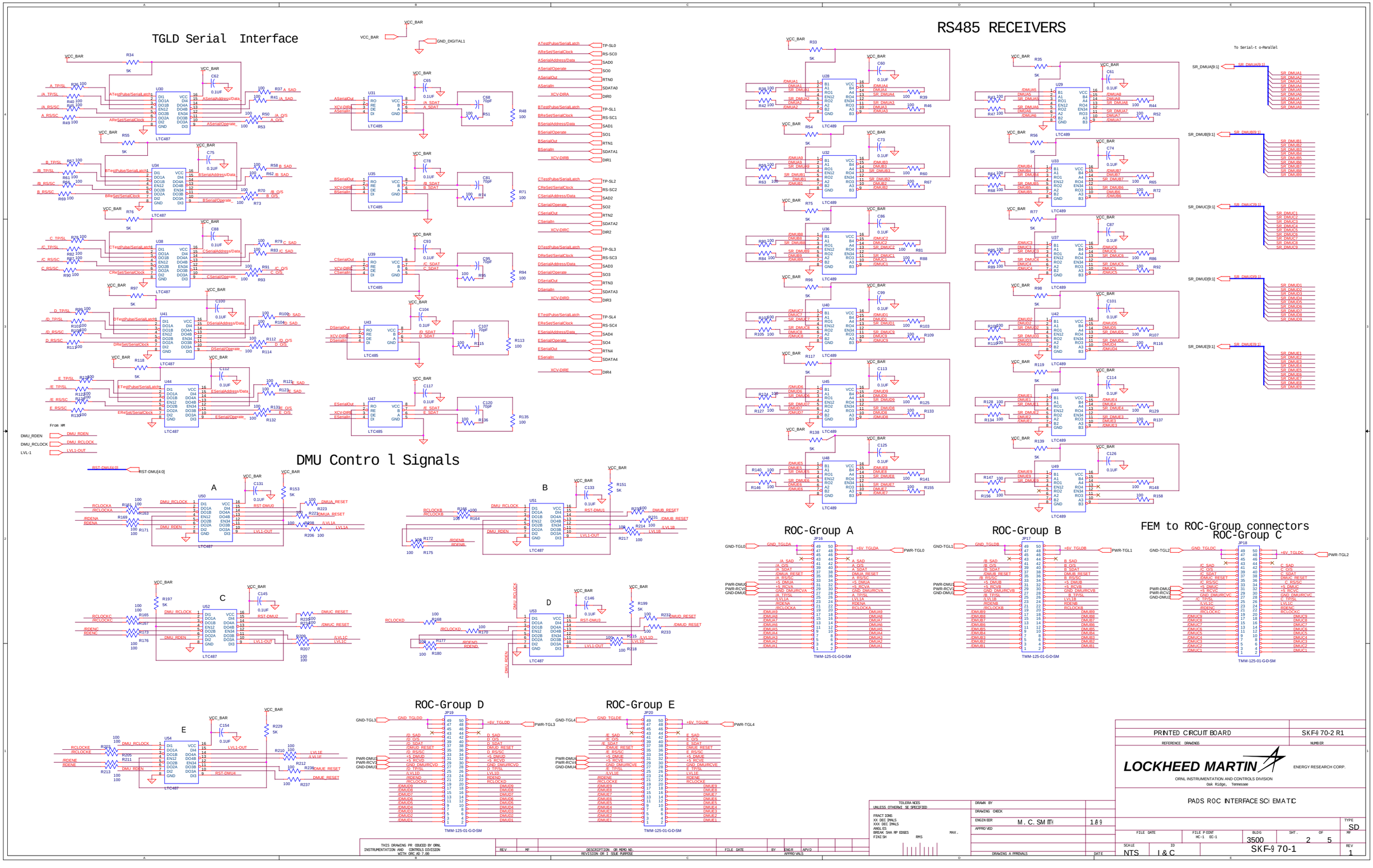
REV	MF	DESCRIPTION OR MEMO NO. REVISION OR I SSUE PURPOSE	FILE DATE	BY	ENGR	APPVD

APPROVALS


TGLD Serial Interface
RS485 RECEIVERS
DMU Contro l Signals
ROC-Group A
ROC-Group B
FEM to ROC-Group connectors
ROC-Group C
ROC-Group D
ROC-Group E
PRINTED CIRCUIT BOARD
SKF-9 70-2 R1
LOCKHEED MARTIN
ENERGY RESEARCH CORP.
ORNL INSTRUMENTATION AND CONTROLS DIVISION
Oak Ridge, Tennessee
PADS ROC INTERFACE SCHEMATIC
SKF-9 70-1
M. C. SMITH