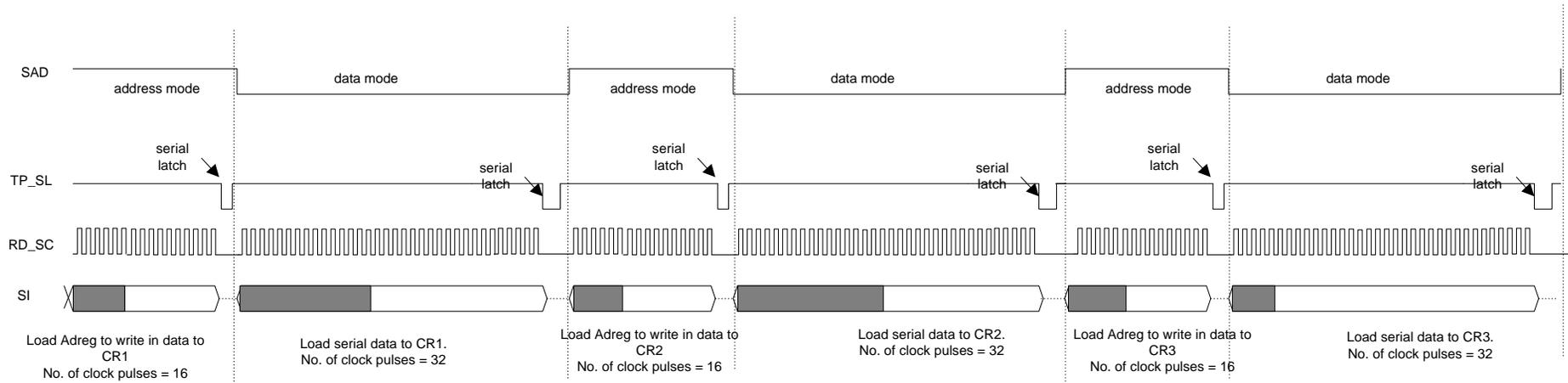


TIMING DIAGRAM FOR SERIAL DATA LOAD INTO ALL 3 REGISTERS OF A TGLD CHIP



TIMING DIAGRAM FOR SERIAL DATA READ OUT FROM ALL 3 REGISTERS OF A TGLD CHIP

