

TGLD SERIAL DATA BITS

TGLD SERIAL ADDRESS REGISTER

msb													lsb
R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0				
R1	Register address MSB; 00=no register, 01=CR1, 10=CR2, 11=CR3												
R0	Register address LSB; 00=no register, 01=CR1, 10=CR2, 11=CR3												
A6	TGLD Address BROADCAST bit												
A5	MSB TGLD Address bit												
A4	5SB TGLD Address bit												
A3	4SB TGLD Address bit												
A2	3SB TGLD Address bit												
A1	2SB TGLD Address bit												
A0	LSB TGLD Address bit												

CR1: TEST PATTERN CONTROL REGISTER

msb																lsb
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	
T1	0=disable test pulse, 1 = enable test pulse, channel 1															
T2	0=disable test pulse, 1 = enable test pulse, channel 2															
T3	0=disable test pulse, 1 = enable test pulse, channel 3															
T4	0=disable test pulse, 1 = enable test pulse, channel 4															
T5	0=disable test pulse, 1 = enable test pulse, channel 5															
T6	0=disable test pulse, 1 = enable test pulse, channel 6															
T7	0=disable test pulse, 1 = enable test pulse, channel 7															
T8	0=disable test pulse, 1 = enable test pulse, channel 8															
T9	0=disable test pulse, 1 = enable test pulse, channel 9															
T10	0=disable test pulse, 1 = enable test pulse, channel 10															
T11	0=disable test pulse, 1 = enable test pulse, channel 11															
T12	0=disable test pulse, 1 = enable test pulse, channel 12															
T13	0=disable test pulse, 1 = enable test pulse, channel 13															
T14	0=disable test pulse, 1 = enable test pulse, channel 14															
T15	0=disable test pulse, 1 = enable test pulse, channel 15															
T16	0=disable test pulse, 1 = enable test pulse, channel 16															

CR2: ATTENUATOR, DISCRIMINATOR, THRESHOLD, TEST AMPLITUDE CONTROL REGISTER

msb																lsb
At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1		
At2	MSB, C-R attenuator; 00=no atten, 01=1/3 atten, 10=1/9 atten															
At1	LSB, C-R attenuator; 00=no atten, 01=1/3 atten, 10=1/9 atten															
Vt6	MSB Discriminator voltage threshold DAC input; 111111 = min threshold															
Vt5	5SB Discriminator voltage threshold DAC input															
Vt4	4SB Discriminator voltage threshold DAC input															
Vt3	3SB Discriminator voltage threshold DAC input															
Vt2	2SB Discriminator voltage threshold DAC input															
Vt1	LSB Discriminator voltage threshold DAC input															
Ta7	MSB Test Pulse Amplitude DAC input; 111111 = 127 fC															
Ta6	6SB Test Pulse Amplitude DAC input															
Ta5	5SB Test Pulse Amplitude DAC input															
Ta4	4SB Test Pulse Amplitude DAC input															
Ta3	3SB Test Pulse Amplitude DAC input															
Ta2	2SB Test Pulse Amplitude DAC input															
Ta1	LSB Test Pulse Amplitude DAC input															

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER

msb																														lsb
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	S6	S5	S4	S3	S2	S1				
D16	MSB, channel 16, 0=enable, 1 = disable																													
D15 - D2	15SB - 2SB, channel15 - channel 2, 0=enable, 1 = disable																													
D1	LSB, channel 1																													
M5	MUX enable/disable bit, 0=enable, 1=disable																													
M4	MSB, mux address; 1111 = channel 16 select																													
M3	3SB, mux address																													
M2	2SB, mux address																													
M1	LSB, mux address; 0000 = channel 1 select																													
S6	MSB, preamp decay slope DAC, 11111 = no decay																													
S5	5SB, preamp decay slope DAC																													
S4	4SB, preamp decay slope DAC																													
S3	3SB, preamp decay slope DAC																													
S2	2SB, preamp decay slope DAC																													
S1	LSB, preamp decay slope DAC																													