EXAMPLE SERIAL DATA INPUT FOR LOADING ALL THREE REGISTERS OF A TGLD CHIP ON A ROC

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	1	0	1

CR1: TEST PATTERN CONTROL REGISTER (msb → lsb)

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	1	0	1

CR2: ATTEN., THRESHOLD, TEST AMP. CONTROL REGISTER (msb → lsb)

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	0	0	0	0	0	0	0	0	1	0	0	0

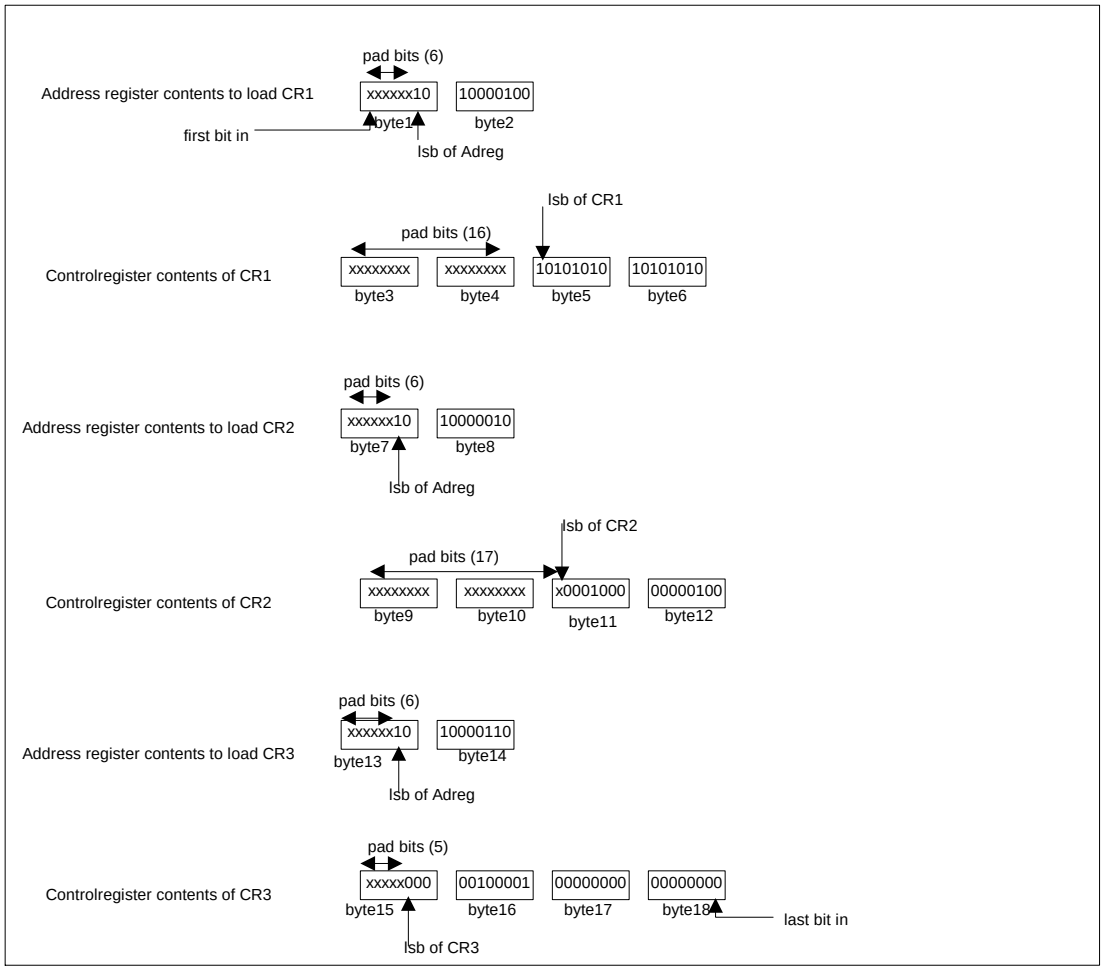
TGLD SERIAL ADDRESS REGISTER (msb → lsb)

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	1	0	1

CR3: CHANNEL DISABLE, MUX AND DECAY SLOPE COMPENSATION CONTROL REGISTER (msb → lsb)

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	S6	S5	S4	S3	S2	S1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0

ROC1, TGLD1 DATA FOR CR1, CR2 AND CR3 WITH PADDING BITS



SERIAL STRING DATA FOR LOADING REGISTERS CR1, CR2 AND CR3 CONSECUTIVELY FOR TGLD1 IN ROC1 IS:

XXXXXX10 10000100 XXXXXXXX XXXXXXXX 10101010 10101010 XXXXXX10 10000010 XXXXXXXX XXXXXXXX X0001000 00000100 XXXXXX10 10000110 XXXXX000 00100001 00000000 00000000

FIRST BIT IN

LAST BIT IN

USHA JAGADISH
3/24/98