Pad Chambers Mode Control

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I. Introduction

The scheduler issues mode commands to the FEM each and every beam clock via the *Timing and Control G-Link*. A total of 20 bits are available for mode control, timing, and other functions. Table 1 gives the hardware definition of the Timing and Control Interface (T&C Interface) (all bits active high).

Table 1

Data Line	Function	Notes
D0	Mode Bit 0	
D1	Mode Bit 1	
D2	Mode Bit 2	
D3	Mode Bit 3	
D4	Mode Bit 4	
D5	Mode Bit 5	
D6	Mode Bit 6	
D7	Mode Bit 7	
D8	Beam Clock	9.4MHz
D9	LVL1 Accept	
D10	Mode Enable	Mode Bits valid when high
D11	EnDat1	Select odd FEM
D12	EnDat2	Select even FEM
D13	User Bit 0	
D14	User Bit 1	
D15	User Bit 2	
D16	Reserved	
D17	Reserved	
D18	Reserved	
D19	Reserved	
STRBOUT	4X Beam Clock	

II. Timing and Control Interface

The T&C Interface provides the following:

- 3 timing signals (LVL1 accept, Beam Clock and 4X Beam Clock);
- mode enable bit plus 7 mode control bits (MB[7:5] are subsystem specific, MB4 is RUN/HALT, MB[3:2] are subsystem special and MB[1:0] are reserved);
- 2 FEM select bits (EnDat[2:1]);
- 3 User Bits
- and 4 reserved bits.

The mode bits are output each beam clock cycle and are decoded to implement a specific command set. Each mode command is sampled by the FEM on the rising edge of the Beam Clock and implemented on the following rising edge (or 1 Beam Clock period later).

III. Command Summary

A set of common commands is listed below. These commands are for normal operations, diagnostics, monitoring, and calibration support. (For more information refer to *Phenix Mode Control* by M. Nance Ericson, Bob Petersen and James W. Walker).

A. Run

Run provides the means to start and continue acquisition. This pertains to all FEM functions including FEE control, packet forming and data transmission to the DCM.

B. Halt

Halt is used to stop all FEM functions including FEE control, packet forming and data transmission to the DCM. Halt provides a static state for serial operations associated with FEM and/or FEE configuration, monitoring and diagnostics.

C. Initialization Reset (Init. Reset)

Init. Reset is used to place the FEM in an initialized state. All data, counters, etc. are reset but the configuration information is retained. LVL-1 qualified data and associated packets that have not been completely sent to the DCMs are lost. This reset will be used at powerup and for complete re-initialization of the FEM (in the event of a synchronization error, etc.)

D. Resync Reset

Resync Reset is used for the *sole purpose* of synchronously resetting the event counter in all FEMs which will resynchronize all beam clock counters across the detector. The actual reset function will be performed on the next valid LVL1 trigger to ensure this reset does not affect the processing of valid LVL1 events by the FEM.

E. Special Reset

Special Reset provides a subsystem-customized reset operation. This function may require multiple beam clock cycles for execution. *For this and other commands requiring more than one beam clock cycle for execution, the scheduler should output the command the appropriate number of beam clock cycles*.

All FEMs will powerup in the Halt state. Careful design of the FEM is required so that all FEM functions start gracefully and predictably.

IV. Mode Bit Definitions

In defining the mode bit definitions there is some standardization of the command set across all subsystem types while allowing flexibility of commands for subsystem-specific functions. The FEM operational state must be completely deterministic - the functional

state can be completely determined by observing the mode bits for any given beam clock; therefore, requires no knowledge of prior states.

The lower 5 mode bits are split into 3 groups, each defining a part of the operational state. MB4 is the Run/Halt Bit and defines the run status of the FEM (1=Run, 0=Halt). MB1 and MB0 control the *reset group* of commands shown in Table 2. MB3 and MB2 control the *custom group* shown in Table 3. MB7, MB6 and MB5 control the *mask* which is applied to each of the *custom group* commands. The mask sets are shown in Table 4. Each group must have a no-operation command to allow for continuous Run/Halt operations with no other functions specified.

Table 2 Reset Group MB1 and MB0

MB1	MB0	Command
0	0	No-op
0	1	Resync Reset
1	0	Init. Reset
1	1	TGLD Reset

Table 3 Custom Group MB3 and MB2

MB3	MB2	Command
0	0	No-op
0	1	Test Pulse (Must include TGLD reset)
1	0	DMU Reset
1	1	Both Reset

Table 4 Mask Sets MB7, MB6 and MB5

MB7	MB6	MB5	Command
0	0	0	No-op
0	0	1	Row A
0	1	0	Row B
0	1	1	Row C
1	0	0	Row D
1	0	1	Row E
1	1	0	*undefined*
1	1	1	Global

Being deterministic allows a mode command structure where each command group can produce an operation regardless of what operation in specified in the other groups. This allows for multiple functions to be specified at once. For instance, a Run can be specified with both a Special Reset and a Custom Group command. This makes the mode bits powerful but also allows for commands that may be incompatible if issued

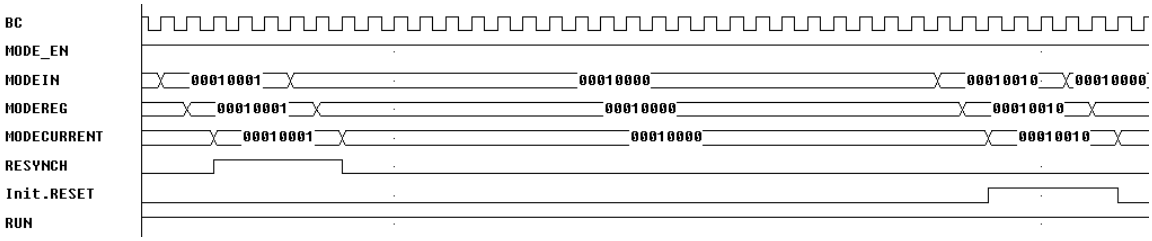
simultaneously. FEMs are designed to handle invalid command sets by defaulting to a Run with no-ops for each of the other command groups. It is safe to assume that error conditions (incompatible or undefined group commands) will be removed from the possible command list during system checkout and initial operation.

V. Examples

The following examples demonstrate how to schedule mode commands based on the valid commands given in Table 5 of the appendix. Note: All other commands will default to the *RUN with no options* mode.

A. Reset FEM

There are two types of reset for the FEM: Resync and Init. The Resync command given by MB[7:0]=00010001 will reset the counters and resynchronize the FEM with the beam clock as shown in Figure 1a. The Init. command given by MB[7:0]=00010010 will reset



all functions at the FEM as shown in Figure 1b. This reset is much like a power-up reset.

Figure 1 FEM Resets

B. Reset TGLD

When resetting the TGLD we must also define the row mask set by MB[7:5]. There is a mask for each row as well as a global mask (Table 5). For a global reset, the mode bit command is MB[7:0]=11110011. This mode command must be issued for a minimum of 10 contiguous beam clocks (or >1µsec) for proper reset of the TGLD (Figure 2).

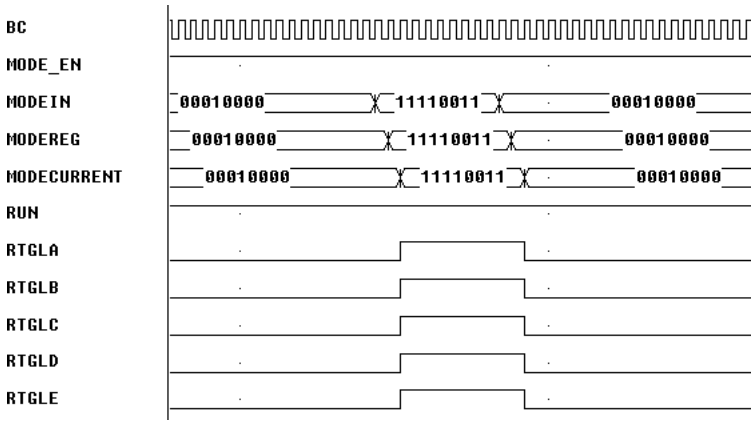
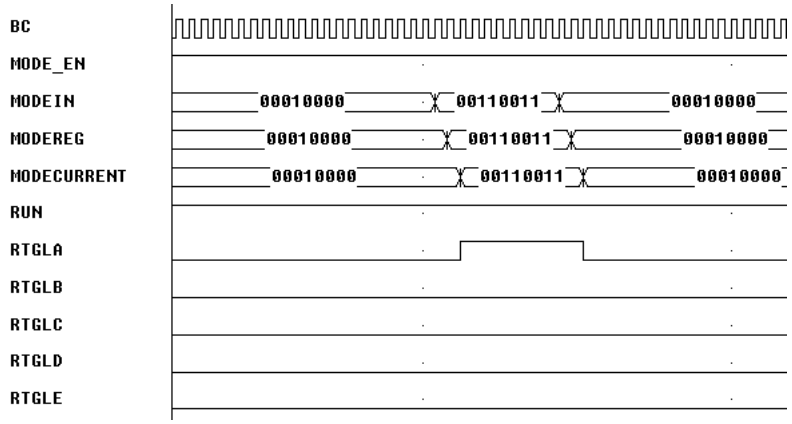


Figure 2 Global TGLD Reset

To reset the TGLDs on row A, for example, the mode bit command is

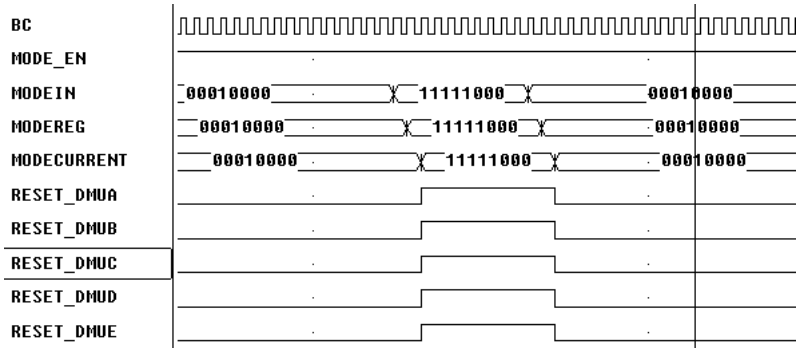


MB[7:0]=00110011. Again, this mode command must be issued for a minimum of 10 contiguous beam clocks (or >1µsec) for proper reset of the TGLD (Figure 3).

Figure 3 Row A TGLD Reset

C. Reset DMU

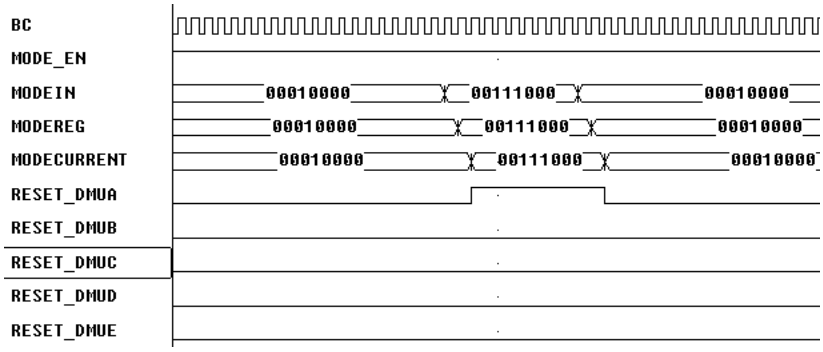
When resetting the DMU we must also define the row mask set by MB[7:5]. Like the TGLD, there is a mask for each row as well as a global mask (Table 5). For a global reset, the mode bit command is MB[7:0]=11111000. This mode command must be issued for a minimum of 2 contiguous beam clocks (or > 0.23µsec) for proper reset of the



DMU (Figure 4).

Figure 4 Global DMU Reset

To reset the DMUs on row A, for example, the mode bit command is



MB[7:0]=00111000. Again, this mode command must be issued for a minimum of 2 contiguous beam clocks (or > 0.23µsec) for proper reset of the DMU (Figure 5).

Figure 5 Row A DMU Reset

D. Reset Both TGLD and DMU

When resetting both the TGLDs and DMUs, again, we must define the row mask set by bits MB[7:5]. There is a mask for each row as well as a global mask (Table 5). For a global reset, the mode bit command is MB[7:0]=11111100. This mode command must be issued for a minimum of 10 contiguous beam clocks (or >1µsec) for proper reset of the TGLD (Figure 6).

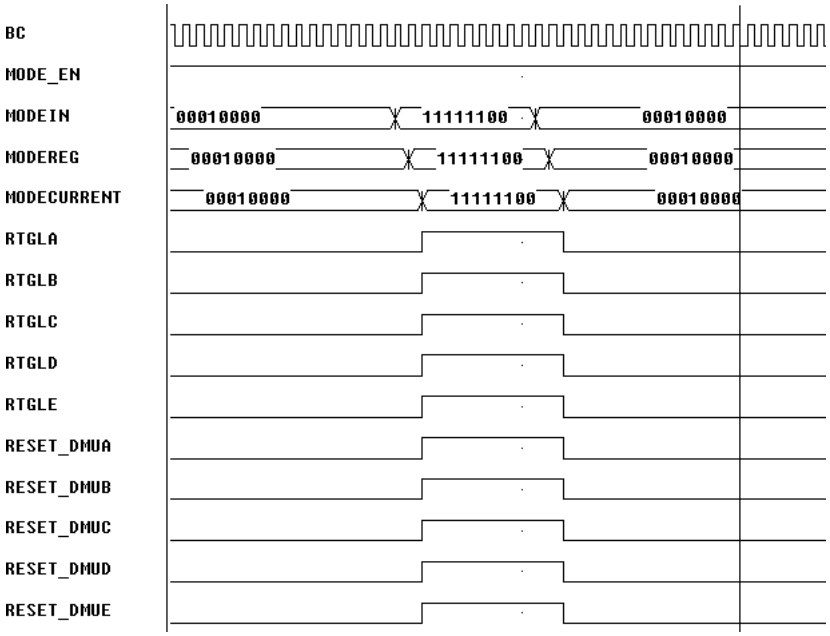
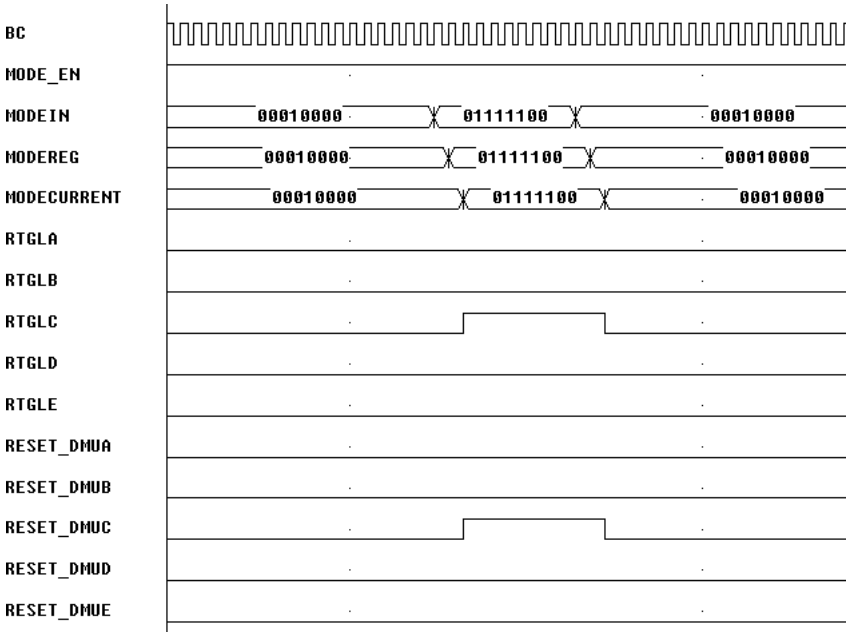


Figure 6 Global Reset Both TGLD and DMU

To reset both the TGLDs and DMUs on row C, for example, the mode bit command is



MB[7:0]=01111100. Again, this mode command must be issued for a minimum of 10 contiguous beam clocks (or >1µsec) for proper reset of the TGLD (Figure 7).

Figure 7 Reset Row C Both TGLD and DMU

E. Test Pulse TGLD

When issuing a test pulse command to the TGLD, we must first issue a reset, then start the test pulse command before releasing the reset as shown in Figure 8. Again, for all commands related to the TGLD, we must also define the row mask set by MB[7:5]. For a global test pulse, the first mode bit command is MB[7:0]=11110011 or a global TGLD reset. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec) for proper setup of the TGLD. The second mode command, MB[7:0}=11110111 will start the test pulse. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec). The third mode command, MB[7:0}=11110100 will release the reset. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec). The fourth and final mode command, MB[7:0}=00010000 will release the test pulse and place the chamber in *RUN* mode. This set of mode commands is demonstrated in Figure 9.

Figure 8 General Timing of Test Pulse

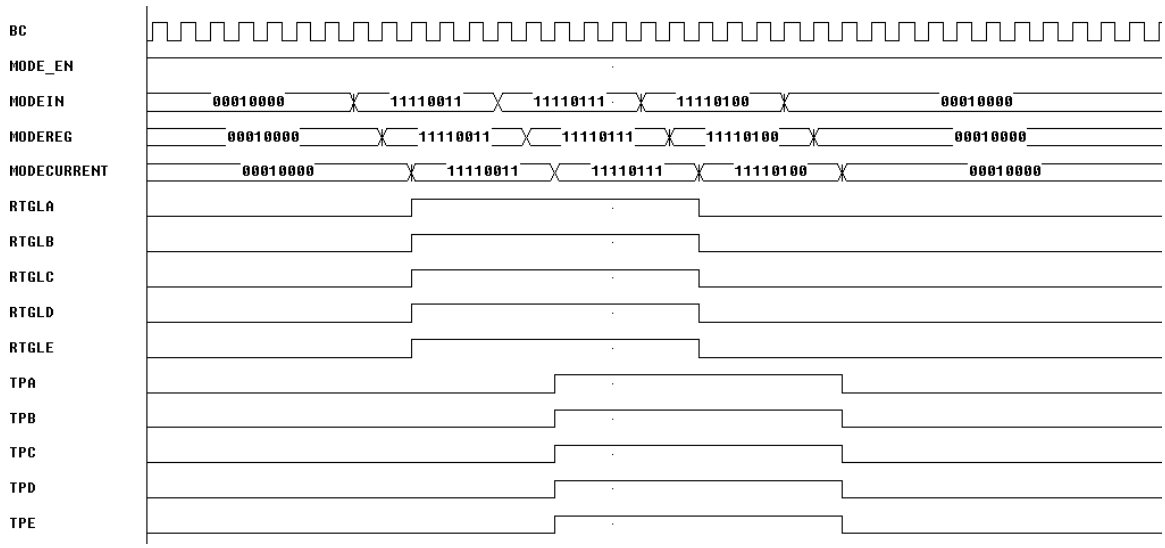


Figure 9 Global Test Pulse

For a test pulse on row D, the first mode bit command is MB[7:0]=10010011 or a row B TGLD reset. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec) for proper setup of the TGLD. The second mode command, MB[7:0}=10010111 will start the test pulse. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec). The third mode command, MB[7:0}=10010100 will release the reset. This mode command must be issued for a minimum of 5 contiguous beam clocks (or >500nsec). The fourth and final mode command, MB[7:0}=00010000 will release the test pulse and place the chamber in *RUN* mode. This set of mode commands is demonstrated in Figure 10.

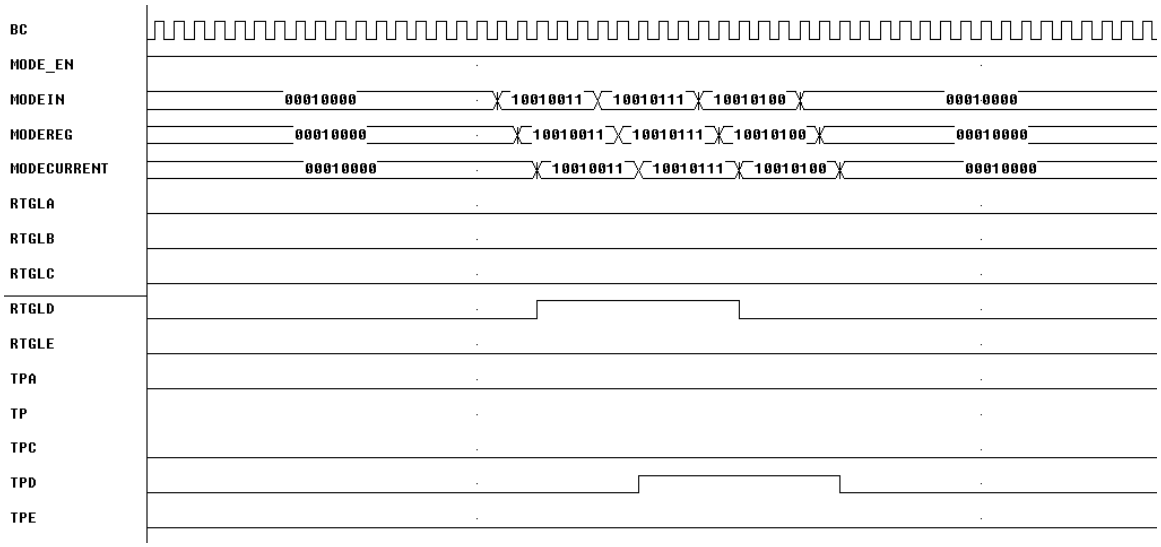


Figure 10 Row D Test Pulse

VI. Appendix

Table 5 Valid Mode Commands

MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0	Command
X	X	X	0	X	X	X	X	HALT
0	0	0	1	0	0	0	0	RUN
0	0	0	1	0	0	0	1	Resync Reset
0	0	0	1	0	0	1	0	Init. Reset
0	0	1	1	0	0	1	1	Reset Row A TGLD
0	1	0	1	0	0	1	1	Reset Row B TGLD
0	1	1	1	0	0	1	1	Reset Row C TGLD
1	0	0	1	0	0	1	1	Reset Row D TGLD
1	0	1	1	0	0	1	1	Reset Row E TGLD
1	1	1	1	0	0	1	1	Reset Global TGLD
0	0	1	1	1	0	0	0	Reset Row A DMU
0	1	0	1	1	0	0	0	Reset Row B DMU
0	1	1	1	1	0	0	0	Reset Row C DMU
1	0	0	1	1	0	0	0	Reset Row D DMU
1	0	1	1	1	0	0	0	Reset Row E DMU
1	1	1	1	1	0	0	0	Reset Global DMU
0	0	1	1	1	1	0	0	Reset Row A Both TGLD & DMU
0	1	0	1	1	1	0	0	Reset Row B Both TGLD & DMU
0	1	1	1	1	1	0	0	Reset Row C Both TGLD & DMU
1	0	0	1	1	1	0	0	Reset Row D Both TGLD & DMU
1	0	1	1	1	1	0	0	Reset Row E Both TGLD & DMU
1	1	1	1	1	1	0	0	Reset Global Both TGLD & DMU
0	0	1	1	0	1	0	0	Test Pulse Row A TGLD*
0	1	0	1	0	1	0	0	Test Pulse Row B TGLD*
0	1	1	1	0	1	0	0	Test Pulse Row C TGLD*
1	0	0	1	0	1	0	0	Test Pulse Row D TGLD*
1	0	1	1	0	1	0	0	Test Pulse Row E TGLD*
1	1	1	1	0	1	0	0	Test Pulse Global TGLD*

* Requires coordination with Reset TGLD. See discussion in section V. Examples.