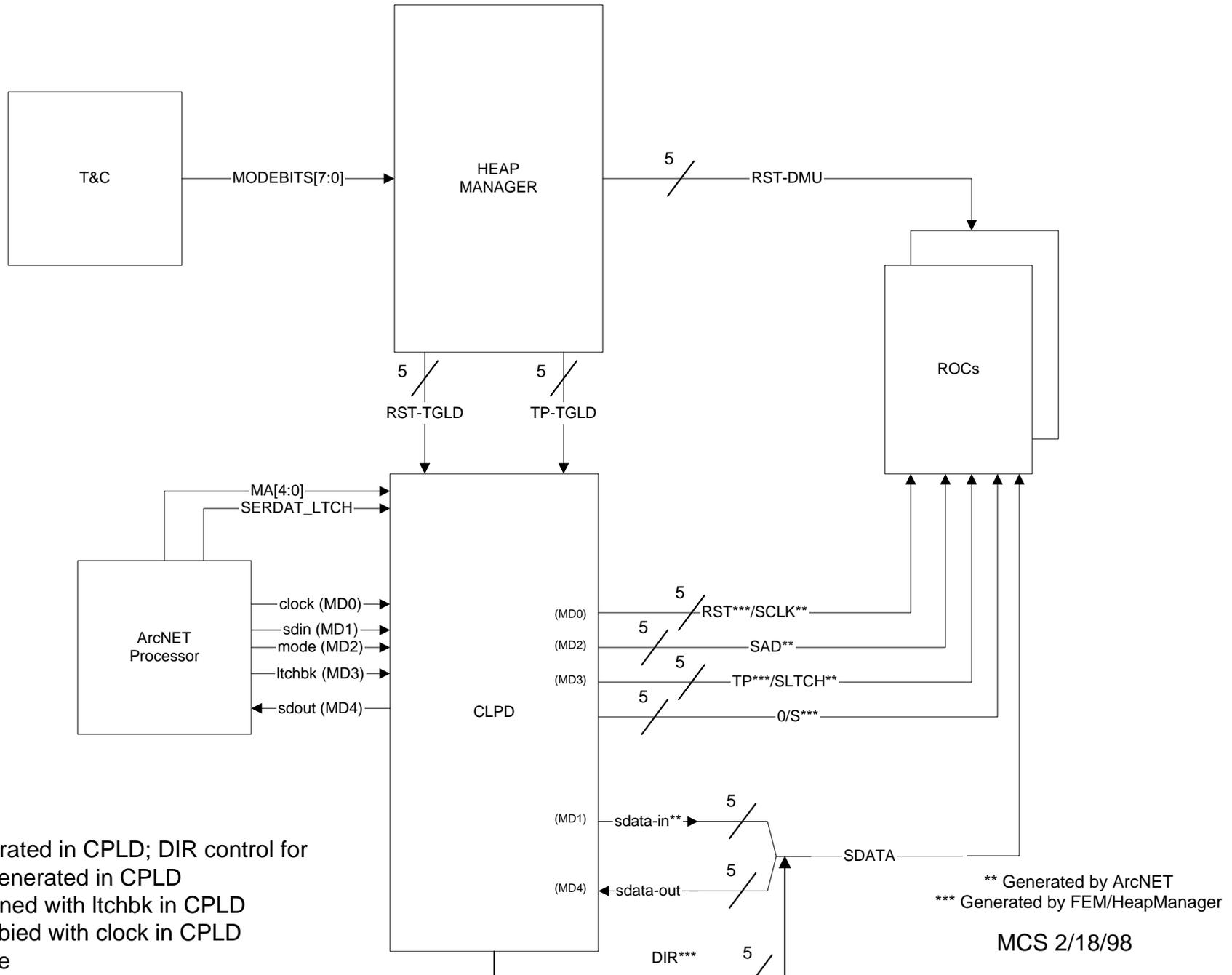


# ROC Interface and Control



1. O/S is generated in CPLD; DIR control for Xceiver also generated in CPLD
2. TP is combined with ltchbk in CPLD
3. RST is combined with clock in CPLD
4. SAD = mode