A Front-End Electronics Module for the PHENIX Pad Chamber[1]

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Abstract

A front-end electronics module (FEM) has been developed for the PHENIX Pad Chamber. The module's control functions are performed by the heap manager unit, an FPGA-based circuit on the FEM. Each FEM processes 2160 channels of front-end electronics (FEE). Data readout and formatting are performed by an additional FPGA-based circuit on the FEM. Three external systems provide initialization, timing, and data information via serial interfaces. This paper discusses the application of the heap manager, data formatter, and serial interfaces to meet the specific control and data readout needs of the Pad Chamber Subsystem. Unit functions, interfaces, timing, data format, and communication rates will be discussed. In addition, subsystem issues regarding mode control, serial architecture and functions, error handling and FPGA implementation and programming will be presented.

I. INTRODUCTION

The Pad Chamber (PC), part of the Tracking System of the PHENIX detector at the RHIC accelerator of Brookhaven National Laboratory, is composed of three layers of pixel detectors (PC-1, PC-2, and PC-3) comprising ~207,360 channels. The main functions of the PC are to provide track information to reduce track matching ambiguities, to provide azimuthal tracking information, to help separate neutral EMCAL showers from charged tracks, and to help veto converted photons. The PC system is divided into two arms. The East Arm is composed of eight sectors of PC-1 and 4 sectors of PC-3. The West Arm is composed of eight sectors of PC-1 and 4 sectors each of PC-2 and PC-3. The system electronics are partitioned into groups of 2160 channels supported by a FEM. Each group contains, forty-five read-out cards (ROC) which process signals from 48 detector channels using two custom ICs developed for PHENIX. The TGL [1], is a sixteen channel analog discriminator (three per ROC) and the DMU is a five-event, forty-eight channel Digital Memory Unit.

Each FEM has a programmable readout and control module (called a heap manager) that provides control signals to the front-end electronics, collects and transmits data, and manages the command interface (timing and control). DMU readout and serial to parallel data conversion are performed by a second programmable unit on the FEM. Additionally, slow serial data and control is performed by an embedded controller and supporting hardware. Figure 1 shows the generalized architecture and the data flow path associated with the PC FEM and interfaces.

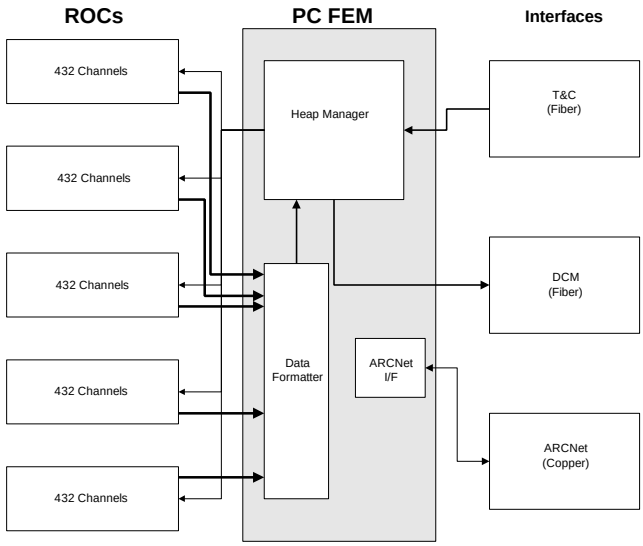

Figure 1 PC System Electronics Diagram.

Each FEM receives system clocks and mode control signals directly from PHENIX Timing and Control (T&C) via Glink fiber at 37.6 MHz or fours times the beam clock. DMU data is received in serial format by the data formatter where it is converted into twenty-bit words for transmission by the heap manager over Glink fiber at twice the beam clock to the higher level data collection system (Data Collection Modules or DCM). The initial PHENIX detector configuration, specifies that two FEMs will share one data collection fiber. This configuration requires FEM to FEM data communication. System FPGA programming and setup are performed via ARCNet interface which consists of a embedded controller and a multiplexer implemented in a re-programmable CPLD.

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II. HEAP MANAGER

In PC, a FEM is mounted at each end of a pixel motherboard. Each FEM processes data from ROCs on the nearest half of the motherboard, 2160 channels. The heap manager performs the following generalized functions: mode interpretation and execution, FEE timing and control, Level-1 (LVL-1) buffering of FEE data, and collection control, packet forming, and communication of LVL-1 qualified data. Figure 2 shows the basic functional blocks of the heap manager. This unit was developed with guidance from a previously designed generic Type I heap manager [2].

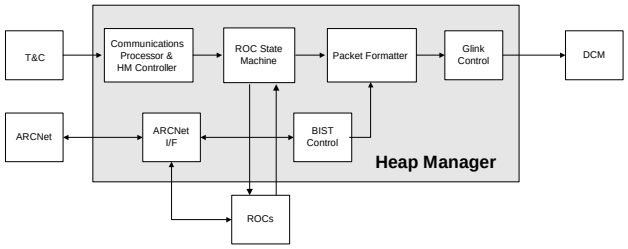

Figure 2 PC Heap Manager Block Diagram.

Mode bits are used to control the operational state of the FEM. The communications processor interprets and distributes control signals to the rest of the FEM and ROCs based on the mode bit commands that are issued each beam clock. A ROC state machine controls the DMU data readout. Data is collected from the DMU serially, and converted to twenty-bit parallel words in the data formatter. This data is formatted into a packet by the heap manager and transmitted via Glink fiber to the DCM.

As shown in Figure 2, three interfaces are associated with each FEM: T&C, DCM, and ARCNet. The T&C interface provides the system clocks, mode control bits, and LVL-1 accept signals - all synchronized to the beam clock. The DCM interface provides a high-speed link for data retrieval from the FEM. The ARCNet interface is a slow serial port for programming FPGAs, sending control information to the heap manager and TGLs, and resetting Glinks.

FEMs function synchronously and asynchronously with the beam clock. DMU controls are synchronized with each beam clock while data packet formation is LVL-1 accept driven. Data transmission from the FEM takes place at twice the beam clock. The FEM is designed to store five qualified event data packets simultaneously. This event storage is accomplished by the five deep event storage in the DMU and sufficiently deep FIFOs on the FEM to buffer data before transmission to the DCM via Glink fiber. Valid events may occur at an average rate not to exceed 25 kHz which allows up to 40 μs for data collection, formatting, and transmission to DCM without creating a data readout bottleneck.

III. DATA FORMATTER

The data formatter receives serial data from forty-five ROCs, converts the serial data into 20-bit parallel words, and checks data and event number parity. Each ROC serial stream is 52-bits in length (48 data bits, 3 event number bits, and a parity bit). The event number is received first (most significant bit, MSB, first) and the event numbers for each of the nine ROCs on the row are compared. If one event number out of the nine does not correlate, an error bit is set. Consequently, five event number parity bits are generated (one for each row), which is placed in the user words. Following the event number bits are the 48 data bits, again MSB first. Finally, the parity bit is checked against the parity of the data bits received. The result of the parity check, one bit per ROC, is also placed in the user words.

Serial data from the ROCs is formed into parallel words by shifting the data into 4-bit registers and storing into RAM internal to the data formatter FPGA. Addressing for the RAM is constructed such that it acts as a FIFO cell. Nine of these cells are used to store the nine segments of the data as shown in Figure 3. The data is then read out by the heap manager during formation of the data packet for transmission to the DCM.

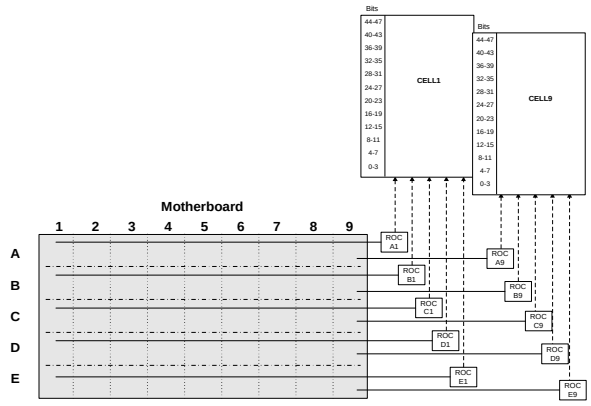

Figure 3 Mapping of data from ROCs.

The data and control interface between the FEM and the ROCs is standard RS-485 protocol. To minimize the number of lines in the interface, some of the TGL signals are shared, having one function during slow serial communication and a different function during operational mode. Figure 4 shows the interface between the heap manager, data formatter, and the ROCs. During a slow serial operation, the ARCNet processor provides the SDATA, SCLK, SAD and SLTCH signals. The O/S, or operate/serial signal, is derived based on the address (MA[4:0]) from the ARCNet processor. Conversely, during the operate mode, T&C provides the RST and TP signals via mode bits to the heap manager communications processor. This information is then passed to the ROCs via the CPLD interface.

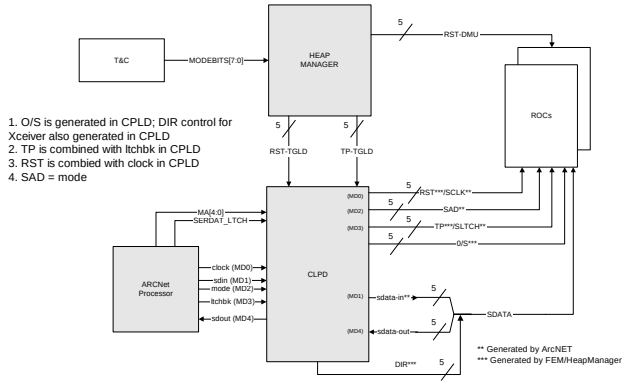

Figure 4 ROC Interface and Control

IV. Timing and Control Interface

The primary function of the T&C Interface is to receive the fast timing signals and mode control and distribute this information to the remainder of the FEM and ROCs. Included in the information are the system clocks, LVL-1-accept, mode control bits, and ARCNet reset.

The Glink receiver function is implemented using the transmitter half of an HP HFBR-5315 optical transceiver and an HP HDMP-1024 giga-bit receiver IC. The timing and mode control signals are received by the heap manager where they are decoded and transmitted to the ROCs. Each row of ROCs receives a copy of the beam clock, LVL-1 (which can be delayed internal to the heap manager), and a reset signal which is decoded from the mode bits. The signal interface between the heap manager and ROCs is RS-485.

V. Data Collection Interface

On every LVL-1 accepted event, the heap manager forms a data packet for transmission to the DCM. This data packet contains the detector ID (coded into the FPGA), the module address (set by jumper on the PCB), header and trailer words, 108 data words, 8 user words, and longitudinal parity. Formatted data packets, consisting of 20-bit words are transmitted to the DCMs via a Glink interface at twice the beam clock. Table 1 shows the data packet format.

The Glink interface consists of an HP HDMP-1022 giga-bit transmitter IC and the transmitter portion of an HP HFBR-5315 optical transceiver.

The data words consist of the pixel information from the ROCs, grouped into nine segments of twelve words. Figure 3 shows how these segments are constructed by the data formatter. The user words communicate error conditions to the DCM. The first two words and five least significant bits of the third word contain data parity errors. The five most significant bits of the third word contain event number parity errors, one bit for each row.

At initial installation of the PHENIX detector, the FEM to DCM ratio will be two, changing to one as the remaining group of DCMs are installed at a future date. Operation in either mode (ratios of 2:1 and 1:1) is accomplished using the reprogrammability of the FPGAs and two channel enable bits ENDAT[1:0] available from T&C. These bits indicate which of the two multiplexed channels (odd or even) transmit data over the shared Glink channel. Each FEM is hardwired on the PCB as either even or odd when installed on the chamber. The heap manager handles this function.

Table 1
PC Data Packet Format.

Word Number	Word Format
1	Header – 20-bits “ON”
2	Detector ID
3	Event Number
4	Module Address
5	Flag Word – 20 bits “OFF”
6	Beam Clock Count
7	First data word of MEM1
. . .	. . .
114	Last Data Word of MEM9
115	First User Word
. . .	. . .
122	Last User Word
123`	Longitudinal Parity
124	Trailer – 20-bits “OFF”

VI. ARCNet Interface

The ARCNet interface provides slow serial access to the PC electronics from the high level control of PHENIX. Its functions include programming of the FPGAs after a cold start or hard system reset, loading of the ROC/TGL control bits (channel enables, D/A settings, calibration enables, multiplexer controls), resetting the Glink interfaces, and controlling the heap manager self-test function. Readback capability exits at every level allowing readback of FPGA ‘done’ condition, Glink synchronization status, and complete readback of heap manager and ROC/TGL programmable parameters.

Each FEM has one ARCNet node which is based on the Standard Microsystems Corporation (SMC) COM20051 Integrated Microcontroller and ARCNet Interface (an Intel 8051-based microcontroller with built-in ARCNet UART). The controller is configured to provide thirteen input/output lines that are used for control and multiplexer functions associated with the node.

The multiplexer is implemented in a Xilinx XC95108 CPLD. This allows the microcontroller to use five bits to address the different serial functions and leaves six bits for I/O. Each read and write function requires a separate address and each row of ROCs is treated separately.

VII. System Initialization

The FEM requires specific initialization procedures to assure proper operation. Resultantly, there is capability for polling the FPGA ‘done’ bits and each Glink interface can be

reset to assure proper synchronization. These functions are performed via ARCNet.

FPGA programming is required upon power up and following a hard system reset. Programming is accomplished by sending a stream of configuration bits via ARCNet interface and polling the 'done' bit at conclusion of data stream.

Glink synchronization is required upon power up and following a Glink reset operation. Synchronizing the link between transmitter and receiver is accomplished by holding the ED (enable data) pin low after a reset as shown in Figure 5. Fill frames are sent until the receiver is locked onto the transmitter as indicated by the STAT0 signal.

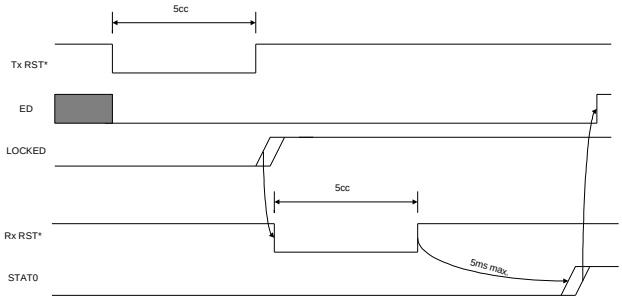

Figure 5 Glink Synchronization (cc = clock cycles)

VIII. Implementation

In-system reprogrammability is a primary objective of the PHENIX experiment design, and facilitates changes that are anticipated in the early test development stages of PHENIX. To accommodate this goal, all applicable digital functions are implemented using field programmable gate arrays (FPGAs). Slow serial access to all configurable parts is accomplished using ARCNet, allowing limited functional reprogrammability across PC without physical access to the electronics. Serial to parallel conversion of the data from the ROCs and subsequent formation into the desired packet format requires significant resources. Consequently, this function is performed in an FPGA external to the heap manager. Architectural design methods and VHDL techniques were used to optimize each FPGA design for function, speed, and power. All designs allow future redesign and expansion. Also, additional lines exist between FPGAs for future expansion.

IX. Conclusions

In PC, system readout and control are implemented as modular, high-density, reprogrammable functions. Control and data readout functions are performed by the heap manager. In-circuit reprogrammability is accomplished by full use of FPGAs for all applicable digital functions. Access for FPGA programming, parameter setup, and diagnostic functions is provided using a ARCNet serial distribution network. Unit functions, interfaces, timing, data format, and communication rates were discussed. In addition, subsystem issues regarding mode control serial architecture and functions, and FPGA implementation and programming were presented.

XI. References

[1] W. L. Bryan, U. Jagadish, et al, "TGLD: A 16-Channel Charge Readout Chip for the PHENIX Pad Chamber Detector Subsystem at RHIC", *IEEE Trans. on Nucl. Sci.*, Vol. 45, No. 3, June 1998, pp. 754-757.

[2] M. N. Ericson, et al., "Development of a Front End Controller/Heap Manager for PHENIX," *IEEE Trans. on Nucl. Sci.*, Vol. 44, No.3, June 1997, pp. 312-317.