Applications Note: G-Link Design for Phenix

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I. Introduction

Efforts to assemble a test fixture to simulate the Timing and Control (T&C) and FEM to DCM links at ORNL have led to some interesting do's and don'ts associated with G-Link design. In this applications note, we will cover some of the potential pitfalls associated with the design of a G-Link transmitter (Tx) or receiver (Rx) unit.

II. Using the Appropriate Chip Set

There are two components which make up one end of a G-Link: 1) the Hewlett Packard (HP) G-Link chip (Tx or Rx) and 2) the Methode or HP optical component (Tx, Rx, or TRx). Each of the G-Link chips are available in ECL or TTL versions (see Table 1). The optical components are available in separate Tx and Rx components from Methode or as a transceiver from HP (see Table 2).

Table 1 HP G-Link Chips

	Tx	Rx
ECL (PECL)	HDMP-1012	HDMP-1014
TTL	HDMP-1024	HDMP-1024

Table 2 Optical Components

	Methode	HP
Tx	MTM-8510-1-SC-S-S	
Rx	MRM-8510-1-SC-S-S	
TRx		HFBR-5305

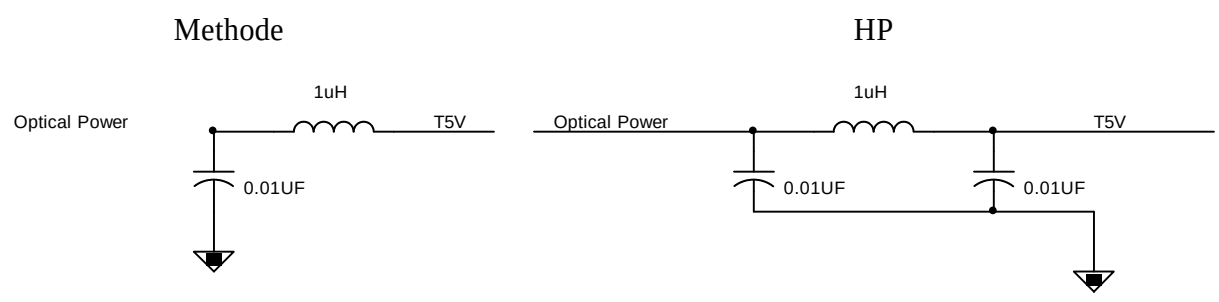
Within Phenix there are three basic types of G-Link connections: 1) T&C Link, 2) FEM to DCM Link, 3) Level 1 Trigger Link. The T&C link operates at 40 MHz and either the PECL or TTL chip set is appropriate when jitter is not a concern. If the timing jitter specifications are of concern, at this time the PECL version is recommended. Either chip set is appropriate for the FEM to DCM link that operates at 20 MHz. The EmCal and Pad Chambers subsystems must transfer DCM data between FEMs on Day 1 and thus should consider using the PECL version to avoid noise problems. Finally, the TTL chip set has not been tested for Trigger links operating at 60 MHz.

III. Avoiding General G-Link Pitfalls

1. Power Supply Filtering

Each of the optical components should be properly bypassed with capacitors and inductors as shown in Figure 1. Those subsystems affected by a magnetic field and cannot use a ferrite bead inductor will find suitable phenolic core inductors from manufactures such as Delevan.

Figure 1 Power Supply Filtering



2. G-Link to Optical Component Connections

The connection between the HP chips and the optical components are differential PECL drive. In the testing here at ORNL and also at AMES, no termination was necessary if 1) the components were placed close together, 2) traces were of equal length, and 3) impedance was controlled at 50Ω. It is critical the differential lines are connected correctly (i.e. optical Rx+ output to the Rx+ input of the HP chip and optical Rx- output to the Rx- input of the HP chip, etc.).

3. HP Chip PLL settings

The HP G-Link chips have two pins to set the locking frequency range of the internal PLL. These pins are denoted DIV1 and DIV0 in the HP data sheets. **Table 3** shows the frequency ranges for the four possible settings. The setting DIV1=0 DIV0=0 is suggested for operating frequencies of 60 MHz and 40 MHz. DIV1=0 DIV0=1 is suggested for 20 MHz operating frequency.

Table 3 G-Link Chip PLL Settings

Parallel Word Frequency (MHz)	DIV1	DIV0
35 – 62.5	0	0
18 – 42	0	1
9 –21	1	0
6.3 – 10.5	1	1

4. STRBIN Duty Cycle

Input latches on G-Link are triggered only on the positive edges of STRBIN, so STRBIN doesn't have to be tightly controlled around a 50% duty cycle. A duty cycle of 50% ± 10% is a conservative number. The setup time for data is 6ns.

Note: There is always a clock signal on STRBOUT Tx and Rx. The clock will drift up in frequency, but it will always be present. Also, with no STRBIN, the Tx will transmit FF0 throught the high-speed DOUT/DOUT* lines.

IV. Designing a Tx Unit

Table 4 below describes the connections for a G-LINK transmitter chip. In PECL designs, all lines should be properly terminated according to PECL design guidelines. Figure 2 shows the Tx timing diagram under normal operations. The appendix includes the reference designs used in the ORNL G-LINK test fixture. Figure 3 shows the necessary circuit for the PLL bypass.

Figure 2 Tx Timing

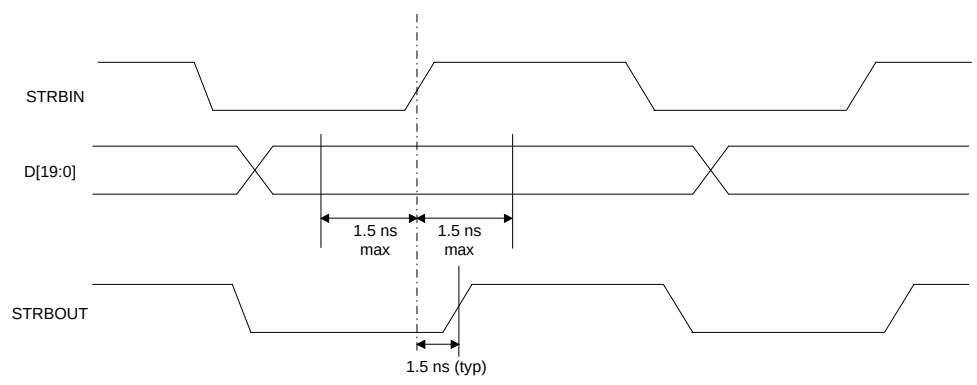
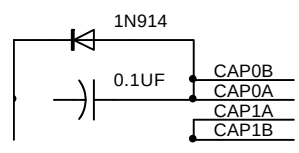


Table 4 Transmitter Connections

Pin Name (ECL)	Pin Type	Description
STRBIN (STRBIN*)	Input	Parallel word strobe frequency clock; Data valid on rising edge
HCLKON	Input	GND
HCLK/HCLK*	Output	AC couple to a 50Ω resistor to GND
LOUT/LOUT*	Output	AC couple to a 50Ω resistor to GND
LOOPEN	Input	GND
DOUT/DOUT*	Output	Connect to optical driver
DIV[1:0]	Input	See Table 3
INV		NC
TEMP/TEMP*		NC
RST*	Input	Transmitter active low reset
D[19:0]	Input	20 bit parallel data
RFD	Output	Re-timed version of ED can use as input to Heap Manager
ED	Input	Active high after lock is achieved
FF	Input	Vcc
CAV*	Input	Active low only when sending control data
DAV*	Input	Active low only when sending data
FLAGSEL	Input	GND
M20SEL	Input	Vcc for 20-bit format; GND for 16-bit format
MDFSEL	Input	GND
LOCKED	Output	Active high indicates transmitter locked
STRBOUT	Output	Copy of STRBIN when transmitter locked
EHCLKSEL	Input	GND
CAP0A, CAP1A , CAP0B, CAP1B	Input	See Figure 3

Figure 3 PLL Bypass Circuit



V. Designing a Rx Unit

Table 5 below describes the connections for a G-LINK receiver chip. In PECL designs, all lines should be properly terminated according to PECL design guidelines. Figure 4 shows the Rx timing diagram under normal operations. The appendix includes the reference designs used in the ORNL G-LINK test fixture. Figure 3 shows the necessary circuit for the PLL bypass.

Figure 4 Rx Timing

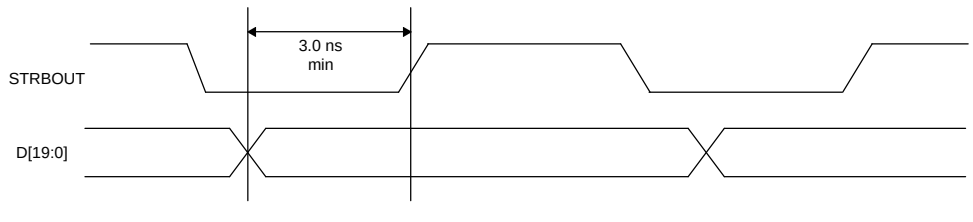


Table 5 Receiver Connections

Pin Name (ECL)	Pin Type	Description
TCLKSEL	Input	GND
TCLK	Input	NC
EQEN	Input	Vcc; Not required when using optical drivers
LIN/LIN*	Input	NC
LOOPEN	Input	GND
DIN/DIN*	Input	Connect to optical receiver
DIV[1:0]	Input	See Table 3
FDIS, ACTIVE, STAT1	Input/ Output	Connect together
STAT0	Output	Active high indicates receiver locked
SMRST[1:0]	Input	Active low receiver reset
D[19:0]	Output	20 bit parallel data
STRBOUT	Output	Parallel word strobe frequency clock; Data valid on rising edge
LINKRDY*	Output	Active low indicates receiver locked
FF	Output	NC
CAV*	Output	Active low only when receiving control data
DAV*	Output	Active low only when receiving data
FLAGSEL	Input	GND
M20SEL	Input	Vcc for 20-bit format; GND for 16-bit format
FLAG	Output	NC
ERROR	Output	Asserted when error in received frame
TEMP/TEMP*		NC
CAP0A, CAP1A , CAP0B, CAP1B	Input	See Figure 3

VI. Resetting the Link

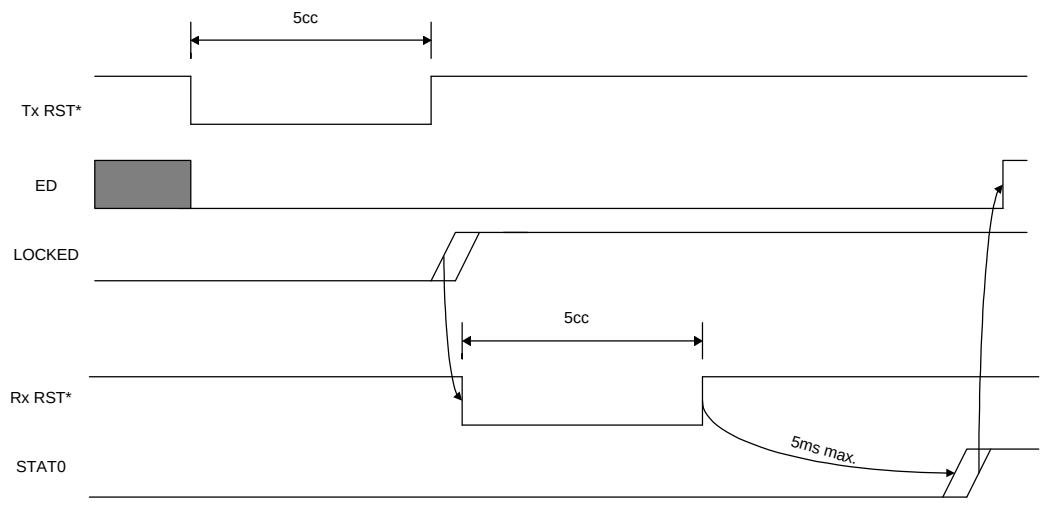
The G-Links lock and maintain lock by sending fill frames. There are two fill frame types available with the HP chips: ff0 and ff1. In Phenix we will use ff1 which requires that the FF pin on the Tx be pulled high. Also, DAV* and CAV* should be inactive when data is not being transmitted.

The first step in resetting the link and thus establishing lock, is to reset the transmitter unit by activating the RST* pin while holding the ED pin low. The RST* pin should be held in the active low state for a minimum of 5 clock cycles. Once this cycle is completed, the transmitter's internal PLL should be locked to the incoming strobe (STRBIN) and the output signal, LOCKED, should be active (high). Also, the STRBOUT should match STRBIN with a slight phase delay. The ED pin should remain low until the receiver has also been reset and locked.

Once the transmitter is locked, the next step is to reset the receiver and allow it to lock to the carrier frequency. The SMRST1* and SMRST0* pins should be pulled to the active low state for a minimum of 5 clock cycles. During this time the receiver's internal state machine will lock the internal PLL to the carrier frequency. Once the lock is complete the STAT0 will be active high and LINKRDY* will be active low. Also, the STRBOUT of the receiver unit should match the STRBIN of the transmitter unit.

A complete timing diagram is shown in Figure 5 below.

Figure 5 Link Reset Timing



VII. Additional Information

Additional information may be found in the data sheets for each of the components. The best information on the jitter of the recovered clock on the receiver is published in a technical article: "*A Two-chip 1.5 GBd Serial Link Interface*", IEEE Journal of Solid State Circuits vol. 27, no. 12, Dec 1992 pp 1805-1811.

References

Hewlett-Packard, "*HDMP-102K Evaluation Board User's Guide*", Rev 1.0, February 1997.

Hewlett-Packard, "*Reference Guide for the HDMP-101K Evaluation Board*", Rev 1.1, November 1996.

Hewlett-Packard, "*Answers to Common G-Link Design Questions*", Rev 2.1, January 1996.

R. C. Walker, et al., "*A Two-chip 1.5 GBd Serial Link Interface*", IEEE Journal of Solid State Circuits vol. 27, no. 12, Dec 1992 pp 1805-1811.

Appendix