Wafer Probe Test Specifications for the TGL98.V2 Chip (revised 2/22/99 onwards)

Overview:
The purpose of this document is to outline the wafer probe testing of the TGL98.V2 chip. The TGL98.V2 is a mixed signal chip that has 16 channels of preamplifier-discriminator channels and associated on-chip digital functions for various adjusts and enables. The main functional units of the chip to be tested are the preamplifier-discriminator block, decoder, serial registers, D/A converter and bias values. The steps to test the chip are devised to verify and isolate a known good die by eliminating a bad die as soon as it is detected. In other words, the progressive test steps need take place only if a die passes the previous test. The testing would do the following in order:

1. Determine the quiescent current drawn at the 3 sets of power supply pins.
2. Determine the bias values at the bias reference pins which will indicate the DAC output values as well as the resistor bias values.
3. Clock in serial data to the 3 sets of serial registers and read the data back which will test the decoder and the serial registers
4. Digitally pulse the on-chip charge-pulser for preamplifier/discriminator channels and observe the output current pulse as well as the reference current output. This tests the preamplifier-discriminator block.

Special instructions for the testing:

The scope of the entire testing includes
1. Design and fabrication of all probing fixtures associated with the chip interface at the wafer probe to the tester.
2. Programming of the tester in accordance with the test specifications
3. Execution of the tests
4. Inking out of "bad dies"
5. Standard dicing of the wafer after placing on sticky film
6. Visual inspection of the die after dicing and
7. Packaging of the good die to Lund (Sweden).

The probe card must be designed and fabricated in accordance to the test circuit shown in FIGURE 1. The separate supplies to power supply sets V1, V2 and V3 must be bypassed by capacitors placed as close to the probes as possible. The grounds are common. The bare die is very sensitive to light and care must be taken to eliminate spurious signal pickup at the input pads due to the presence of 60Hz. and other stray fields.

The die will be on 6" diameter wafers from Orbit's 1.2u analog CMOS process. The price quotation should be for testing 2 batches of wafers. A first, smaller batch of 5 wafers (4500 chips) and a second batch of 37 wafers (33,300 chips) which will need to be tested in about 6 weeks to 3 months from the first batch. There will be about 900 dies per wafer. Tested wafers will be standard diced. As soon as any die fails it will be identified as defective and any remaining tests for that die can be suspended. Bad die will also be returned to Lund, Sweden, but has to be inked to distinguish it from a good die.

Details of the testing:

The pad diagram of TGL98.V2 chip is given in Appendix 1 along with a table describing the pin details in Appendix 2. The numbering of the pins starts at the SW corner and proceeds in a clockwise direction. The test circuit, which is to be fabricated as the probe card is given in FIGURE 1. All inputs Vin(x) are left open with no connection for these tests. Iout(x) outputs are 70uA current pulses through 8.2k load resistor (574mV (peak). This means a nominal signal of pulse height ~400 mV (+/- 20%) and a pulse width of 150 ns (+/- 20%) occurring about 100 ns after the test pulse has been issued. All bias pins are to be probed and their voltages measured. The probe on AO will help to setup the test properly.

The serial decoder/addressing scheme of the TGL98.V2 is described in Appendix 3. The data register bits are defined in Appendix 4. Logic levels are 5V CMOS. The pad dimensions of the TGL98.V2 chip (fabricated in 1.2u ORBIT process as a SMALL chip) is given in Appendix 5.

The control pins and their functions are given briefly in Table 1.

Table 1. Control signal pins and their function

Pad	Pin Name	Type	Functional description
OS(30)	Operate (bar)/Serial mode	input	Mode bit: Used to define the shared function pins. OS = 5V => serial data mode; OS = 0V => operate chip mode.
SAD (31)	Serial Address/ Data(bar) mode	input	When OS=5V: SAD = 5V => address register select; and SAD = 0V => control register select; When OS = 0V: SAD = don't care.
RD_SC(33)	Reset Disable / Serial Clock shared function pin	input	RD = (RD_SC).OS(bar); analog reset SC = (RD_SC).OS; serial clock
TP_SL (34)	Test pulse / Serial latch shared function pin	input	TP = (TP_SL).OS(bar); test pulser SL = (TP_SL).OS.; serial latch
SI(35)	Serial Input	input	Serial data input pin.
SO(36)	Serial Output	output	Serial data output pin – active when RW bit =1, SAD=0 Else tristated.
SOE (32)	Transceiver direction select	output	SOE = 5V => read-back data from chip. Internally generated chip signal Else, tristated

Test 1:

1. Quiescent Current Measurement Test

The chip requires 3 independent power supplies of 5V DC and a reference voltage of 2.5V to function. Bypass capacitors of shown value need to be placed as close as possible to the chip between probe card needle and ground. Table 2 gives the criteria for the TGL98.V2 power pads and performance. The values in the table are those after the power-up state.

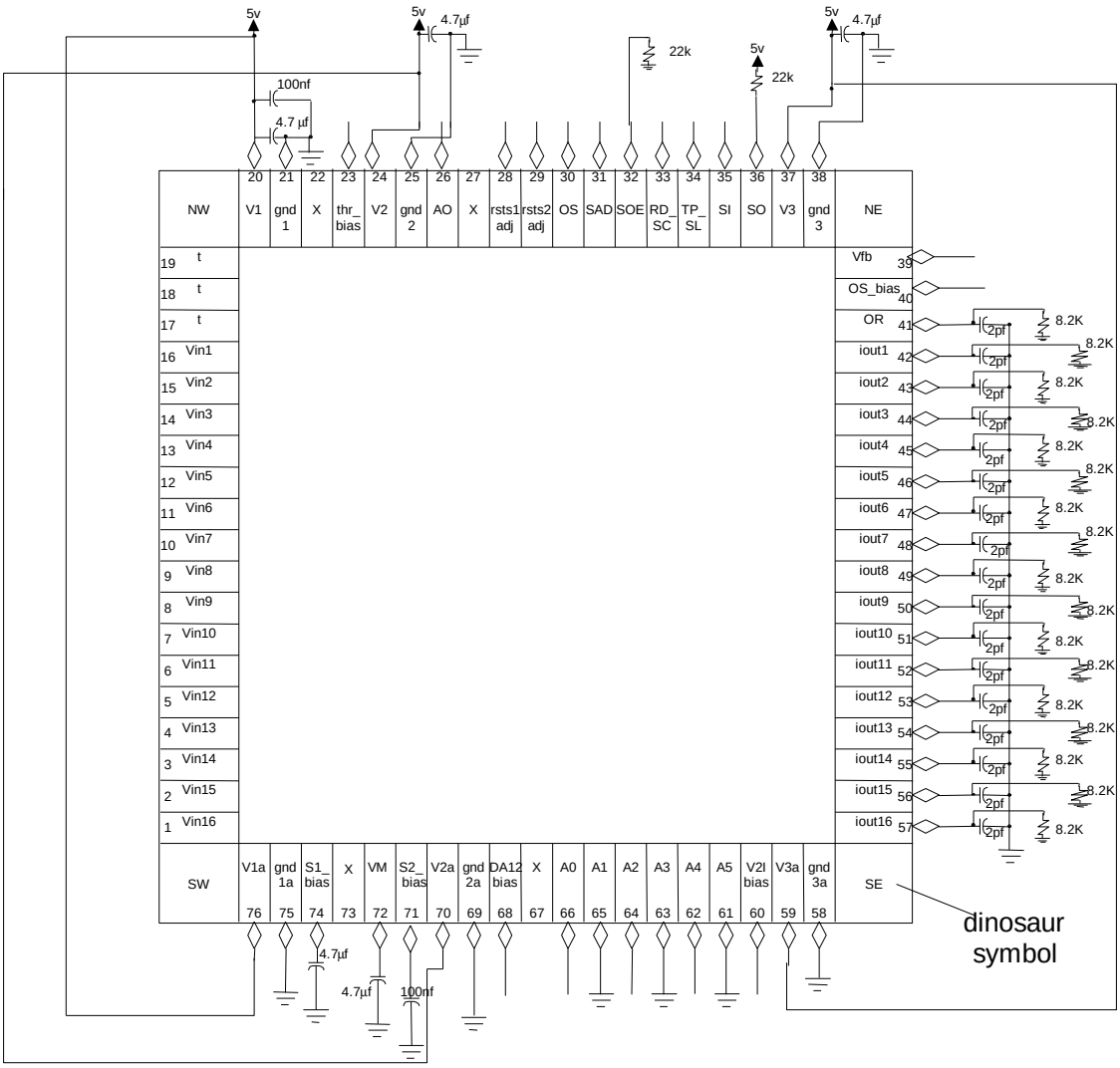
Table 2: Power pads and performance

Pad	Supply	Bypass	Function	Current drawn	Acceptable margin
20 and 76	5V dc	4.7uF ;	(V1)Analog1 supply	4.7mA	4.0mA – 5.5mA
21 and 75	0		Analog1 ground		
24 and 70	5V dc	4.7uF;	(V2)Analog2 supply	2.8mA	2.0mA – 3.3mA
25 and 69	0		Analog2 ground		
37 and 59	5V dc	4.7uF;	(V3)Digital supply	0.28mA	0.2mA – 0.5mA
38 and 58	0		Digital ground		
72	2.5V dc	4.7uF	(VM)Midpoint ref.	4.7 uA	+/- 1uA

If the current drawn at all pads are within the acceptable margin proceed to the next test

Note 1: All grounds are common.
Note 2: The input signals at the input pins SI, RD_SC, TP_SL, SAD and OS should be steady 0v for Test1 and Test2.

FIG. 1:TEST SETUP FOR THE WAFER PROBE TEST OF TGL98.v2



TEST 2:

2. Testing the Bias pin values:

   The voltages at the bias reference pins are to be measured just after the power-up state. If any one of these values is 0V or 5V the chip is deemed to fail at this point. The bias pads that need to be probed are given in Table 3.

Table 3: Bias pads and performance

Pad	Function	Nominal Value	Acceptable margin Min - Max
40	OS_bias – oneshot bias	3.2 V	2.56 V – 3.84 V
41	OR – Output reference current (~20uA) thru 8.2K	150mV	82mV – 240mV
68	DA12_bias	1.17 V	0..94 V – 1.4 V
71	S2_bias	3.15 V	2.5V – 3.8V
74	S1_bias	1.8 V	1.2V – 2.5 V

If the voltages at all pads are within the acceptable margin proceed to the next test

Note: The input signals at the input pins SI, RD_SC, TP_SL, SAD and OS should be steady 0v for Test1 and Test2.

TEST 3: Serial and Address Data Communication Test

Note: The serial register values are all to be loaded lsb (least significant bit) in first as indicated in the timing diagrams when writing to any register in TGL98.V2.

1. Select serial control mode for this test by setting serial mode pin OS = 5V

Note 1: Binary patterns refer '1' to CMOS Logic 5V, '0' to CMOS Logic 0V
Note 2: The clock frequency is 10 MHz and is applied to RD_SC pin.
Note 3: The data is shifted in on the rising edge of the clock when you write to a register
Note 4: The data is shifted out on the rising edge of the clock when you read-back from a register
Note 5: Read-back cannot be made with the broadcast bit A6 of address register set to 1. So, read-back should always be done with an address match.

TEST 3a: Write to and Read back CR1 even bits (address match test)
Refer to timing diagram in FIGURE 3a for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR1) and mode (write)
   a. Select address mode by setting SAD = 5V
   b. Clock in 0010010101 b pattern to address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after data is clocked in.

2. Write '1's to even bits of the control register CR1
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 0101 0101 0101 010b to load CR1 even bits with '1'. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after serial data is clocked.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR1) and mode (read-back)
   a. Select address mode by setting SAD = 5V
   b. Clock in 1010 0101 01 b pattern to address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	0	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Read back '1's from the even bits of control register CR1
   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue one clock pulse when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 18 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check the data shifted out on the rising edge of the clock via the SO pin.
      It should be 0101 0101 0101 0101 010b

TEST 3b: Write to and Read back CR1 odd bits (address match test)

Refer to timing diagram in FIGURE 3b for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR1) and mode (write)

   a. Select address mode by setting SAD = 5V
   b. Clock in 0010010101 b pattern to address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Write ‘1’s to odd bits of control register CR1

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1010 1010 1010 1010 101b to load CR1 odd bits with ‘1’. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR1) and mode (read-back)
   a. Select address mode by setting SAD = 5V
   b. Clock in 1010 0101 01 b pattern to address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	0	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after data is clocked in.

2. Read back 1’s from odd bits of control register CR1
   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue one clock pulse when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 18 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check data shifted out on the rising edge of the clock via the SO pin.
      It should read 1010 1010 1010 1010 101b

TEST 3c Write to and Read back CR2 even bits; A6=1 (broadcast mode test- no address match)

Refer to timing diagram in FIGURE 3c for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR2) and mode (write)

   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Write ‘1’s to even bits of CR2 register

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 0101 0101 010 b to load CR2 odd bits with ‘1’. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data is clocked.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR2) and mode (read-back)
   a. Select address mode by setting SAD = 5V
   b. Clock in 1100 0101 01b pattern to the address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Read back 1’s from even bits of control register CR2

   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue a single clock pulse when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 14 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check data shifted out on the rising edge of the clock via the SO pin.
      It should read 0101 0101 0101 010 b

TEST 3d: Write to and Read back CR2 odd bits; A6=1 (broadcast mode test- no address match)

Refer to timing diagram in FIGURE 3d for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR2) and mode (write)

   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b to the address register.

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Write the control word to the control register (CR2)

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1010 1010 1010 101 b to load CR2 odd bits with '1'. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after serial data is clocked.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR2) and mode (read-back)
   a. Select address mode by setting SAD = 5V for serial data transfer to address register through SI pad
   b. Clock in 1100 0101 01b pattern to the address register.

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	0	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after data is clocked in.

2. Read back 1's from odd bits of control register CR2

   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue a single clock pulse when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 14 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check data shifted out on the rising edge of the clock via the SO pin.
      It should read 1010 1010 1010 101 b

TEST 3e: Write to and Read back CR3 even bits; A6=1 (broadcast mode test- no address match)

Refer to timing diagram in FIGURE 3e for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR3) and mode (write)

   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to the address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

3. Write the control word to the control register (CR3)

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 0101 0101 0101 0101 0101 010 b to load 1's in CR3 even bits. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after serial data is clocked.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR3) and mode (read-back)
   a. Select address mode by setting SAD = 5V
   b. Clock in 1110 0101 01b pattern to the address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Read 1's from even bits of control register (CR3)

   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue a single clock when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 26 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check data shifted out on the rising edge of the clock via the SO pin.
      It should read 0101 0101 0101 0101 0101 0101 010 b

TEST 3f: Write to and Read back CR3 odd bits; A6=1 (broadcast mode test- no address match)

Refer to timing diagram in FIGURE 3f for the following test steps.

A. DATA WRITE PROCEDURE:

1. Load address register to select control register address (CR3) and mode (write)

   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to the address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

4. Write the control word to the control register CR3

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1010 1010 1010 1010 1010 1010 101 b to load 1's in CR3 odd bits. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after serial data is clocked.

B. DATA READ-BACK PROCEDURE:

1. Load address register to select control register address (CR3) and mode (read-back)
   a. Select address mode by setting SAD = 5V
   b. Clock in 1110 0101 01b pattern to the address register

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
1	1	1	0	0	1	0	1	0	1

   c. Latch the address register by 5V -> 0V transition on TP_SL line after serial data is clocked in.

2. Read back 1's from odd bits of control register CR3

   a. Select data mode by setting SAD =0V
   b. Issue a pulse 0V -> 5V -> 0V through TP_SL pin, after SAD changes state to 0V.
   c. Issue a single clock pulse when TP_SL is 5V. This will latch back data to be shifted out.
   d. Check SOE pin also. After SAD changes to 0v it should change from a tristated condition to 5V.
   e. Issue 26 clock pulses after the latch-back operation and after TP_SL has returned to 0V.
   f. Check the data shifted out on the rising edge of the clock via the SO pin.
      It should read 1010 1010 1010 1010 1010 1010 101 b

TEST 4: Operating mode Test for Amplitude, Attenuator

Preamplifier-Discriminator testing for 8 conditions:

4.1 2fC(DAC=2) input charge, 3 fC threshold (THR=50), Att=1; four channels pulsed at a time; all channels enabled

4.1.a. channels 1-4 test pulsed
4.1.b.channels 5-8 test pulsed
4.1.c.channels 9-12 test pulsed
4.1.d.channels 13-16 test pulsed

4.2 5 fC (DAC=7)input charge, 3 fC threshold(THR=50), Att=1; four channels pulsed at a time; all channels enabled

4.2.a. channels 1-4 test pulsed
4.2.b. channels 5-8 test pulsed
4.2.c. channels 9-12 test pulsed
4.2.d. channels 13-16 test pulsed

4.3 5 fC (DAC=6)input charge, 7 fC threshold(THR=10), Att=1; four channels pulsed at a time; all channels enabled

4.3.a. channels 1-4 test pulsed
4.3.b. channels 5-8 test pulsed
4.3.c. channels 9-12 test pulsed
4.3.d. channels 13-16 test pulsed

4.4 9fC (DAC=10)input charge, 7 fC threshold (THR=10), Att=1; four channels pulsed at a time; all channels enabled

4.4.a. channels 1-4 test pulsed
4.4.b. channels 5-8 test pulsed
4.4.c. channels 9-12 test pulsed
4.4.d. channels 13-16 test pulsed

4.5 All channels at 12fC (DAC=15) input charge, 15 fC threshold (THR=31), Att=1/3;all channels pulsed; all channels enabled

4.6 All channels at 19fC (DAC=24) input charge, 15 fC threshold(THR=31), Att=1/3;all channels pulsed; all channels enabled

4.7 All channels at 33 fC (DAC=42)input charge, 44 fC threshold(THR=31), Att=1/9;all channels pulsed; all channels enabled

4.8 All channels at 58 fC (DAC=73) input charge, 44 fC threshold(THR=31), Att=1/9;all channels pulsed; all channels enabled

The tests 4.1 to 4.8 will all have same value in CR3 (all channels enabled, mux off, Vfb=1.5v(DAC=30))
The sequence for this will be

1. Set serial mode.
2. Set SAD and TP_SL pins as needed
3. Load address register to write to CR3
4. Load serial control registers CR3 – for all channels enabled, mux off, Vfb = 1.5V (DAC=30)

Then for tests 4.1 to 4.4 first load CR2 with appropriate value for that test

5. Set serial mode.

6. Set SAD and TP_SL pins as needed
7. Load address register to write to CR2
8. Load serial control registers CR2 with appropriate values of threshold and test pulse values

For each test 4.1 through 4.4, load appropriate values into CR1 to pulse channels 1-4, then 5-8, then 9-12 and 13-16. After each load of CR1 generate a test pulse and observe the outputs.

1. Set serial mode
2. Load address register to write to CR1
3. load serial control registers CR1 to pulse channels 1-4, steepest slope
4. Setup operating mode
5. Issue reset
6. Issue test pulse
7. Observe the output at pads iout1 … iout16.

Repeat steps 1-7 above changing only step 3 for channels 5-8, 9-12, and 13-16 successively.

The sequence for tests 4.5 to 4.8 will be (CR3 is the same as loaded earlier). Now CR1 will be the same for these 4 tests (i.e. all channels pulsed and steepest slope)

1. Set serial mode.
2. Set SAD and TP_SL pins as needed
3. Load address register to write to CR1
4. Load serial control registers CR1 with all channels pulsed

Then for each test 4.5 through 4.8, load appropriate values into CR2

5. Set serial mode
6. Load address register to write to CR2
7. load serial control registers CR2 with appropriate threshold and test pulse values
8. Setup operating mode
9. Issue reset
10. Issue test pulse
11. Observe the output at pads iout1 … iout16.

Note: *The outputs will be pulses that are 150 ns (+/- 30 ns) wide, ~570mV(+/- 20%) in amplitude (if flat-top is reached) occurring about 100ns after the test pulse has been issued. The output at OR pin must be a steady at ~150 mV (+/- 20mV) signal. The tester should be set at a threshold of about 200mV. Any signal above that at the output pins should be construed as a "fired channel".*

Test 4 :
For all tests 4.1 to 4.8 (CR3 is same)All channels enabled; mux off; Vfb=1.5v equiv(DAC=30)
(Common for all tests 4.1 through 4.8)

Refer to the timing diagram in FIGURE 4.0 for this part of the test.

1. Set up serial mode
   Set serial mode pin OS = 5V

2. Set SAD pin =5V; set TP_SL pin = 5V

3. Load address register to write to CR3

   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR3 – for all channels enabled, mux disabled; Vfb = 1.5v
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0000 0000 0000 0000 1000 0011 110 b to load CR3. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4.1:
All channels at 2 fC (DAC=2) input charge, 3 fC (DAC=50)threshold, Att=1

Refer to the Timing diagram in FIGURE 4.1 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1; threshold = 3fC; pulse amplitude = 2fC
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0011 0010 0000 010 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	1	0	0	1	0	0	0	0	0	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4.1a:
Channels 1-4 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.1.a for this test.

3. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR1 – channels 1-4 pulsed ; steepest slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 0000 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

5. Change OS pin to 0V for operating mode.

6. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

7. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

8. Observe the output at pads iout1 … iout16 (42 – 57).
   No outputs must fire.

Test 4.1b:
Channels 5-8 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.1.b for this test.

9. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

10. load serial control registers CR1 – channels 5-8 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 1111 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

11. Change OS pin to 0V for operating mode.

12. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

13. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

14. Observe the output at pads iout1 … iout16 (42 – 57).

No outputs must fire.

Test 4.1c:
Channels 9-12 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.1.c for this test.

15. Load address register to write to CR1
    a. Select address mode by setting SAD = 5V
    b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

    c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

16. load serial control registers CR1 – channels 9-12 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 1111 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

17. Change OS pin to 0V for operating mode.

18. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

19. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

20. Observe the output at pads iout1 … iout16.
    No outputs must fire.

Test 4.1d:
Channels 13-16 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.1.d for this test.

21. Load address register to write to CR1
    a. Select address mode by setting SAD = 5V
    b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

22. load serial control registers CR1 – channels 13-16 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 0000 1111 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

23. Change OS pin to 0V for operating mode.

24. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

25. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

26. Observe the output at pads iout1 … iout16 (42 – 57).
    No outputs must fire.

Test 4.2:
All channels at 5 fC (DAC=7)input charge, 3 fC (DAC=50)threshold, Att=1

Refer to the Timing diagram in FIGURE 4.2 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1; threshold = 3fC; pulse amplitude = 5fC
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0011 0010 0000 111 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	1	0	0	1	0	0	0	0	0	1	1	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4.2a:
Channels 1-4 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.2.a for this test.

3. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR1 – channels 1-4 pulsed ; steepest slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 0000 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

5. Change OS pin to 0V for operating mode.

6. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

7. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

8. Observe the output at pads iout1 … iout16 (42 – 57).
   Only outputs 1-4 must fire.

Test 4.2b:
Channels 5-8 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.2.b for this test.

9. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

10. load serial control registers CR1 – channels 5-8 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 1111 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

11. Change OS pin to 0V for operating mode.

12. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

13. Issue test pulse

Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

14. Observe the output at pads iout1 … iout16 (42 – 57).
    Only outputs 5-8must fire.

Test 4.2.c:
Channels 9-12 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.2.c for this test.

15. Load address register to write to CR1
    a. Select address mode by setting SAD = 5V
    b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

    c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

16. load serial control registers CR1 – channels 9-12 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 1111 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

17. Change OS pin to 0V for operating mode.

18. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

19. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

20. Observe the output at pads iout1 … iout16.
    Only outputs 9-12must fire.

Test 4.2.d:
Channels 13-16 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.2.d for this test.

21. Load address register to write to CR1

a. Select address mode by setting SAD = 5V
b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

22. load serial control registers CR1 – channels 13-16 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 0000 1111 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

23. Change OS pin to 0V for operating mode.

24. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

25. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

26. Observe the output at pads iout1 … iout16 (42 – 57).
    Only outputs 13-16 must fire.

Test 4.3:
All channels at 5 fC (DAC=6) input charge, 7 fC (DAC=10)threshold, Att=1

Refer to the Timing diagram in FIGURE 4.3 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1; threshold = 7fC(DAC=10); pulse amplitude = 5fC(DAC=6)
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0000 1010 0000 110 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	0	0	1	0	1	0	0	0	0	0	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4.3.a:
Channels 1-4 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.3.a for this test.

3. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR1 – channels 1-4 pulsed ; steepest slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 0000 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

5. Change OS pin to 0V for operating mode.

6. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

7. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

8. Observe the output at pads iout1 … iout16 (42 – 57).
   No outputs must fire.

Test 4.3b:
Channels 5-8 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.3.b for this test.

9. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

10. load serial control registers CR1 – channels 5-8 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 1111 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

11. Change OS pin to 0V for operating mode.

12. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

13. Issue test pulse

Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

14. Observe the output at pads iout1 … iout16 (42 – 57).
    No outputs must fire.

Test 4.3.c:
Channels 9-12 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.3.c for this test.

15. Load address register to write to CR1
    a. Select address mode by setting SAD = 5V
    b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

    c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

16. load serial control registers CR1 – channels 9-12 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 1111 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

17. Change OS pin to 0V for operating mode.

18. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

19. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

20. Observe the output at pads iout1 … iout16.
    No outputs must fire.

Test 4.3.d:
Channels 13-16 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.3.d for this test.

21. Load address register to write to CR1

a. Select address mode by setting SAD = 5V
b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

22. load serial control registers CR1 – channels 13-16 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 0000 1111 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

23. Change OS pin to 0V for operating mode.

24. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

25. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

26. Observe the output at pads iout1 … iout16 (42 – 57).
    No outputs must fire.

Test 4.4:
All channels at 9 fC (DAC=10)input charge, 7 fC (DAC=10)threshold, Att=1

Refer to the Timing diagram in FIGURE 4.4 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1; threshold = 7fC(DAC=10); pulse amplitude = 9fC(DAC=10)
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0000 1010 0001 010 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	0	0	1	0	1	0	0	0	0	1	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4.4a:
Channels 1-4 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.4.a for this test.

3. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR1 – channels 1-4 pulsed ; steepest slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 0000 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

5. Change OS pin to 0V for operating mode.

6. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

7. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

8. Observe the output at pads iout1 … iout16 (42 – 57).
   Only outputs 1-4 must fire.

Test 4.4b:
Channels 5-8 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.4.b for this test.

9. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

10. load serial control registers CR1 – channels 5-8 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 1111 0000 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

11. Change OS pin to 0V for operating mode.

12. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

13. Issue test pulse

Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

14. Observe the output at pads iout1 … iout16 (42 – 57).
    Only outputs 5-8must fire.

Test 4.4.c:
Channels 9-12 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.4.c for this test.

15. Load address register to write to CR1
    a. Select address mode by setting SAD = 5V
    b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

    c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

16. load serial control registers CR1 – channels 9-12 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 1111 0000 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0

    c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

17. Change OS pin to 0V for operating mode.

18. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

19. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

20. Observe the output at pads iout1 … iout16.
    Only outputs 9-12must fire.

Test 4.4.d:
Channels 13-16 pulsed; steepest slope

Refer to the Timing diagram in FIGURE 4.4.d for this test.

21. Load address register to write to CR1

a. Select address mode by setting SAD = 5V
b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

22. load serial control registers CR1 – channels 13-16 pulsed ; steepest slope
    a. Change to data mode by setting SAD =0V
    b. Clock in pattern 0000 0000 0000 1111 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0

c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

23. Change OS pin to 0V for operating mode.

24. Issue reset
    Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

25. Issue test pulse
    Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

26. Observe the output at pads iout1 … iout16 (42 – 57).
    Only outputs 13-16 must fire.

Test 4. 5to8:
All channels pulsed; steepest leakage slope; all channels enabled, mux off, Vfb=1.5v (DAC=30)
(CR1 values common to tests 4.5 through 4.8)

Refer to the Timing diagram in FIGURE 4.5to8 for this test. (CR3 is already loaded with the right value)

1. Set up serial mode
   Set serial mode pin OS = 5V

2. Set SAD pin =5V; set TP_SL pin = 5V

3. Load address register to write to CR1

   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

4. load serial control registers CR1 – for all channels pulsed, steepest leakage slope

   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 1111 1111 1111 000 b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 4. 5:
All channels at 12fC input charge (DAC=15), 15 fC threshold (DAC=31), Att=1/3 (01)

Refer to the Timing diagram in FIGURE 4.5 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1/3; threshold = 15fC; pulse amplitude = 12fC
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 1111 0001 111 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	1	0	1	1	1	1	1	0	0	0	1	1	1	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

4. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

5. Observe the output at pads iout1 … iout16 (42 – 57).
   No outputs must fire.

Test 4.6:
All channels at 19fC (DAC=24) input charge, 15 fC threshold (DAC=31), Att=1/3(01);all channels pulsed; steepest leakage slope; all channels enabled

Refer to the Timing diagram in FIGURE 4.6 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1/3; threshold = 15fC; pulse amplitude = 19fC
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 1111 0011 000 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	1	0	1	1	1	1	1	0	0	1	1	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

4. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

5. Observe the output at pads iout1 … iout16 (42 – 57).
   All outputs must fire.

Test 4.7:
All channels at 33fC (DAC=42) input charge, 44 fC threshold (DAC=31), Att=1/9 (10b);all channels pulsed; steepest leakage slope; all channels enabled

Refer to the Timing diagram in FIGURE 4.7 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1/9; threshold = 44fC(DAC=31); pulse amplitude = 33fC(DAC=42)
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1001 1111 0101 010 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
1	0	0	1	1	1	1	1	0	1	0	1	0	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

4. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

5. Observe the output at pads iout1 … iout16 (42 – 57).
   No outputs must fire.

Test 4.8:
All channels at 58fC (DAC=73)input charge, 44 fC threshold (DAC=31), Att=1/9(10b);all channels pulsed; steepest leakage slope; all channels enabled

Refer to the Timing diagram in FIGURE 4.8 for this test.

1. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR2 – for att=1/9; threshold = 44fC(DAC=31); pulse amplitude = 58fC(DAC=73)
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1001 1111 1001 001 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
1	0	0	1	1	1	1	1	1	0	0	1	0	0	1

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

4. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

5. Observe the output at pads iout1 … iout16 (42 – 57).
   All outputs must fire.

TEST 5: Operating mode Test for Cross Talk/ Feedthrough

a. All channels at 90 fC input charge, 2 fC threshold, Att=1;odd channels pulsed; all channels enabled
b. All channels at 90 fC input charge, 2 fC threshold, Att=1;even channels pulsed; all channels enabled

The sequence will be

1. Setup serial mode
2. Set SAD and TP_SL pins
3. Load address register to write to CR2
4. load serial control registers CR2 – for 90fC charge input, 2fC threshold, att=1
5. Load address register to write to CR3
6. load serial control registers CR3 – for all channels enabled, mux off, Vfb = 1.5V DAC equivalent

Then for each section, load appropriate values into CR1

1. Set serial mode
2. Load address register to write to CR1
3. load serial control registers CR1 to appropriate value
4. Set operating mode
5. Issue reset
6. Issue test pulse
7. Observe the output at pads iout1 … iout16 (42 – 57).

Note: *The outputs will be pulses that are 150 ns (+/- 30 ns) wide, ~570mV(+/- 20%) in amplitude (if flat top is reached) occurring about 100ns after the test pulse has been issued. The output at OR pin must be a steady at ~150 mV (+/- 20mV) signal. The tester should be set at a threshold of about 200mV. Any signal above that at the output pins should be construed as a "fired channel".*

Test 5: All channels at 90fC (DAC=110); threshold = 2fC (DAC=50), att=1 (00), steepest leakage; all channels enabled; mux off; Vfb = 1.5v equiv.
Refer to the timing diagram in FIGURE 5 for this part of the test.

1. Set up serial mode by OS pin= 0V and TP_SL pin = 5V

2. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

3. Load serial control registers CR2 – for 90fC charge input (DAC=110), 2fC threshold (DAC=50), att=1
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0011 0010 1101 110 b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	1	0	0	1	0	1	1	0	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

4. Load address register to write to CR3
   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

5. load serial control registers CR3 – for all channels enabled, mux disabled; Vfb = 1.5v
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0000 0000 0000 0000 1000 0011 110 b to load CR3. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 5a:
All channels at 90fC input charge, 2 fC threshold, Att=1;odd channels pulsed; steepest leakage slope; all channels enabled

Refer to the Timing diagram in FIGURE 5a for this test.

1. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V. Set OS = 5v for serial mode.
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR3 – for odd channels pulsed, steepest slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1010 1010 1010 1010 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Change to operating mode by setting OS=0v

4. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

5. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

6. Observe the output at pads iout1 … iout16 (42 – 57).
   Only odd channel outputs must fire.

Test 5b:
All channels at 90fC input charge, 2 fC threshold, Att=1;even channels pulsed; steepest slope; all channels enabled

Refer to the Timing diagram in FIGURE 5b for this test.

1. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V. Set OS = 5v for serial mode.
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR1 for even channels pulsed
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 0101 0101 0101 000 b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Change to operating mode by setting OS=0v

4. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

5. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

6. Observe the output at pads iout1 … iout16 (42 – 57).
   Only even channel outputs must fire.

TEST 6: Operating mode Test for Cross Talk/ Feedthrough via channel disables

a. All channels at 90 fC input charge, 2 fC threshold, Att=1;all channels pulsed; odd channels enabled
b. All channels at 90 fC input charge, 2 fC threshold, Att=1;all channels pulsed; even channels enabled

The sequence will be
1. Setup OS to serial mode
2. Set SAD and TP_SL pins
3. Load address register to write to CR1
4. load serial control registers CR1 – for all channels pulsed, steepest leakage slope
5. Load address register to write to CR2
6. load serial control registers CR2 – for 90fC charge input, 2fC threshold, att=1

Then for each section, load appropriate values into CR3
1. Set up OS to serial mode
2. Load address register to write to CR3
3. load serial control registers CR3 to appropriate value
4. Change OS to operating mode
5. Issue reset
6. Issue test pulse
7. Observe the output at pads iout1 … iout16 (42 – 57).

Note: *The outputs will be pulses that are 150 ns (+/- 30 ns) wide, ~570mV(+/- 20%) in amplitude (if flat-top is reached) occurring about 100ns after the test pulse has been issued. The output at OR pin must be a steady at ~150 mV (+/- 20mV) signal. The tester should be set at a threshold of about 200mV. Any signal above that at the output pins should be construed as a "fired channel".*

Test 6: All channels at 90fC; threshold = 2fC, att=1, maximum leakage slope; all channels pulsed
Refer to the Timing diagram in FIGURE 6 for this test.

1. Set up operating mode pin OS = 5V for serial mode and TP_SL pin = 5V

2. Load address register to write to CR1
   a. Select address mode by setting SAD = 5V
   b. Clock in 0011 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	0	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

5. load serial control registers CR1 – all channels pulsed and maximum leakage slope
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1111 1111 1111 1111 000b to load CR1. Clock in 19 times.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

6. Load address register to write to CR2
   a. Select address mode by setting SAD = 5V
   b. Clock in 0101 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	0	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

7. load serial control registers CR2 – for att=1; charge = 90fC (DAC=110); threshold = 2fC(DAC=50)
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0011 0010 1101 110b to load CR2. Clock in 15 times.

At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1
0	0	1	1	0	0	1	0	1	1	0	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

Test 6a: All channels at 90fC input charge, 2 fC threshold, Att=1;all channels pulsed; steepest leakage slope; odd channels enabled

Refer to the Timing diagram in FIGURE 6a for this test.

1. Load address register to write to CR3
   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. load serial control registers CR3 – for odd channels enabled; mux off; VFb=1.5v equiv.
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 1010 1010 1010 1010 1000 0011 110b to load CR3. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0	0	0	0	1	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

3. Change to operating mode by setting OS=0v

4. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

5. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

6. Observe the output at pads iout1 … iout16 (42 – 57).
   Only odd channel outputs must fire.

Test 6b:
All channels at 90fC input charge, 2 fC threshold, Att=1;all channels pulsed; steepest leakage slope; even channels enabled

Refer to the Timing diagram in FIGURE 6b for this test.

1. Load address register to write to CR3
   a. Select address mode by setting SAD = 5V
   b. Clock in 0111 0000 00 b pattern to SI pin

R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0

   c. Latch the address register by 5V -> 0V transition on TP_SL line after address register contents are clocked in.

2. Load serial control registers CR3 – for odd channels enabled; mux off; VFb=1.4v equiv.
   a. Change to data mode by setting SAD =0V
   b. Clock in pattern 0101 0101 0101 0101 1000 0111 110b to load CR3. Clock in 27 times.

D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	0	0	0	0	1	1	1	1	0

   c. Latch the data register by 5V -> 0V transition on TP_SL line after data register contents are clocked.

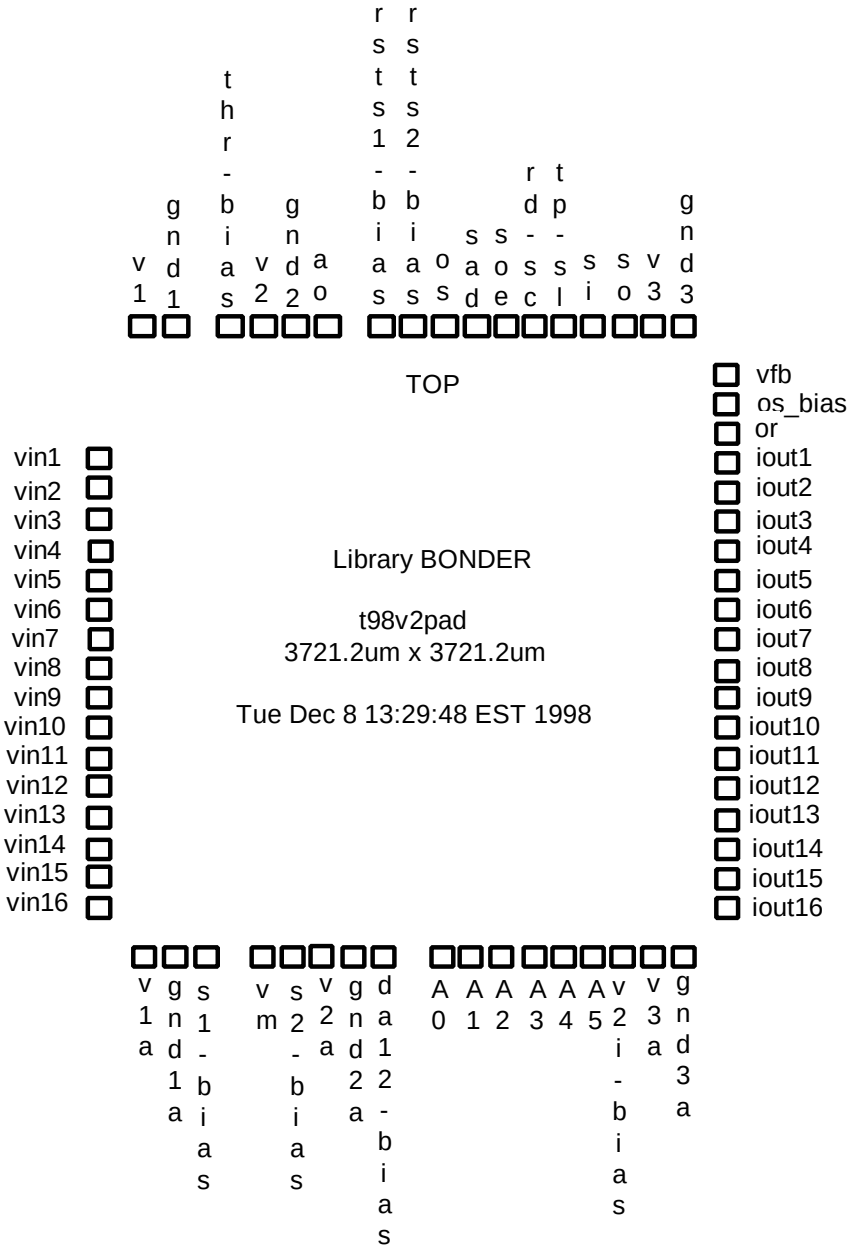
3. Change to operating mode by setting OS=0V

4. Issue reset
   Issue a 2 µsec. 0 -> 5V -> 0V pulse through RD_SC pin about 10 µseconds after OS has gone 0V. This issues the reset to the preamp.

5. Issue test pulse
   Wait for 7 µsec. after the RD_SC reset pulse. Bring TP_SL pin to 0V. This issues the internal test pulse.

6. Observe the output at pads iout1 … iout16 (42 – 57).
   Only even channel outputs must fire.

APPENDIX 1: PINOUT OF THE TGL98.V2 CHIP



APPENDIX 2: TGL98.V2 PIN LIST

Pin.no	Name.	Description	I/O type
1	Vin16	Input 16	Charge input
2	Vin15	Input 15	Charge input
3	Vin14	Input 14	Charge input
4	Vin13	Input 13	Charge input
5	Vin12	Input 12	Charge input
6	Vin11	Input 11	Charge input
7	Vin10	Input 10	Charge input
8	Vin9	Input 9	Charge input
9	Vin8	Input 8	Charge input
10	Vin7	Input 7	Charge input
11	Vin6	Input 6	Charge input
12	Vin5	Input 5	Charge input
13	Vin4	Input 4	Charge input
14	Vin3	Input 3	Charge input
15	Vin2	Input 2	Charge input
16	Vin1	Input 1	Charge input
17	t	Power thru spacer pad	
18	t	Power thru spacer pad	
19	t	Power thru spacer pad	
Corner	NW	Power thru corner pad	
20	V1	Preamp S1 supply	Preamp S1 supply, RC iso from LDO
21	Gnd1	Ground	Common ground
22	X	Ground ring spacer pad	
23	THRbias	Threshold bias bypass	Threshold current ref., bypass cap to gnd.
24	V2	Discriminator/ S2 supply	Analog supply to S2, mux and discriminator, RC iso from LDO
25	Gnd2	Ground	Common ground
26	AO	Analog output	Analog output voltage
27	X	Ground ring spacer pad	
28	RSTS1	S1 reset length adjust/ bypass	Reset circuit (1st stage) charging current ref., Bypass cap toV3
29	RSTS2	S2 reset length adjust/ bypass	Reset circuit (2nd stage) charging current ref., Bypass cap toV3
30	OS	Operate/serial mode	Digital input, 489 rcvr
31	SAD	Address/data control	Digital input, 489 rcvr
32	SOE	Serial output enable	Digital output, open drain, 485 xcvr, tristate
33	RD/SC	Reset-Disable/Serial clock	Digital input, 489 rcvr
34	TP/SL	Test pulse/ Serial latch	Digital input, 489 rcvr
35	SI	Serial input	Digital input, 485 xcvr
36	SO	Serial output	Digital output, open drain, 485 xcvr,triatate
37	V3	Digital/switching supply	Digital/ Reset/ Switching supply, RC isolated from LDO
38	Gnd3	Ground	Common ground
Corner	NE	Power thru corner pad	
39	Vfb	Power thru spacer pad	Feedback adjust thru DAC, bypass cap to gnd.
40	OSbias	One shot bias adjust/ bypass	Oneshot current bias ref., bypass cap to V3
41	OR	Output reference current	Current source output 20uA
42	Iout1	Output 1	Current source output, 70uA
43	Iout2	Output 2	Current source output, 70uA
44	Iout3	Output 3	Current source output, 70uA
45	Iout4	Output 4	Current source output, 70uA
46	Iout5	Output 5	Current source output, 70uA
47	Iout6	Output 6	Current source output, 70uA
48	Iout7	Output 7	Current source output, 70uA
49	Iout8	Output 8	Current source output, 70uA
50	Iout9	Output 9	Current source output 70uA
51	Iout10	Output 10	Current source output 70uA
52	Iout11	Output 11	Current source output 70uA
53	Iout12	Output 12	Current source output 70uA
54	Iout13	Output 13	Current source output 70uA
55	Iout14	Output 14	Current source output 70uA
56	Iout15	Output 15	Current source output 70uA
57	Iout16	Output 16	Current source output 70uA
Corner	SE	Power thru corner pad	
58	Gnd3a	Ground	Common ground
59	V3a	Digital/ switching supply	Digital/ Reset/ Switching supply, RC isolated from LDO
60	V2Ibias	Current switch bias adjust/ bypass	V2I cell bias current ref., bypass cap to V3
61	A5	Address line 5	CMOS pull-up input, gnd or nc
62	A4	Address line 4	CMOS pull-up input, gnd or nc
63	A3	Address line 3	CMOS pull-up input, gnd or nc
64	A2	Address line 2	CMOS pull-up input, gnd or nc
65	A1	Address line 1	CMOS pull-up input, gnd or nc
66	A0	Address line 0	CMOS pull-up input, gnd or nc
67	X	Ground ring spacer pad	
68	da12_bias	Differential Amp. Bias adjust/ bypass	Diffamp. Stage 1,2 bias current ref. , bypass cap to gnd.
69	Gnd2a	Ground	Common ground
70	V2a	Discriminator/ S2 supply	Analog supply to S2, mux and discriminator, RC iso from LDO
71	S2bias	S2 bias adjust/ bypass	S2 current ref. bypass, cap to V2
72	VM	Voltage midpoint input	2.5V reference input, w/ bypass to gnd.
73	X	Ground ring spacer pad	
74	S1bias	S1 bias adjust/ bypass	S1 current ref. bypass, cap to gnd
75	Gnd1a	Ground	Common ground
76	V1a	Preamp S1 supply	Preamp S1 supply, RC iso from LDO
Corner	SW	Power thru corner pad	

APPENDIX 3

The TGL98.V2 has a **10 bit address register tgl_adreg** that stores command data is present in the chip. It qualifies the clocks and latches based on value of OS and SAD signals. It generates the shift register select signal "sel" to either read in data from a serial string or latch back data from the serial register latch based on the value of rw, ro and r1. The address register contents A0..A5 are passed through a decoder that checks if the addresses match with the hardwired chip address. The chip is selected if addresses match or if bit A6 (broadcast bit is 5V). It decodes the commands received only if that chip is being addressed. The **address decoder** first compares the lowest 5 data bits with A0.. A5 pins (66. 61) to see if they match or checks to see if A6='1'. Only if one of the above mentioned conditions match is the rest of the decoding enabled.

The TGL98.V2 has three sets of **serial data registers CR1, CR2 and CR3** to do the controls of the TGL98.V2 for different modes of operation and configuration, which are controlled, by a serially loaded address register.

CR1 is the test pattern control register. It selects which channel is to be enabled for test pulsing and has 3 bits for adjusting the leakage slope of the preamp. The signal to select a channel is active high (5V).

CR2 is the Control register that controls the attenuator, the discriminator threshold and the test amplitude. The test amplitude is a 7 bit DAC input that selects the value of Vtest which varies in steps of 1fC equivalent. The discriminator threshold is a 6 bit DAC input that sets the discriminator level. The attenuator select helps to select the gross charge range of interest.

CR3 is the register that enables/disables (0/1) a channel and also sets the bits that control the preamp MUX output and sets the 6 bits that adjust the feedback voltage DAC.

The serial data bits of the address register and the 3 data registers is briefly defined in Appendix 4.

The data is shifted via pin (SI) and read out via pin (SO). The test patterns to be applied follow the given sequence. SOE is an output pin which enables the 489 transceiver board. It is tristated when data is shifted in and pulled low (0V) when data is being shifted out of the chip.

APPENDIX 4: TGL98.V2 SERIAL DATA BITS

TGL98.V2 SERIAL ADDRESS REGISTER

msb									lsb
R/W	R1	R0	A6	A5	A4	A3	A2	A1	A0

R0	Register address MSB; 00=no register, 01=CR1, 10=CR2 , 11= CR3
R1	Register address LSB; 00=no register, 01=CR1, 10=CR2 , 11= CR3
A6	TGL98.V2 address broadcast bit
A5	MSB TGL98.V2 address bit
A4	5SB TGL98.V2 address bit
A3	4SB TGL98.V2 address bit
A2	3SB TGL98.V2 address bit
A1	2SB TGL98.V2 address bit
A0	LSB TGL98.V2 address bit

CR1: TEST PATTERN AND DECAY SLOPE COMPENSATION CONTROL REGISTER

msb																		lsb
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	DS3	DS2	DS1

T1	0= disable test pulse, 1= enable test pulse, channel 1
T2	0= disable test pulse, 1= enable test pulse, channel 2
T3	0= disable test pulse, 1= enable test pulse, channel 3
T4	0= disable test pulse, 1= enable test pulse, channel 4
T5	0= disable test pulse, 1= enable test pulse, channel 5
T6	0= disable test pulse, 1= enable test pulse, channel 6
T7	0= disable test pulse, 1= enable test pulse, channel 7
T8	0= disable test pulse, 1= enable test pulse, channel 8
T9	0= disable test pulse, 1= enable test pulse, channel 9
T10	0= disable test pulse, 1= enable test pulse, channel 10
T11	0= disable test pulse, 1= enable test pulse, channel 11
T12	0= disable test pulse, 1= enable test pulse, channel 12
T13	0= disable test pulse, 1= enable test pulse, channel 13
T14	0= disable test pulse, 1= enable test pulse, channel 14
T15	0= disable test pulse, 1= enable test pulse, channel 15
T16	0= disable test pulse, 1= enable test pulse, channel 16
DS3	MSB, decay slope select MUX, 111 = no decay
DS2	2SB, decay slope select MUX
DS1	LSB, decay slope select MUX, 000 = max. decay

CR2: ATTENUATOR, DISCRIMINATOR, THRESHOLD, TEST AMPLITUDE CONTROL REGISTER

msb														lsb
At2	At1	Vt6	Vt5	Vt4	Vt3	Vt2	Vt1	Ta7	Ta6	Ta5	Ta4	Ta3	Ta2	Ta1

At2	MSB, C-R attenuator, 00= no atten, 01=1/3 atten, 10=1/9 atten
At1	LSB, C-R attenuator, 00= no atten, 01=1/3 atten, 10=1/9 atten
Vt6	MSB discriminator voltage threshold DAC input, 111111 = min threshold
Vt5	5SB discriminator voltage threshold DAC input
Vt4	4SB discriminator voltage threshold DAC input
Vt3	3SB discriminator voltage threshold DAC input
Vt2	2SB discriminator voltage threshold DAC input
Vt1	LSB discriminator voltage threshold DAC input
Ta7	MSB Test Pulse Amplitude DAC input, 1111111 = 127 fC
Ta6	6SB Test Pulse Amplitude DAC input
Ta5	5SB Test Pulse Amplitude DAC input
Ta4	4SB Test Pulse Amplitude DAC input
Ta3	3SB Test Pulse Amplitude DAC input
Ta2	2SB Test Pulse Amplitude DAC input
Ta1	LSB Test Pulse Amplitude DAC input

CR3: CHANNEL DISABLE, ANALOG OUTPUT MUX SELECT AND FEEDBACK VOLTAGE CONTROL REGISTER

msb																									lsb
D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	M5	M4	M3	M2	M1	F6	F5	F4	F3	F2	F1

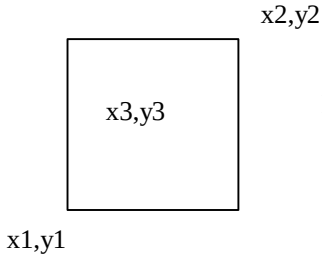
D16	MSB, channel 16, 0=enable, 1= disable
D15 – D2	15SB – 2SB , channel 15 – channel 2 , 0= enable, 1 = disable
D1	LSB, channel 1
M5	Mux enable/disable bit, 0=enable, 1=disable
M4	MSB, analog output mux address, 1111 = channel 16 select
M3	3SB analog output mux address
M2	2SB analog output mux address
M1	LSB analog output mux address
F6	MSB, Vfb DAC input, 11111 = 2.5v
F5	5SB, Vfb DAC input
F4	4SB, Vfb DAC input
F3	3SB Vfb DAC input
F2	2SB Vfb DAC input
F1	LSB Vfb DAC input

APPENDIX 5: PAD DIMENSIONS FOR THE TGL98.V2 CHIP

Pad dimensions for the TGL98 chip

Chip BoundBox [(0,0), (6224,6224)] = SW co-ords & NE co-ords

lambda 0.6
Note: All dimensions are with reference to the SW most corner of the chip



INDIVIDUAL PAD REFERENCES

pin name	pin no.	Side	pad SW co-ords in microns (x1, y1)	pad NE co-ords in microns (x2, y2)	pad center co-ords in microns (x3, y3)
$Vin16	1	W	(6.6, 290.4)	(94.2, 378)	(50.4, 334.2)
$Vin15	2	W	(6.6, 459.6)	(94.2, 547.2)	(50.4, 503.4)
$Vin14	3	W	(6.6, 631.2)	(94.2, 718.8)	(50.4, 675)
$Vin13	4	W	(6.6, 800.4)	(94.2, 888)	(50.4, 844.2)
$Vin12	5	W	(6.6, 972)	(94.2, 1059.6)	(50.4, 1015.8)
$Vin11	6	W	(6.6, 1141.2)	(94.2, 1228.8)	(50.4, 1185)
$Vin10	7	W	(6.6, 1312.8)	(94.2, 1400.4)	(50.4, 1356.6)
$Vin9	8	W	(6.6, 1482)	(94.2, 1569.6)	(50.4, 1525.8)
$Vin8	9	W	(6.6, 1653.6)	(94.2, 1741.2)	(50.4, 1697.4)
$Vin7	10	W	(6.6, 1822.8)	(94.2, 1910.4)	(50.4, 1866.6)
$Vin6	11	W	(6.6, 1994.4)	(94.2, 2082)	(50.4, 2038.2)
$Vin5	12	W	(6.6, 2163.6)	(94.2, 2251.2)	(50.4, 2207.4)
$Vin4	13	W	(6.6, 2335.2)	(94.2, 2422.8)	(50.4, 2379)
$Vin3	14	W	(6.6, 2504.4)	(94.2, 2592)	(50.4, 2548.2)
$Vin2	15	W	(6.6, 2676)	(94.2, 2763.6)	(50.4, 2719.8)
$Vin1	16	W	(6.6, 2845.2)	(94.2, 2932.8)	(50.4, 2889)
$V1	20	N	(290.4, 3640.2)	(378, 3727.8)	(334.2, 3684)
$gnd1	21	N	(460.2, 3640.2)	(547.8, 3727.8)	(504, 3684)
$THR_bias	23	N	(800.4, 3640.2)	(888, 3727.8)	(844.2, 3684)
$V2	24	N	(972, 3640.2)	(1059.6, 3727.8)	(1015.8, 3684)
$gnd2	25	N	(1141.8, 3640.2)	(1239.4, 3727.8)	(1185.6, 3684)
$AO	26	N	(1312.8, 3640.2)	(1400.4, 3727.8)	(1356.6, 3684)
$RSTS1_adj	28	N	(1653.6, 3640.2)	(1741.2, 3727.8)	(1697.4, 3684)
$RSTS2_adj	29	N	(1822.8, 3640.2)	(1910.4, 3727.8)	(1866.6, 3684)
$OS	30	N	(1994.4, 3640.2)	(2082, 3727.8)	(2038.2, 3684)
$SAD	31	N	(2163.6, 3640.2)	(2251.2, 3727.8)	(2207.4, 3684)
$SOE	32	N	(2335.2, 3640.2)	(2422.8, 3727.8)	(2379, 3684)
$RD_SC	33	N	(2504.4, 3640.2)	(2592, 3727.8)	(2548.2, 3684)
$TP_SL	34	N	(2676, 3640.2)	(2763.6, 3727.8)	(2719.8, 3684)
$SI	35	N	(2845.2, 3640.2)	(2932.8, 3727.8)	(2889, 3684)

$SO	36	N	(3016.8, 3640.2)	(3104.4, 3727.8)	(3060.6, 3684)
$V3	37	N	(3186, 3640.2)	(3273.6, 3727.8)	(3229.8, 3684)
$gnd3	38	N	(3357, 3640.2)	(3445.2, 3727.8)	(3400.8, 3684)
$Vfb(PAD)	39	E	(3640.2,3357.6)	(3727.8,3445.2)	(3864, 3401.4)
$OS_bias	40	E	(3640.2, 3186)	(3727.8, 3273.6)	(3684, 3229.8)
$OR	41	E	(3640.2, 3016.8)	(3727.8, 3104.4)	(3684, 3060.6)
$Iout1	42	E	(3640.2, 2845.2)	(3727.8, 2932.8)	(3684, 2889)
$Iout2	43	E	(3640.2, 2676)	(3727.8, 2763.6)	(3684, 2719.8)
$Iout3	44	E	(3640.2, 2504.4)	(3727.8, 2592)	(3684, 2548.2)
$Iout4	45	E	(3640.2, 2335.2)	(3727.8, 2422.8)	(3684, 2379)
$Iout5	46	E	(3640.2, 2163.6)	(3727.8, 2251.2)	(3684, 2207.4)
$Iout6	47	E	(3640.2, 1994.4)	(3727.8, 2082)	(3684, 2038.2)
$Iout7	48	E	(3640.2, 1822.8)	(3727.8, 1910.4)	(3684, 1866.6)
$Iout8	49	E	(3640.2, 1653.6)	(3727.8, 1741.2)	(3684, 1697.4)
$Iout9	50	E	(3640.2, 1482)	(3727.8, 1569.6)	(3684, 1525.8)
$Iout10	51	E	(3640.2, 1312.8)	(3727.8, 1400.4)	(3684, 1356.6)
$Iout11	52	E	(3640.2, 1141.2)	(3727.8, 1228.8)	(3684, 1185)
$Iout12	53	E	(3640.2, 972)	(3727.8, 1059.6)	(3684, 1015.8)
$Iout13	54	E	(3640.2, 800.4)	(3727.8, 888)	(3684, 844.2)
$Iout14	55	E	(3640.2, 631.2)	(3727.8, 718.8)	(3684, 675)
$Iout15	56	E	(3640.2, 459.6)	(3727.8, 547.2)	(3684, 503.4)
$Iout16	57	E	(3640.2, 290.4)	(3727.8, 378)	(3684, 334.2)
$gnd3a	58	S	(3357, 6.6)	(3444.6, 94.2)	(3400.8, 50.4)
$V3a	59	S	(3187.2, 6.6)	(3274.8, 94.2)	(3231, 50.4)
$V2I_bias	60	S	(3015.6, 6.6)	(3103.2, 94.2)	(3059.4, 50.4)
$A5	61	S	(2846.4, 6.6)	(2934, 94.2)	(2890.2, 50.4)
$A4	62	S	(2674.8, 6.6)	(2762.4, 94.2)	(2718.6, 50.4)
$A3	63	S	(2505.6, 6.6)	(2593.2, 94.2)	(2549.4, 50.4)
$A2	64	S	(2334, 6.6)	(2421.6, 94.2)	(2377.8, 50.4)
$A1	65	S	(2164.8, 6.6)	(2252.4, 94.2)	(2208.6, 50.4)
$A0	66	S	(1993.2, 6.6)	(2080.8, 94.2)	(2037, 50.4)
$DA12_bias	68	S	(1652.4, 6.6)	(1740, 94.2)	(1696.2, 50.4)
$gnd2a	69	S	(1482.6, 6.6)	(1570.2, 94.2)	(1526.4, 50.4)
$V2a	70	S	(1311.6, 6.6)	(1399.2, 94.2)	(1355.4, 50.4)
$S2_bias	71	S	(1142.4, 6.6)	(1230, 94.2)	(1186.2, 50.4)
$VM	72	S	(970.8, 6.6)	(1058.4, 94.2)	(1014.6, 50.4)
$S1_bias	74	S	(630, 6.6)	(717.6, 94.2)	(673.8, 50.4)
$gnd1a	75	S	(460.2, 6.6)	(547.8, 94.2)	(504, 50.4)
$V1a	76	S	(289.2, 6.6)	(376.8, 94.2)	(333, 50.4)