

## A Discriminator with a Current-Sum Multiplicity Output for the PHENIX Multiplicity Vertex Detector\*

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### Abstract

A current output multiplicity discriminator for use in the front-end electronics (FEE) of the Multiplicity Vertex Detector (MVD) for the PHENIX detector at RHIC has been fabricated in the a 1.2- $\mu\text{m}$  CMOS, n-well process. The discriminator is capable of triggering on input signals ranging from 0.25 MIP to 5 MIP. Frequency response of the discriminator is such that the circuit is capable of generating an output for every bunch crossing (105 ns) of the RHIC collider. Channel-to-channel threshold matching was adjustable to  $\pm 0.05$  MIP. One channel of multiplicity discriminator occupied an area of  $85 \mu\text{m} \times 630 \mu\text{m}$  and consumed  $515 \mu\text{W}$  from a single 5-V supply. Details of the design and results from prototype device testing are presented.

### I. INTRODUCTION

The PHENIX Multiplicity Vertex Detector (MVD) is the inner most detector of PHENIX. MVD consists of  $\sim 34,000$  channels used primarily to provide event characterization, a centrality trigger, the collision vertex position along the beams and the measurement of fluctuations in the charged particle distributions. The system has silicon strip detectors arranged in two concentric barrels around the beam pipe in the center of PHENIX and endcaps consisting of a single layer of silicon pad detectors. The front end electronics (FEE) are optimized for minimum size, power dissipation and cost, while the design allows for the unfolding of multiple particle hits in each silicon pixel.

Figure 1 depicts the system diagram for a single channel of the MVD front-end electronics (FEE). Each channel of MVD contains a charge sensitive preamplifier, analog memory units (AMUs), an 11-bit ADC and a multiplicity discriminator. By summing the outputs of many multiplicity discriminators, a value proportional to the number of colliding particles is created. This information aids in the generation of a Level-1 trigger [1,2].

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The high channel count coupled with the small physical area in which the FEE reside require a low-power, small-area, multiplicity discriminator implementation. A design goal of approximately  $500 \mu\text{W}/\text{channel}$  was established as an upper limit for power consumption. Additionally, due to detector pitch constraints, the discriminator (as well as all other MVD FEE) must be arrayable within an  $85 \mu\text{m}$  pitch.

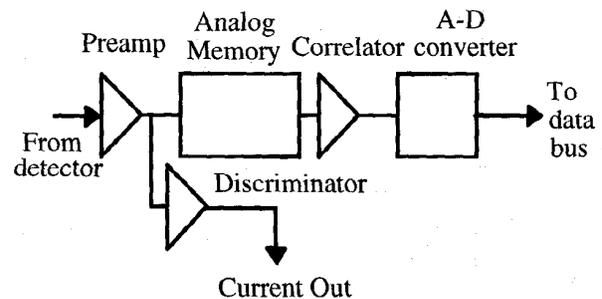


Figure 1: Block diagram of MVD FEE.

Another aspect of the high channel count is the need to have a common discriminator threshold setting for 32-channels of multiplicity discriminator located on a single die. This goal requires that the discriminator be extremely well matched over all process variations. For this reason, methods of offset elimination have been examined.

Timing constraints for the multiplicity discriminator are dictated by the RHIC bunch crossing interval, which has been established as 105 ns in order to achieve the highest possible luminosity. Within every 105 ns cycle, the discriminator is capable of providing valid event information.

### II. MULTIPLICITY DISCRIMINATOR DESIGN

Since the discriminator receives input signals directly from a charge sensitive preamplifier (gain equal to  $20 \text{ mV}/\text{fC}$ ), it must operate with step inputs. Each applied step consists of a fixed risetime pulse (60 ns) with varying amplitudes. Removing the long decay tail of the preamplifier signal requires differentiation. Passive and active differentiation topologies were both considered. Passive differentiation is easy to implement and well matched across channels. However, for the discriminator to be active during every bunch crossing, the differentiation time constant must be kept small

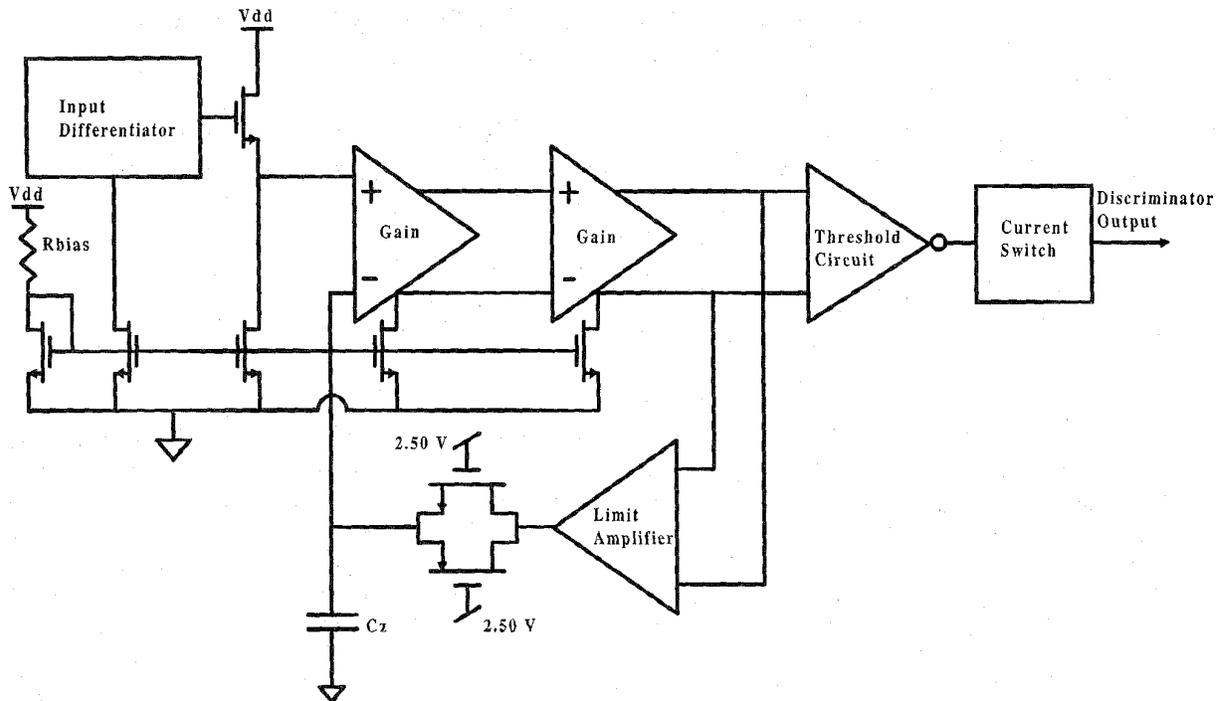


Figure 3: Complete diagram for 1 channel of multiplicity discriminator.

which leads to severe signal attenuation. Such high levels of signal attenuation place further constraints on the remaining circuitry. However, active differentiation provides an adequate frequency response as well as signal amplification.

Typical active differentiators utilizing operational amplifiers are inappropriate for this application because of size constraints. An acceptable compromise to the area, power, speed and matching specifications was selected and is shown in Figure 2. Devices M1 and M4 comprise a basic common-gate stage whose gain is given by

$$A_v = g_{m(\text{eff}(\text{M1}))} R_{DS(\text{M4})}. \quad (1)$$

Signal differentiation is achieved through the C-R network generated by the 0.50 pF capacitor and the relatively small resistance seen looking into the source of M1. M2 and M3 provide the necessary bias current for the differentiator. Through adjustment of the voltage applied to the gate of the M4 device biased in the ohmic region, the amount of signal gain may be varied.

The circuit of Figure 2 is especially susceptible to channel-to-channel mismatch resulting from random process variations. The major sources of error stem from the channel-to-channel variations produced by drain current mismatch in M2 and transconductance mismatch in M1. It has been shown that transconductance matching is directly proportional to the WL product [4]. Thus, maximizing the area of M1 minimizes the gain error associated with  $g_m$  mismatch. Transistors M2a and M2b provide a means by which the differentiator bias current can be varied from approximately 10  $\mu\text{A}$  to 20  $\mu\text{A}$  by turning n-channel switches, M2sa and M2sb, either on (logic high) or off (logic low). By adjusting the differentiator bias current for each channel, channel-to-channel mismatch can be reduced.

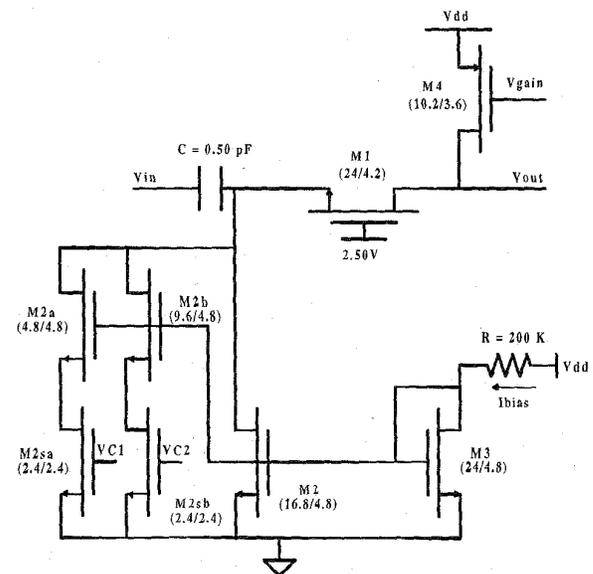


Figure 2: Input differentiator topology.

The remainder of the multiplicity discriminator, illustrated in the block diagram of Figure 3, consists of two gain stages, a dc feedback circuit to eliminate offsets, a threshold circuit, and an output current switch. Each gain stage is composed of a differential single-stage amplifier with a gain of 5 V/V.

After amplification, the resulting differential signal is applied to the threshold circuit of Figure 4. The threshold detect circuit of Figure 4 is similar to one described previously and channel-to-channel matching on the order of  $\pm 3$  mV has been observed [3,5].

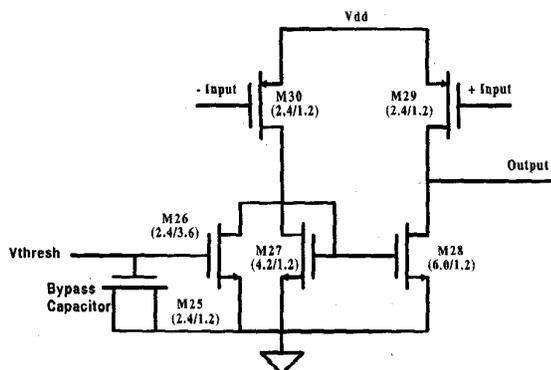


Figure 4: Threshold adjustment circuit.

Mismatch between the input devices of the gain stages introduces an offset voltage. Achieving the highest possible channel-to-channel matching requires dc feedback to eliminate this offset. Continuous dc feedback was selected to eliminate offsets because of the low event rate expected for the MVD.

To maintain circuit stability required implementation of an 8 pF hold capacitor within the dc feedback loop. A high density capacitor structure, whose cross-section is shown in Figure 5, facilitated inclusion of this large device while still maintaining the stringent area requirements of the discriminator. The capacitor combines the densities obtained by poly-poly and MOS capacitor structures. This combined density can approach 2 fF/μm<sup>2</sup> while maintaining a series resistance of less than 30 Ω.

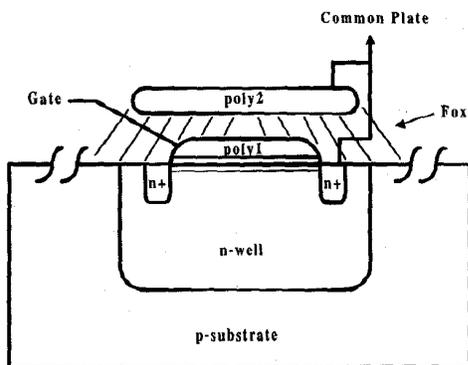


Figure 5: High density capacitor structure used to implement the 8 pF hold capacitor.

The final element required to implement the function of multiplicity discrimination is the current switch output circuit. To convert the output voltage into an acceptable current suitable for summing, the topology of Figure 6 was utilized. Transistors M1 - M4 comprise the bias and reference voltage common to 32-channels of discriminator. When the discriminator triggers (logic low), M6 turns on and allows a nominal current of 30 μA to flow through M5 and onto the current summing bus.

### III. RESULTS

An 8-channel prototype version of the multiplicity discriminator proposed for use within the MVD was evaluated based on the system requirements previously discussed. One

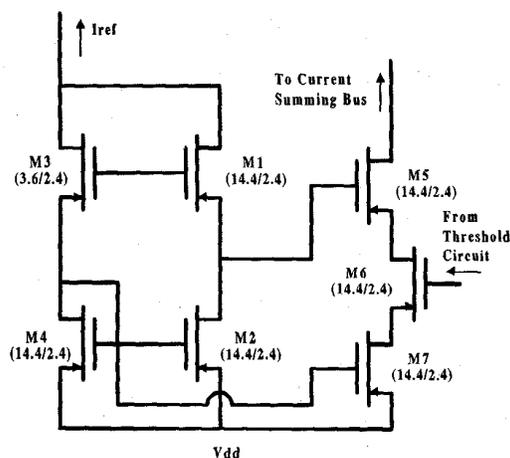


Figure 6: Output current switch topology.

channel occupied an area of 85 μm x 630 μm and consumed roughly 515 μW from a single 5-V supply.

The multiplicity discriminator was tested with a 60 ns risetime signal supplied from a LeCroy 9210 pulse generator. As shown in Figure 7, the discriminator was capable of triggering on 20-mV input signals while providing an appropriate timing response. Additionally, through proper manipulation of the input differentiator gain adjustment and the threshold adjustment, the discriminator could be adjusted such that inputs greater than 450 mV were required to trigger the circuit. The graph of Figure 8 illustrates the triggering characteristics of the discriminator for various settings of these externally adjustable bias voltages.

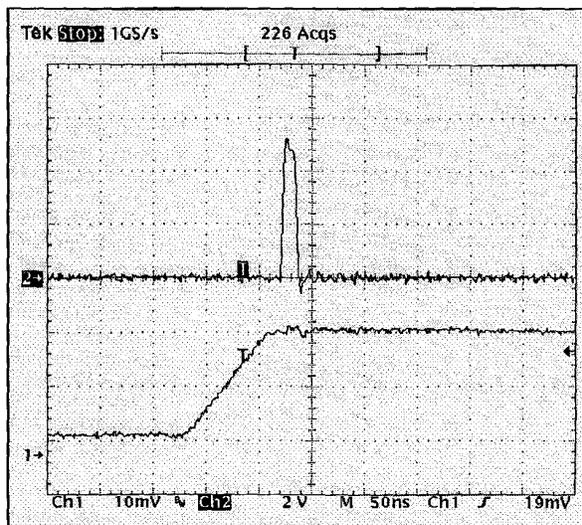


Figure 7: Sample discriminator output.

Two methods were used to evaluate the channel-to-channel matching characteristics. The first evaluation of the discriminator threshold matching characteristics was performed with a fixed input differentiator bias current of 18 μA. The average threshold voltage mismatch for the 5 prototype chips tested was ± 8.1 mV. The alternative evaluation utilized the individual channel current adjustment illustrated in Figure 2. Implementation of this adjustment

resulted in a reduction of channel-to-channel mismatch to  $\pm 4.2$  mV. Table 1 provides a comparison of the threshold mismatch with and without adjustment for the 5 sample chips.

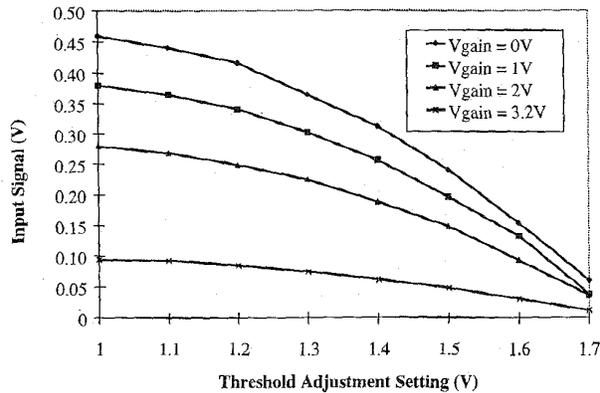


Figure 8: Input required to trigger discriminator as a function of gain and threshold setting.

Table 1.

Threshold mismatch of prototype chips with and without adjustment.

Chip	Threshold Matching without Adjustment	Threshold Matching with Adjustment
1	$\pm 7.75$ mV	$\pm 3$ mV
2	$\pm 5.25$ mV	$\pm 4$ mV
3	$\pm 9.25$ mV	$\pm 5$ mV
4	$\pm 7$ mV	$\pm 4.5$ mV
5	$\pm 11.25$ mV	$\pm 4.5$ mV
Average	$\pm 8.1$ mV	$\pm 4.2$ mV

#### IV. CONCLUSIONS

A small area, arrayable multiplicity discriminator suitable for use in the MVD at RHIC has been presented. This circuit provides a highly flexible design which allows for compensation of random processing mismatch over multiple channels. The circuit establishes a low-power, small-area means of direct integration with a charge sensitive preamplifier.

#### V. ACKNOWLEDGMENTS

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#### VI. REFERENCES

- [1] Kehoe, W. L., et al., PHENIX Conceptual Design Report, 29 Jan. 1993.
- [2] Britton, C. L., et al., "Low Noise, Low Power Dissipation LSI Electronics for Heavy Ion Detectors". *Conference Record of 1996 IEEE International Symposium on Circuits and Systems*, Vol. 1, pp. 133-136.
- [3] Simpson, M. L., et al., "A Monolithic, Constant-Fraction Discriminator Using Distributed R-C Delay Line Shaping,"

*IEEE Transactions on Nuclear Science*, Vol. 43, No. 3, June 1996, pp. 1695-1699.

- [4] Lakshmikummar, K. R., et al., "Characterization and Modeling of Mismatch in MOS Transistors for Precision Analog Design," *IEEE Journal of Solid-State Circuits*, Vol. SC-21, No. 6, December 1986.
- [5] Smith, R. S., "Development of a Multiplicity Discriminator for High Energy Physics Experiments," Masters Thesis, University of Tennessee, Knoxville, December 1996.