

Mixed Signal Custom Integrated Circuit Development for Physics Instrumentation

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ABSTRACT

The Monolithic Systems Development Group at the Oak Ridge National Laboratory has been greatly involved in custom mixed-mode integrated circuit development for the PHENIX detector at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory and position-sensitive germanium spectrometer front-ends for the Naval Research Laboratory (NRL). This paper will outline the work done for both PHENIX and the Naval Research Laboratory in the area of full-custom, mixed-signal CMOS integrated electronics.

The PHENIX detector is a large multi-component detector at the Relativistic Heavy Ion Collider (RHIC) at Brookhaven National Laboratory. PHENIX has over 400,000 channels of electronics, most of which is implemented using custom integrated circuits. We presently have responsibility for developing and manufacturing electronics for the event vertex-finding subsystem, the pads tracking subsystem, the electromagnetic calorimeter subsystem, and the muon tracking/identification subsystems. We have developed an architecture utilizing simultaneous read-write analog memories used throughout the detector that allows data to be continuously taken even during event readout (a deadtime-less system). The manufacturing technologies being used range from multi-layer printed-circuit boards to multi-layer, multi-chip modules (MCMs).

The germanium spectrometer electronics for the Naval Research Laboratory consist of low-noise preamplifier-shapers-peak stretchers and discriminators. The preamplifiers have been optimized for detector capacitances of approximately 10 pF and shaping times of 5-10 μ s.

This paper will present the architectures chosen for the various PHENIX detectors which include position-sensitive silicon, capacitive pixel, and phototube detectors, and performance results for the subsystems as well as a system description of the NRL germanium strip system and its performance. The performance of the custom preamplifiers, discriminators, analog memories, analog-digital converters, and control circuitry for all systems will be presented.

Keywords: Physics, electronics, CMOS

1. PHENIX

The PHENIX Detector, shown in Fig. 1, consists of three magnets (1 Central and 2 Muon) and four instrumented spectrometers or *arms*. The East and West *CENTRAL ARMS* (inner detectors, tracking system, ring imaging Cherenkov detector, time-of-flight system, and electromagnetic calorimeters) are instrumented to detect electrons, photons, and charged hadrons. The North and South *MUON ARMS* are instrumented with tracking chambers and particle identifiers to detect muons. At least three upgrade options are under consideration.

The Inner detectors consist of the beam-beam counter and the Multiplicity-Vertex Detector (MVD). The tracking system consists of drift chambers, pad chambers, and the time-expansion chamber. Moving outward there are the Ring-Imaging Cherenkov Detector (RICH), Time-of-flight (TOF) system, electromagnetic calorimeter (EmCal), and the muon arm (tracking

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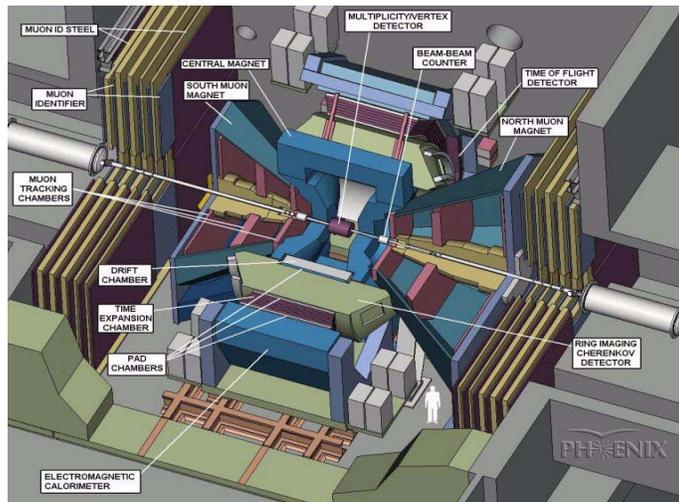


Figure 1. PHENIX detector

and particle ID). In all, there are approximately 400,000 channels of electronics, 325,000 of which ORNL has responsibility for the associated integrated circuits.

1.1 PHENIX Subsystems

1.1.1 MVD

The requirements of low-power consumption, small physical area, a channel count of approximately 34,000, and flexible data handling make the MVD of the PHENIX detector at RHIC one of the most challenging of the PHENIX detector subsystems [1]. Additional requirements, which include a minimum 10:1 system signal-to-noise ratio for a single Minimum Ionizing Particle (MIP) signal (which results in noise less than 2500 electrons rms) and discrimination of a 0.25 MIP event for the per-channel multiplicity discriminator, offer yet further challenges.

The MVD is a 2-layer barrel detector comprised of 112 silicon strip detectors and 2 disk-shaped end caps comprised of 24 wedge-shaped pad detectors. Each detector is made up of 256 individual strips and connects to a single 1.96" x 1.76" Multi-Chip Module (MCM). Each MCM comprises eight tgv32 32-channel preamplifier chips, eight 32-channel analog memory/analog-digital converter chips (AMUADC), two programmable Xilinx control chips, and a summing opamp for the trigger sum. A block diagram of a single channel is shown in Fig. 2. The detector is a clam-shell design constructed in two halves to close about the beam pipe. The main physics goals of the detector are to provide a multiplicity measurement to the PHENIX Level-1 trigger, and to reconstruct the collision vertex to better than 2 mm.

There are a variety of silicon readout systems in the literature. The majority of systems read out events on the silicon strips with a preamplifier and discriminator and some newer systems are planning to use analog readout. The MVD readout is a

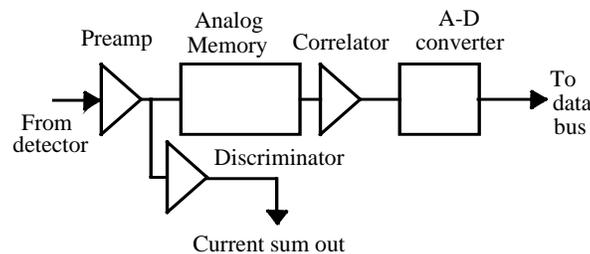


Figure 2. Block diagram of one MVD channel

hybrid of both. It uses analog information for the primary vertex-finding information and a discriminator for the multiplicity information. The two custom chips on the MVD will be described separately.

1.1.1.1 Thin Glenn Vertex (Tgy32)

A block diagram of two channels of the Thin Glenn preamplifier is shown in Fig. 3. This includes the preamplifier, discriminator[2], current-sum output bus, and individual channel adjustments such as the calibration, noisy-channel disable, and discriminator offset adjustment. Each function of each channel is individually programmable through the use of a serial data string. Five 6-bit digital-analog converters (DAC) [3] are used to program calibration voltages, feedback resistor control voltages, discriminator threshold voltages, discriminator dynamic range, and discriminator bias. A serial string 190 bits long is required to fully program the preamplifier chip. The entire serial string can be read back for verification without affecting the programmed values.

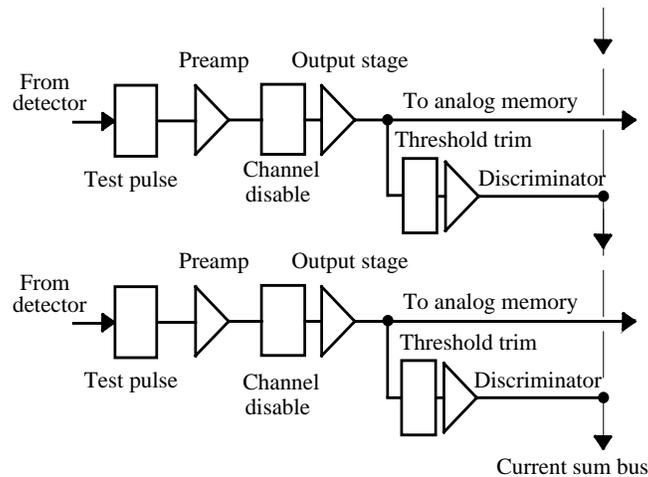


Figure 3. Two-channel block diagram

The preamplifier [1], whose block diagram is presented in Fig. 4, utilizes an active PMOS cascode amplification stage for maximum dynamic range. Signal-to-noise optimization is accomplished by varying the value of preamplifier feedback resistor because ac-coupled detectors with polysilicon bias resistors are being used in the MVD. The feedback resistor is a long-channel PMOS device that is adjusted by another serially programmed DAC. The adjustable range of the resistor-capacitor RC time constant is from infinity to 500 ns.

The test pulse is accomplished by switching a capacitor between a voltage supplied by a DAC and the preamplifier +5 V supply. This difference allows each channel to be tested with a programmable analog voltage. The test pulse will enable outputs as great as 5 MIPs.

In this design, the feedback capacitor is split into two parts, Cf1 and Cf2, as shown in Fig. 4. Capacitor Cf1 is connected from the input to the dominant node. The other capacitor Cf2 is connected from the input to a source follower output. The second stage voltage amplifier also has two input capacitors, one from each node. Proper sizing of the four capacitors allows the gain and compensation of the linear chain to be adjusted almost independently.

The multiplicity discriminator [1, 2], whose block diagram is shown in Fig. 5, is used to determine the presence of an event above threshold on each channel. The current-mode outputs of 256 discriminators (eight chips) are summed to produce a multiplicity output whose amplitude is proportional to the number of fired discriminators. The design allows triggering at every beam crossing (105 ns) with no deadtime. The threshold for all 32 channels on one chip is set by a DAC-supplied voltage and the threshold range (the maximum and minimum values of the threshold) is set by another DAC. Because these two DACs control all 32 channels at once, channel-channel variations in input offset voltage are adjusted by a 2-bit fine adjustment which is serially programmed. Some of the basic performance parameters are listed in Table 1. The tgy32 die size is 4.1 mm X 4.6 mm.

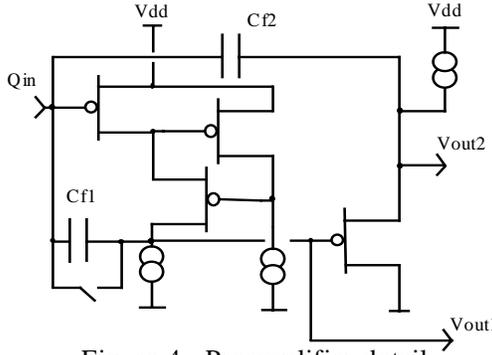


Figure 4. Preamplifier detail

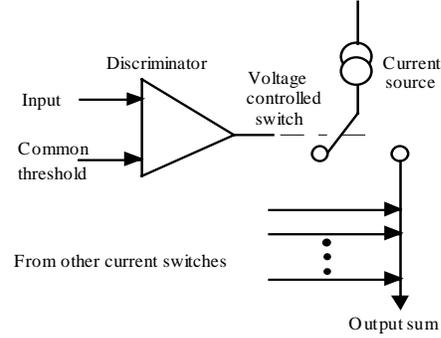


Figure 5. Discriminator block diagram

Table 1. tgv32 basic performance parameters

Parameter	Value
Noise	660 + 75 e/pF
Power dissipation	1.7 mW/channel
Risetime (0 pF)	20 ns
Risetime (13 pF)	40 ns
Minimum Threshold	20 mV (1/4 MIP)
Maximum threshold	~ 400 mV (5 MIP)
Maximum signal	~ 1.5 V (19 MIP)

1.1.1.2 AMUADC

Fig. 6 shows a block diagram of the AMU-ADC. It consists of 32 parallel analog memory pipes, each pipe 64 cells deep. Each memory cell contains a 0.5 pF capacitor, which stores the sampled input analog voltage, and read and write switches that connect the memory capacitor to either the Read amplifier or input signal, respectively. The output of each pipe is buffered through a Read amplifier to drive its corresponding ADC channel. The AMU can be either directly read into the ADC or any two AMU cells on all channels can be subtracted by the double-correlated sampler present on each channel.

The Wilkinson topology ADC [4] requires two analog references for its conversion process, V_{REF} (reference voltage) and I_{REF} (reference current). V_{REF} sets the beginning voltage for the ramp waveform, and I_{REF} controls the slew rate of the ramp. Both references are supplied using on-chip programmable digital-to-analog converters (DACs). A third on-chip DAC provides the Correlator reference voltage.

True pipeline operation is enabled by the use of a buffer register located at the output of each ADC channel. This allows a new cell address to be read out to the ADC input and begin a new conversion at the same time that the previous result is being read out of the ADC.

The ADC section operates in either 12-, 11-, 10-, or 9-bit conversion modes. Although a user requiring lower precision could choose 12-bit conversions and simply truncate unnecessary bits, selecting a lower resolution significantly decreases the total conversion time. Equation (1) represents the time t_{conv} needed by the ADC section to perform a conversion. The variable n is the number of desired bits, f is the ADC clock frequency, and T_{oh} is time needed for setup overhead. The variable n is the

$$t_{conv} = \frac{2^{n-1}}{f} + T_{oh} \quad (1)$$

number of bits used in the conversion and would be either 9, 10, 11, or 12. The exponent is $n-1$, instead of n , because the counter circuit counts on both the rising and falling clock edges thereby reducing the time required by a factor of 2. This imposes a requirement for a 50% duty cycle clock to ensure equal bin width and good differential nonlinearity (DNL). The maximum measured clock frequency for the prototype chips has averaged 230 MHz.

The overhead time T_{oh} includes several signals needed to initialize the ADC, but is actually dominated by the settling time needed for the AMU readout amplifier. Two ADC signals, Auto-Zero (AZ) and the Internal Comparator Switch (ICS),

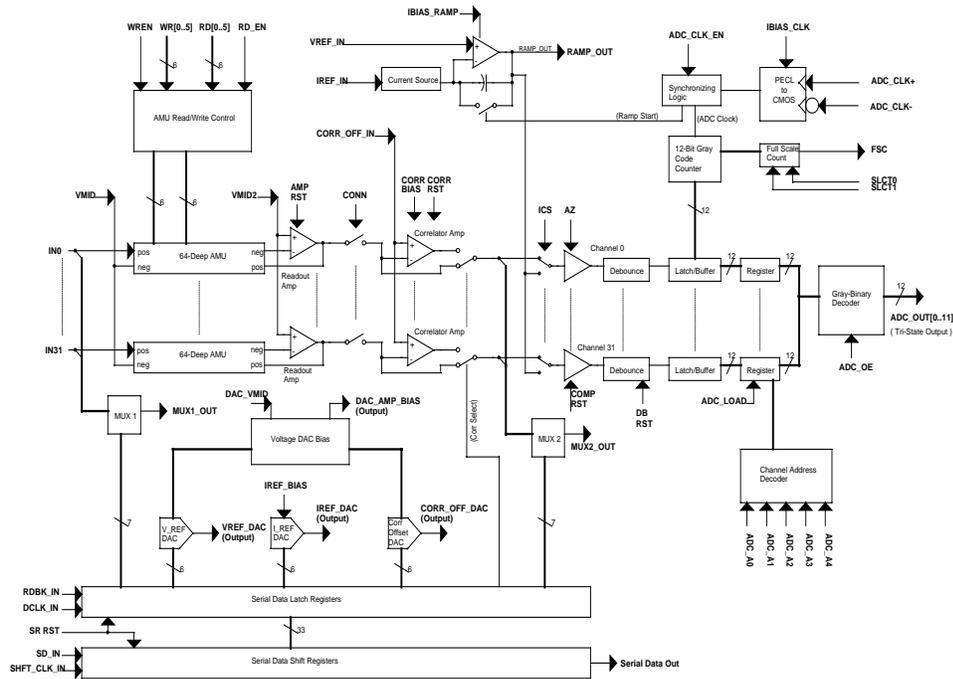


Figure 6. AMU ADC block diagram

control CMOS switches used to pre-charge capacitors in the comparator circuits. The duration of the AZ and ICS signals must be sufficiently long to fully charge the capacitors due to the finite resistance of the switches and the resulting R-C time constant. Each of these require at least 100 ns for 12-bit accuracy. General performance parameters are shown in Table 2.

1.1.2 PAD Chamber

The PHENIX PC subsystem consists of three sections, PC1, PC2 and PC3, with an east and west arm for each section. These three tracking detector sections are each positioned at different radial distances from the collision vertex. The PC subsystem accounts for 207,360 of the approximately 400,000 detector channels in PHENIX.

Since the PC tracking detectors are sandwiched between multiple calorimeters, it is important that the PC's radiation absorption be as low as possible, to avoid energy measurement degradation in adjoining calorimeters. Additionally, the large number of PC detector elements preclude bringing pad wire connections outside the detector's active region. This requires the PC front-end electronics be mounted within the PC detector's active region. A minimum density packaging scheme is applied to the entire front-end electronics. In the following section, PC front-end electronics architecture is described. Following this architectural description and the custom integrated circuit requirements is given.

Table 2. AMUADC chip performance parameters

<i>Parameter</i>	<i>Value</i>
Input range	0.25V – 4.75V
AMU writing rate	10 MHz
Power dissipation	12 mW + 3.6 μ W/MHz/channel
Clock rate	40 MHz – 200 MHz
Conversion time	$2.5 \mu\text{s} + (2^{n-1})/f_{\text{clock}}$ (n=# of bits)
INL (12 bit)	0.04%
INL (10 bit with correlator)	0.2%
DNL (12 bit)	130%
DNL (11 bit)	70%
DNL (10 bit)	80%
Gain	1 V/V

1.1.2.1 PC Front-End Electronics Architecture

A typical PC front-end electronic channel consists of a charge sensitive preamplifier, signal differentiator, leading edge discriminator, beam crossing sampler and delay memory unit (DMU). The DMU delays and holds the pixel state until the PHENIX trigger system signals for event readout. A PC TGLD channel block diagram is shown in Fig. 7. In addition to these TGLD operational functions, on-chip control and testing functions are included to allow remote control and evaluation of front-end electronics operational status while sealed inside the experiment after installation.

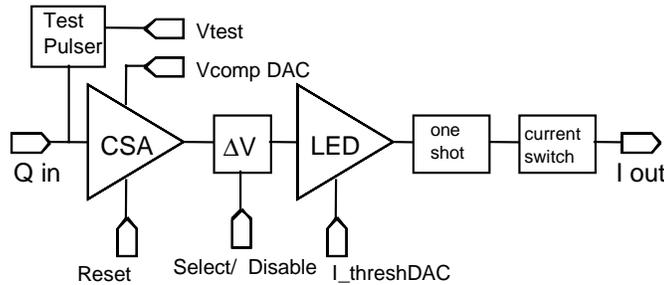


Figure 7. Single Channel Block Diagram of PC TGLD

Three bare die TGLD, one DMU and three RS-485 interface chips are mounted chip-on board to form a 48 channel readout card (ROC). Each PC detector subpanel has 45 ROCs arranged as five rows with nine ROCs each, for 2160 channels of pad readout. These 2160 channels of pad readout are controlled by a front-end module that interfaces with the PHENIX on-line data acquisition system.

1.1.2.2 Charge Sensitive Preamp Design

The PC charge sensitive preamplifier, which is similar to that mentioned in the *tg32* section, was designed for positive charge input with a gain of 10mV/fC. The preamp consists of two stages. The first stage, is a charge to voltage amp with a gain of -2.5mV/fC. The second stage is a voltage amp with a gain of -4V/V. The first stage is composed of an inverting, single gain stage, cascode amplifier followed by a non-inverting, level shifting buffer stage with a combined 0.4pF double polysilicon feedback capacitor. The feedback capacitor is split between the output of the cascode amp and the output of the common drain, level shifting buffer. The feedback capacitor can be reduced to 0.2pF to increase the charge gain to -5mV/fC if higher charge amplification is required. This first stage input is referenced to the positive power supply rail and its output swings towards the negative rail for positive input charges.

The second stage is an inverted version of the first stage with a combined 0.8pF input coupling capacitor and a 0.2pF feedback capacitor producing a -4V/V gain. This inverting voltage amp is referenced to the negative power supply rail and swings towards the positive supply for negative input voltages.

The PHENIX timing and control system generates experiment wide reset signals every millisecond. An internal digital delay generator generates carefully timed multi-phase reset signals to the TGLD preamp to prevent transient off-set voltages induced by reset switch charge injection. The differentiator and discriminator outputs are also disabled during this reset period to avoid spurious outputs to the DMU.

1.1.2.3 Differentiator and Discriminator Design

The preamp is followed by a passive CR differentiation stage composed of a 1 pF poly-poly capacitor and a 140K poly resistor connected to a midpoint voltage of 2.5V. The differentiated signal is passed into the discriminator. Fig. 8 shows the schematic of the CR differentiator and discriminator.

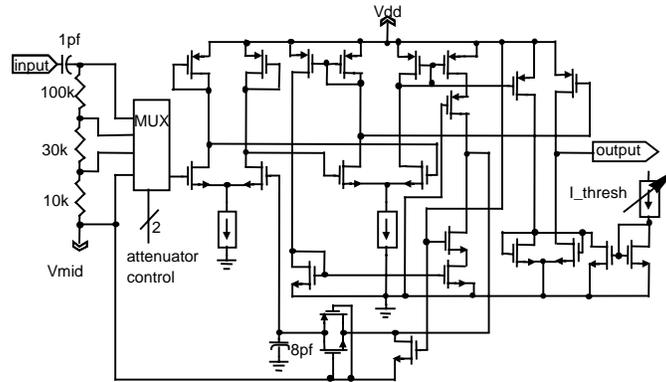


Figure 8. TGLD Differentiator and Discriminator

The discriminator block consists of two stages of differential amplifiers that give a net gain of 10. A third stage converts the output from the differential amplifier to a single ended output. This is fed back to the first differential stage negative input to form a DC stabilization feedback loop. It sets the reference for the first stage. The output of the second stage differential amplifier feeds the inputs of a differential voltage comparator stage. A mismatched current mirror load causes off-set bias currents in the comparator which controls the discriminator's threshold. The comparator's offset current is adjusted by robbing current from the over biased side of the differential circuit to provide a 4:1 discriminator threshold adjustment range. A six bit, on-chip, current DAC [3] connected to an inverting current mirror pulls current from the mismatched current mirror load of the comparator stage.

To achieve the necessary threshold adjustment range for PC1 minimum sensitivity and PC3 maximum insensitivity, the 140K poly resistor of the CR differentiator is divided into three sections forming a three step attenuator. Taps of 1/1, 1/3 and 1/9 attenuation factors scale the discriminator input. The taps are chosen to ensure that the 3 different threshold adjustment ranges overlap. Combining selectable CR differentiator taps and adjustable discriminator off-set currents gives discontinuous but adjustable threshold settings from approximately 1.5fC to 90fC for a dynamic range of 60:1.

The discriminator output is passed through a one-shot that produces fixed 150ns pulse width outputs. The one-shot output switches a 50uA current source on and off to interface with the DMU. Switched current source outputs minimize both output voltage swings and signal coupling back to the inputs. The chip also generates a 25uA fixed reference current for the DMU input stages.

1.1.3 EM Calorimeter

A four-channel multi-function integrated circuit designated as the MONDO Chip has been developed for the PHENIX electromagnetic calorimeter. The calorimeter is used for both energy measurements and particle identification. There are actually two types of electromagnetic calorimeters – one using lead glass modules and the other using lead and scintillating fibers. From an electrical signal viewpoint, the only difference is the pulse from the lead-scintillator calorimeter is faster than that from the lead-glass calorimeter.

The general scheme of the electromagnetic calorimeter (EmCal) front end electronics is shown in Fig. 9. Each photomultiplier tube (PMT) is connected to a passive integrator circuit by a short (< 1m) coaxial cable, and this circuit is connected in turn to the inputs of the MONDO chip. The MONDO Chip contains an energy measurement channel, and a

timing measurement channel. It also forms several types of analog energy sums which are used in the experiment trigger. The energy and timing outputs of the MONDO chip are sampled at the bunch crossing rate (9.4 MHz) by an analog memory (AMU). Upon receipt of a level-1 trigger, the appropriate samples are read from the AMU and digitized by a multi-channel ADC. The analog energy sums are converted to a digital format either through multi-level discriminators contained in the MONDO chip or by an external FADC. This trigger data is sent to the level-1 trigger logic.

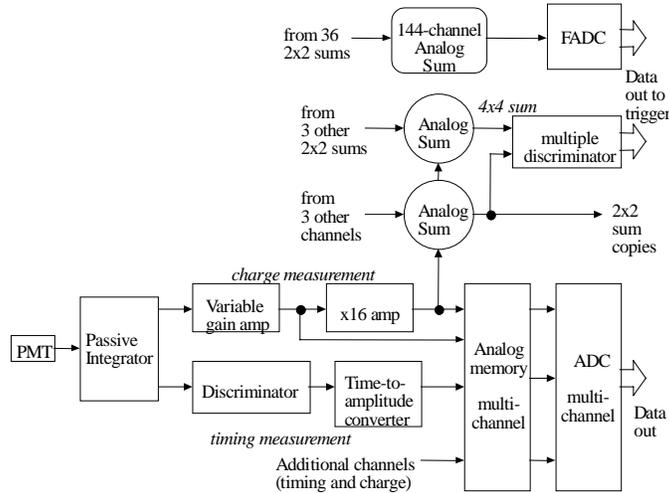


Figure 9: EmCal front end electronics block diagram.

A single channel of the MONDO Chip is shown in greater detail in Figure 10. The passive integrator provides two inputs to the MONDO Chip. The energy input is the integral of the charge delivered by the PMT. The charge is converted to a voltage by the 510-pF capacitor and that voltage is in turn amplified by the amplifiers of the energy channel. The timing input is the differential voltage across the 50-Ω resistor. The integrator is continuously reset by the 100-kΩ resistor.

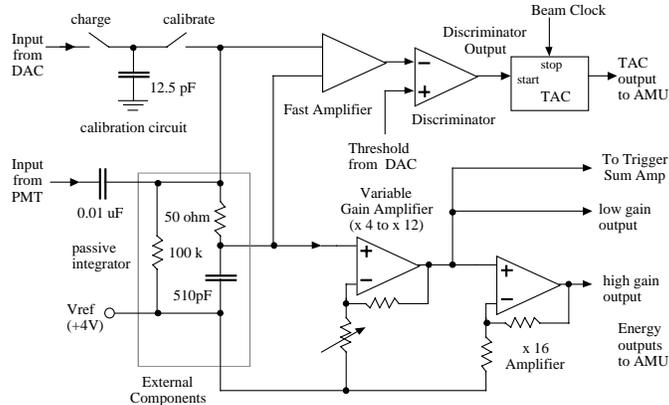


Figure 10: Single channel circuit diagram.

The energy channel consists of two wideband voltage amplifiers. The low-gain output is produced by the variable gain amplifier (VGA). The VGA equalizes the gains of different channels prior to forming analog energy sums, and its gain is programmable over a 3:1 range using a 5-bit digital control. Prototypes of this circuit have been described in detail earlier [5]. The energy channel use double correlated sampling to correct any change in the signal baseline due to previous events and achieves a 14-bit dynamic range for a full scale input of 500 pC.

The timing channel uses a constant fraction discriminator (CFD) and time-to-amplitude converter to measure the time of the input pulse relative to the next beam clock. A pulse exceeding the CFD threshold fires the CFD which in turn starts the TAC. The next rising edge of the beam clock (106 ns period) stops the TAC. The TAC output settles for one beam clock before being sampled and reset. The entire process uses three beam clocks cycles, so there is a dead time of two cycles. Since the lead-glass and the lead-scintillator calorimeters have considerably different pulse shapes, a different CFD is used for each, and there are actually two variants of the MONDO Chip. The lead-scintillator CFD was developed for PHENIX [6], while

the lead-glass is similar to that used for the WA98 lead-glass calorimeter [7]. Both discriminators include a switch to allow use in leading edge mode. The TAC circuit is also similar to that used for WA98, but was adapted for use in PHENIX. The timing channel full scale range is 100 ns with a least count of 50 ps and an uncertainty on the order of 200 ps rms for signals above 100 mV in amplitude.

A calibration circuit is included with each channel. This circuit allows injecting a charge programmable from 0 to 50 pC into the passive integrator (the timing input of the chip). This allows testing the basic functions of the energy, timing and trigger circuits.

Figure 11 is a block diagram of the complete MONDO Chip. The chip has four channels, two levels of analog energy summing circuits and discriminators, and several serially-programmed DACs and registers. The DACs are used to control the CFD threshold, gain and offset, the TAC ramp rate, the calibration signal level, and the energy sum thresholds. Registers control the discriminator mode (CFD or leading edge), the VGA gain and frequency response and enable channels to be calibrated or summed by the trigger sum circuit.

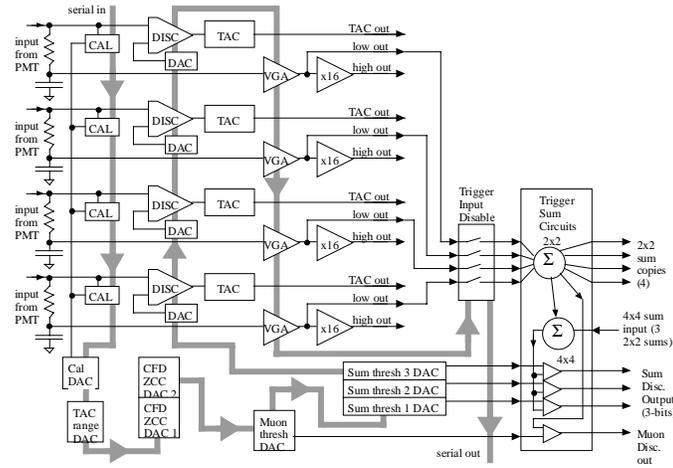


Figure 11: MONDO Chip block diagram.

The trigger sum circuit sums the four energy outputs, and has been designed to be live on every beam clock cycle. Since the energy channel integrates, the summing circuit performs an analog correlation so the output represents only the sum of the charge that has arrived in the current beam clock cycle. The sum for the previous cycle is used as the baseline for the current cycle. The output switches between two correlators with one acquiring its baseline while the other is summing. The 2x2 sum output is a current. Several copies are made and used in 4x4 sums that are discriminated using three levels. Use of current mode signals allows simple copying and summing. The summing circuit was described in detail by Frank [8]. Performance parameters of the chip are presented in Table 3. The MONDO Chip has been designed for implementation using 1.2 μm Orbit CMOS. The overall chip dimensions are 3905 μm by 3905 μm .

Table 3. MONDO chip performance parameters

<i>Parameter</i>	<i>Value</i>
Energy dynamic range	>14 bits
Gain programming over a 3:1 range	5-bit resolution
Minimum discriminator threshold	< 10mV
Timing range	80 ns
Timing jitter	50 ps rms (for > 100 mV input)
Energy sum formation time	< 100 ns

2. GERMANIUM SPECTROMETER

Double-sided solid-state strip detectors are important in a wide variety of photon detection applications that require both good spatial resolution and energy resolution. Germanium strip detectors are currently available which provide 2 mm spatial

resolution combined with excellent energy resolution over a wide energy range extending to ~ 1 MeV [9]. CdZnTe and silicon strip detectors are finding applications as hard and soft X-ray detectors [10, 11]. All of these detectors require compact, low-noise electronics with on the order of 10 to 1000's of channels. Both polarities of signals must be measured. Applications such as space-based detector systems also require that these electronics are low power. Most photon counting applications require that the electronics be self-triggering over a wide dynamic range. Very few end-to-end systems with all of these properties have been developed. Examples of chips developed originally for silicon strip detectors are the XA-1 (commercial device from IDE AS), and the ACE chip (NASA/Caltech). We present here results from an ASIC chip set developed at Oak Ridge National Laboratory (ORNL) specifically for the germanium strip detector.

Four ASICs have been developed using the ORBIT FORESIGHT $1.2 \mu\text{m}$ n-well process. These chips are referred to collectively as NRL-4, and represent the fourth step in a series of prototype chips developed specifically for the germanium strip detector. One chip set is PMOS and the other NMOS for positive and negative input signals respectively. A standard die size of 2.4×2.4 mm was selected for circuit development. The front-end chip is a two channel preamplifier and shaping amplifier similar to the chip described in reference [12]. The preamplifier has a conversion gain of ~ 35 mV/fC and an RC recovery time ~ 1 msec. The design is descended from the preamplifier developed by ORNL for silicon track detectors in the PHENIX and PHOBOS projects for the Relativistic Heavy Ion Collider [13]. The peaking time of the output pulse is $\sim 6\text{--}9$ μs which is optimized for the energy resolution achieved for a germanium detector with low current leakage. Pulse shaping is CR-RC² with poles provided by n-well or p-well resistors respectively. The second chip is a two channel Peak Detect and Hold (PDH) circuit with a discriminator for self-triggering. The peak detection circuit is based on a design by Kruiskamp and Leenarts [14] and uses a MOS current mirror instead of a rectifying diode, thereby minimizing the effect of charge injection into the hold capacitor when a peak is detected [15].

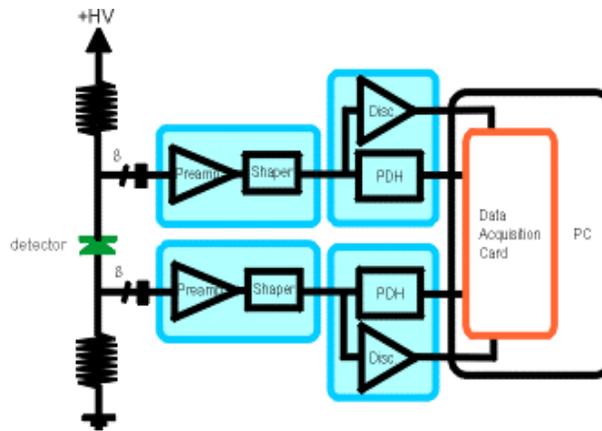


Figure 12. Block diagram of preamp-shaper-stretcher-DAC

A simplified block diagram of the readout system is shown in Figure 12. The four varieties of ASICs are indicated by the shaded boxes. The demonstration system provides 8 p-channel and 8 n-channel readouts. Four copies of each ASIC are required in the full 8-channel system since the prototype ASICs are 2 channel devices (detail not shown in the Figure). In the 8×8 system, the PDH signals are digitized using a standard data acquisition card with 16 channels multiplexed into a 12-bit ADC. The data acquisition card is plugged into a personal computer (PC). Differential line drivers, optical isolators, and a ferrite loop were added between the PC and the demonstration board in order to minimize noise pick-up from the PC. Discriminator signals on the PDH circuits are combined to provide a trigger for the data acquisition cycle. All 16 signals are digitized. Data is stored in list mode for subsequent processing and analysis.

Several biasing adjustments are made external to the ASICs in the prototype chip set. Key adjustments are the DC level of the amplifier chip baseline, gate voltage of the feedback MOSFET (feedback resistance), discriminator voltage, and linear gate reference voltage. For this work, the NMOS devices were all operated with a baseline of 1.5 V and the PMOS devices with a baseline of 3.5 V. A large pulse will drive the NMOS shaping amplifier to near 5 V and the PMOS shaping amplifier to near 0 V from the baseline.

The ASICs are powered by a single 5 V power supply. Power consumption for the preamplifier through peak-detector is ~ 4 mW/channel. Most of the power is consumed in the front-end MOSFET in the preamplifier. The PDH accounts for only 0.5 mW/channel.

The measured noise of the preamplifiers was, for the NMOS, $205\text{ e} + 14.6\text{ e/pF}$ and for the PMOS, $190\text{ e} + 38.6\text{ e/pF}$. The spectrum of a pulser is shown in Figure 13. The x-axis is scaled to units of input charge (electrons) using a calibration of 38 mV/fC. The peak is well fit to a gaussian function with a width of 869 electrons Full Width Half Maximum (FWHM). Corrected for noise pick-up from the PC, the true noise is reduced to 716 e FWHM. This is equivalent to 2.1 keV FWHM using a germanium detector as a signal source, 2.6 keV FWHM in Silicon, or 3.6 keV FWHM in CdZnTe.

The dynamic range of the NRL-4 chip set corresponds to an energy range in germanium of roughly 12 keV–1.2 MeV with an over-all linearity is better than $\pm 0.2\%$. The low end of the dynamic range is limited by noise and some small head-room necessary for the PDH to function. Energy resolution of 2.1 keV FWHM should be possible using a germanium strip detector with a good design to minimize parasitic capacitance (assumed to be ~ 6 pF). This energy range and performance should already be adequate in a number of applications such as large area coded-aperture or Compton imaging systems built around an array of strip detectors.

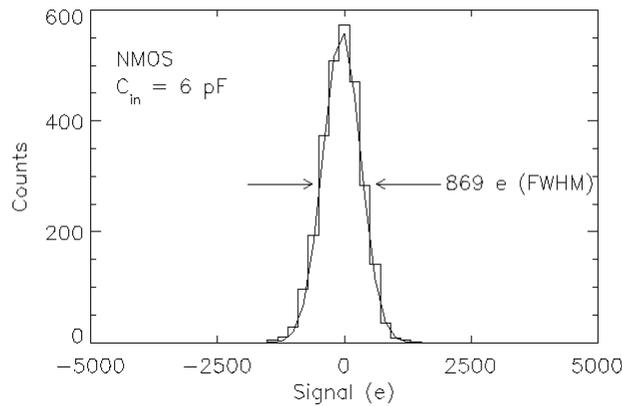


Fig. 13 . Pulse-height histogram of an NMOS channel with a 36 fC input pulse. The histogram is plotted relative to the peak position on an x-axis scale in units of input charge.

Although this performance is already good enough for many applications, better energy resolution is still useful for measuring narrow lines, Doppler broadening and background rejection. The potential of germanium detectors to deliver sub-keV resolution demands lower noise electronics. Energy resolution can be improved by averaging signals from both detector faces [9]. With the NRL-4 electronics, energy resolution obtained using signals from both sides of the detector should be ~ 1.6 keV FWHM. Cooling the CMOS chips has also been demonstrated to reduce noise in previous work [12]. Another approach is to increase the preamplifier power consumption, thus increasing the transconductance of the front end MOSFET.

The next generation chip set is planned to combine both polarity inputs in a single front-end, and to include both the amplifier stages and the PDH circuit on a single multi-channel chip with a multiplexed output.

3. SUMMARY

This paper has presented a summary of some the major chips developed for the PHENIX detector. These include those for the Multiplicity-Vertex Detector, the Central Tracker (Pad Chamber), and the Electromagnetic Calorimeter. The overall architecture as well as some of the basic performance specifications were presented. In addition, architecture and performance of signal processing chips developed for the Naval Research Laboratory for germanium spectroscopy was presented.

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