A Prototype ASIC for APD Array Readout of Scintillating Fibers

John R. Macri, Mark L. McConnell and Mark Widholm
Space Science Center, University of New Hampshire

Alan Wintenberg, Usha Jagadish and Shane Frank
Oak Ridge National Laboratory

Abstract

We report on the development of custom front end electronics for use with avalanche photodiode (APD) arrays as part of a NASA technology study for the readout of scintillating plastic fibers. This particular effort focuses on the SOlar Neutron TRACking experiment (SONTRAC). The SONTRAC detector measures the direction and energy of incident 20 to 250 MeV neutrons by recording the tracks of the ionizing recoil protons in a closely packed bundle of scintillating plastic fibers. The scintillating fiber and APD array combination is also under study for application in high energy gamma-ray telescopes that track minimum-ionizing electron-positron pairs. APD arrays featuring 64 1 mm square pixels are used for detecting and measuring the scintillation light emitted from the fibers. An application-specific integrated circuit (ASIC) implementation of the electronics is required to produce a detector sufficiently compact for practical use in a flight experiment featuring many thousands of channels. This paper briefly outlines the SONTRAC concept, presents the design of a four-channel prototype ASIC fabricated using the 0.35 micron TSMC process and describes the prototype testing and results. (As of the abstract submission date, the ASIC is being fabricated. We expect prototype testing to be completed before the conference.)

I. Detector Concept and ASIC Requirements

Reports on the SONTRAC detector concept and on the planar processed APD arrays used here were presented at a previous IEEE Nuclear Science Symposium [1], [2]. Figure 1 shows recent photographs of a prototype 64 pixel (8 x 8) APD array in test configurations coupled with scintillating fibers and read out with discrete electronics. The 64 APD pixels are formed in an 8 x 8 array with 1.27 mm pitch. The windowless APD array is bonded to a ceramic carrier with the signal leads emerging from the bottom. The paper will summarize current project status.

The APD readout electronics for SONTRAC must be compact and low power to serve the approximately 100,000 closely-packed scintillating fiber channels composing a flight detector. The front end electronics ASIC serving all channels of each APD array in the detector must fit within the area occupied by that array. Power consumption must be less than 1 mW per channel. For any detected proton track event, relatively few fiber channels, perhaps 100 distributed across as many ASICs, will register signals. As such, off-chip, system-level trigger logic and sparse readout of the data is required.

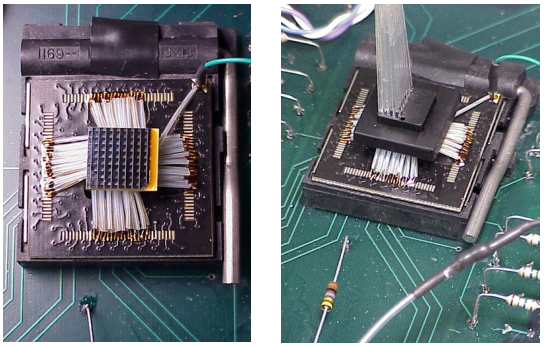
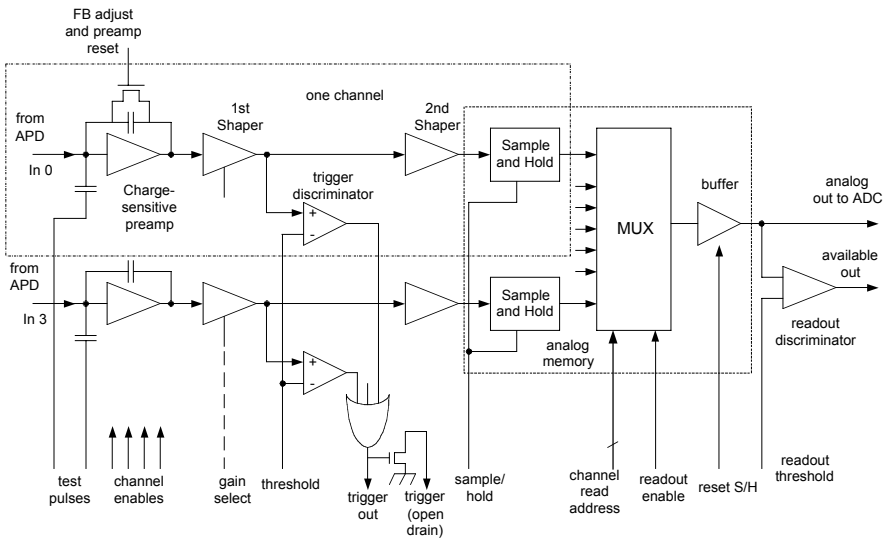


Figure 1. 64 pixel APD array (left); array coupled to scintillating fiber bundle (right)

II. ASIC Design

Figure 2 is a block diagram of the ASIC. Fast (<10 ns) signals will be presented to the ASIC from the pixels of an APD array. The ASIC will have multiple channels each consisting of a charge-sensitive preamplifier, shapers, discriminator, etc. The prototype ASIC has four channels; ultimately, 64 will be needed to match the 8 by 8 APD array. The operation of one channel is as follows. Pulses produced by an APD pixel are integrated using a charge-sensitive preamplifier and then shaped using two stages of pulse shaping. A discriminator following the first shaping stage has a programmable threshold and is used to detect the leading edge of pulses. Its output is logically OR'ed with that of all other discriminators, and that result is sent to the system-level trigger logic. The second shaping stage passively filters the pulse and increases the peaking time to approximately 200 ns. The peak of this signal is be held by the sample-and-hold circuit which is controlled by the external trigger logic. Once an event has triggered the system, the readout phase starts. The system controller, which is not part of the ASIC, uses the multiplexer to sequentially send the output of each sample-and-hold to the analog output and to the readout discriminator. If the signal is above the threshold of the readout discriminator, then it is digitized by the ADC, but if is below the threshold, the system controller skips digitizing that channel and proceeds to readout the next one.



The preamplifier and shapers are designed to operate on less than 0.5 mW and to have no more than 500 electrons (rms) noise for a 2 pF detector. The charge sensitive preamplifier has a gain of 5mV/fC and is followed by a programmable voltage gain stage that does double duty as the first shaping stage. Gains of 1.6V/V (low gain setting for the bigger test pulses) or 12V/V (high-gain setting for the actual charges expected) are possible. The first pulse shaper is approximately CR-RC with a peaking time of approximately 70 ns.

In order to save power, a passive shaper is used for the second shaping stage. The passive shaper will consist of a simple RC filter (Figure 3) with the C being part of the sample and hold, which is an analog memory [3]. While sampling, the first switch is closed. It has a low resistance compared to the fixed resistor. The nominal peaking time is 200 ns when processing the pulse developed by the first shaping stage. The first switch is opened to allow capturing the peak (hold mode). The second switch is normally open and is closed to allow reading of the held peak.

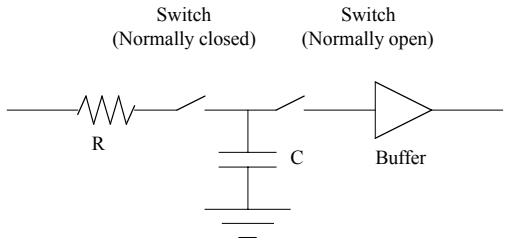


Figure 3. Second shaper stage and analog memory.

In an array detector that is designed to capture multi-channel, simultaneous events, it is possible to combine information from several channels in real time and to use that information to trigger sampling of all channels. By combining the information and not sampling any channels unless the predetermined conditions are met, only events that are potentially of interest are captured, and the probability of the event being interesting is increased. An additional benefit of this type of triggering is the sampling of channels that would have insufficiently small signals to self-trigger.

For SONTRAC, we can operate on the assumption that events of interest will have a proton end-of-track (Bragg peak) signal in at least one channel. Since this is a large signal, it will be well above the noise and easy to discriminate on. The basic idea is to set the discriminator threshold to a level that is a relatively small fraction of the end-of-track signal, but well above the noise. This should give a time mark (logic pulse) delayed a small fraction of the first shaper peaking time (150ns). The outputs of all the discriminators on a single chip are OR'ed together and sent to the detector trigger logic (which might OR all chip OR-outputs together.) to produce a system trigger. The system trigger would be an input to the chip and would be delayed by an on-chip delay to cause the sample-and-hold circuit to go into hold mode just as the output of the second shaper peaks.

III. Test Fixture and Important Conclusions

The test fixture supports an APD array and several prototype ASIC chips for readout. Scintillating fiber bundles composed of 64 250 micron square scintillating plastic fibers can be coupled to the APD surface for testing in a proton beam. The test fixture permits external adjustment of key biases and shaping parameters as well as control of the discriminator levels and implementation of the external, system-level, trigger. Test pulses can be applied independently to each channel and the performance at important nodes of the circuit can be examined for the prototype chip's spy channel.

Test results to be reported will include measurements of circuit performance relative to the requirements and the simulations. We will present an analysis of signal to noise performance in an end-to-end test configuration employing incident proton radiation on scintillating fibers coupled to an APD array and the prototype ASICs. We will outline the work required to further develop the ASIC for flight instrumentation and for other APD array applications

IV. References

[1] Ryan, J. M., et al., " A Scintillating Plastic Fiber Tracking Detector for Neutron and Proton Imaging and Spectroscopy", IEEE NSS Conf. Record, Paper N14-62 (1999)

[2] Shah, K. S., et al., "Planar Processed APDs and APD Arrays for Scintillation Detection", IEEE NSS Conf. Record, Vol. 1, p. 56 (1999)

[3] Britton, C. L., et al., ""An Analog Random-Access Memory in the AVLSI-RA Process for an Interpolating Pad Chamber", IEEE NSS Conf. Record, p. 261 (1994)