# TGLD: A 16-Channel Charge Readout Chip for the PHENIX Pad Chamber Detector Subsystem at RHIC[1]

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*Abstract*

This paper describes TGLD, a charge readout chip for the PHENIX Pad Chamber (PC) subsystem at Brookhaven National Laboratory's Relativistic Heavy Ion Collider (RHIC) in Upton, NY. Due to the PC's high channel density, the TGLD and associated circuitry operate within the active detector region as permanent, zero access components, with remote set-up and test during collider operation. The TGLD design accommodates varying pad capacitance and charge gain for three detector subassemblies that detect particles at three different distances from the PHENIX collision vertex. The design also provides adjustable discrimination thresholds from MIP/10 to 2 MIP (Minimum Ionizing Particle). Three TGLD chips operate with a complimentary digital memory unit (DMU) to form 48 channel low power, low mass, readout cards. Partitioning of readout electronics and address control for robust remote operation are discussed. Component and system test results are also reported.

## I. Introduction

The PHENIX experiment is a large and complex, multi-detector experiment. It is comprised of ten different detector subsystems designed to track and measure the energies of heavy ion collisions with ion masses up to gold. The PHENIX PC subsystem consists of three sections, PC1, PC2 and PC3, with an east and west arm for each section. These three tracking detector sections are each positioned at different radial distances from the collision vertex. The PC subsystem accounts for 207,360 of the approximately 600,000 detector channels in PHENIX.

Since the PC tracking detectors are sandwiched between multiple calorimeters, it is important that the PC's radiation absorption be as low as possible, to avoid energy measurement degradation in adjoining calorimeters. Additionally, the large number of PC detector elements preclude bringing pad wire connections outside the detector's active region. This requires the PC front-end electronics be mounted within the PC detector's active region. A minimum density packaging scheme is applied to the entire front-end electronics. In the following section, PC front-end electronics architecture is described. Following this architectural description, TGLD requirements, design and testing is given.

## II. PC Front-End Electronics Architecture

A typical PC front-end electronic channel consists of a charge sensitive preamplifier, signal differentiator, leading edge discriminator, beam crossing sampler and delay memory unit (DMU). The DMU delays and holds the pixel state until the PHENIX trigger system signals for event readout. A PC TGLD channel block diagram is shown in Figure 1. In addition to these TGLD operational functions, on-chip control and testing functions are included to allow remote control and evaluation of front-end electronics operational status while sealed inside the experiment after installation.

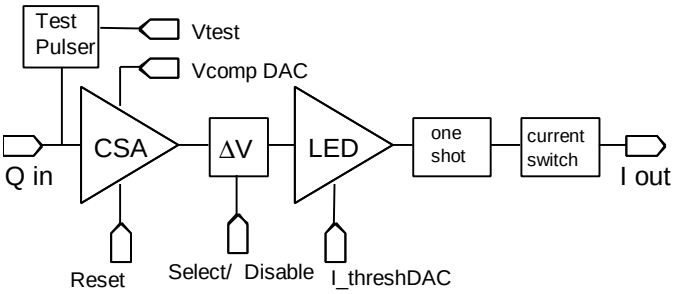


Figure 1. Single Channel Block Diagram of PC TGLD

Three bare die TGLD, one DMU and three RS-485 interface chips are mounted chip-on board to form a 48 channel readout card (ROC). Figure 2 illustrates a PC ROC. Each PC detector subpanel has 45 ROCs arranged as five rows with nine ROCs each, for 2160 channels of pad readout. These 2160 channels of pad readout are controlled by a front-end module that interfaces with the PHENIX on-line data acquisition system.

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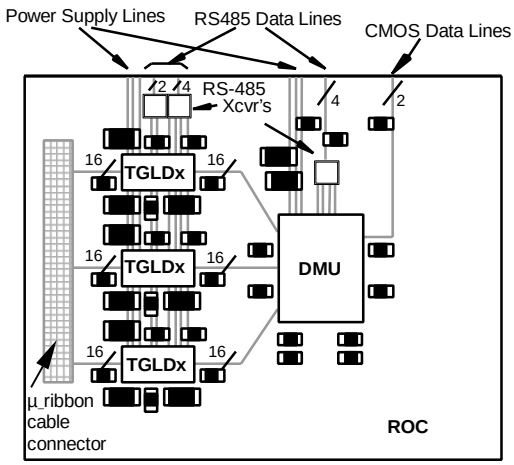


Figure 2. PC Read-Out Card diagram

## III. TGLD REQUIREMENTS

TGLD is designed to be a low power, charge readout chip that can be used with any of three different size pad chamber detectors. The TGLD ASIC has 16 channels, each with a charge sensitive preamp, a C-R differentiator, a leading edge discriminator, a one-shot and a current switch interface to DMUs at the output of each channel. TGLD also contains serial access control registers, DACs, test pulsers, analog multiplexers and channel enable and disable controls.

Pad capacitances for PC1, PC2 and PC3 are 23pF, 36pF and 42pF respectively due to increasing pixel size. Similarly, detector charge sensitivity ranges from 18fC/MIP for PC1 to 36fC/MIP for PC3. PHENIX experiment requirements require PC discriminator thresholds from MIP/10 for PC1 to a few MIPs for PC3. This translates to discrimination thresholds over the range of 2fC to 90fC. A single gain preamp and discriminator design must be stable for this range of detector capacitances, charge sensitivities and threshold adjustments. Preamp, differentiator and discriminator circuit descriptions follow below.

## IV. CHARGE SENSITIVE PREAMP DESIGN

The PC charge sensitive preamplifier was designed for positive charge input with a gain of 10mV/fC. The preamp consists of two stages. The first stage, is a charge to voltage amp with a gain of -2.5mV/fC. The second stage is a voltage amp with a gain of -4V/V. The first stage is composed of an inverting, single gain stage, cascode amplifier followed by a non-inverting, level shifting buffer stage with a combined 0.4pF poly-poly feedback capacitor. The feedback capacitor is split between the output of the cascode amp and the output of the common drain, level shifting buffer. The feedback capacitor can be reduced to 0.2pF to increase the charge gain to -5mV/fC if higher charge amplification is required. This first stage input is referenced to the positive power supply rail and its output swings towards the negative rail for positive input charges.

The second stage is an inverted version of the first stage with a combined 0.8pF input coupling capacitor and a 0.2pF feedback capacitor producing a -4V/V gain. This inverting voltage amp is referenced to the negative power supply rail and swings towards the positive supply for negative input voltages. Figure 3 shows a simplified schematic of the charge sensitive preamp. A detailed description of this preamp topology is given by Britton [1].

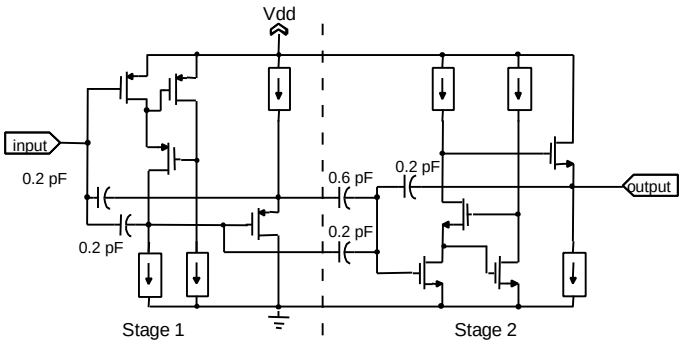


Figure 3. Charge Sensitive Preamp

The PHENIX timing and control system generates experiment wide reset signals every millisecond. An internal digital delay generator generates carefully timed multi-phase reset signals to the TGLD preamp to prevent transient off-set voltages induced by reset switch charge injection. The differentiator and discriminator outputs are also disabled during this reset period to avoid spurious outputs to the DMU.

## V. DIFFERENTIATOR AND DISCRIMINATOR DESIGN

The preamp is followed by a passive CR differentiation stage composed of a 1 pF poly-poly capacitor and a 140K poly resistor connected to a midpoint voltage of 2.5V. The differentiated signal is passed into the discriminator. Figure 4 shows the schematic of the CR differentiator and discriminator.

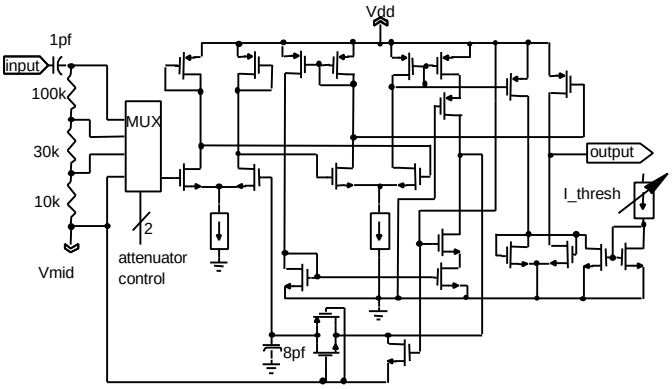


Figure 4. TGLD Differentiator and Discriminator

The discriminator block consists of two stages of differential amplifiers that give a net gain of 10. A third stage converts the output from the differential amplifier to a single ended output. This is fed back to the first differential stage negative input to form a DC stabilization feedback loop. It sets the reference for the first stage. The output of the second stage differential amplifier feeds the inputs of a differential voltage comparator stage. A mismatched current mirror load causes off-set bias currents in the comparator which controls the discriminator's threshold. The comparator's offset current is adjusted by robbing current from the over biased side of the differential circuit to provide a 4:1 discriminator threshold adjustment range. A six bit, on-chip, current DAC [2] connected to an inverting current mirror pulls current from the mismatched current mirror load of the comparator stage.

To achieve the necessary threshold adjustment range for PC1 minimum sensitivity and PC3 maximum insensitivity, the 140K poly resistor of the CR differentiator is divided into three sections forming a three step attenuator. Taps of 1/1, 1/3 and 1/9 attenuation factors scale the discriminator input. The taps are chosen to ensure that the 3 different threshold adjustment ranges overlap. Combining selectable CR differentiator taps and adjustable discriminator off-set currents gives discontinuous but adjustable threshold settings from approximately 1.5fC to 90fC for a dynamic range of 60:1.

The discriminator output is passed through a one-shot that produces fixed 150ns pulse width outputs. The one-shot output switches a 50uA current source on and off to interface with the DMU. Switched current source outputs minimize both output voltage swings and signal coupling back to the inputs. The chip also generates a 25uA fixed reference current for the DMU input stages.

## VI. Serial Registers, DACs, Pulsers & Multiplexers

The PC readout electronics are mounted inside the pad chamber assembly and are not accessible for manual adjustment of controls. To allow remote set-up and control, each TGLD has four sets of registers that control chip/register address, mask bits and DAC values. The addressing and control scheme used in the TGLD is flexible enough to selectively input and read out serial data for different functions residing in different serial registers. This is particularly useful in adjusting operating parameters in a system that has 207,360 channels. This has also been helpful in testing ROCs. The control data includes 16 bits for output enable/disable, 16 bits for test pulser enable/disable, two bits for attenuation select, five bits for analog MUX decoding, six bits for preamp decay slope DAC control, six bits for discriminator threshold DAC control, seven bits for input test pulser amplitude DAC control and 10 bits for TGLD chip/control register address control.

To facilitate remote testing, TGLD incorporates 16 on-chip test charge pulsers for testing individual and combined channels with individual channel masking. The amplitude of all charge pulsers is set by a common on-chip DAC that can be adjusted to generate an equivalent test pulse of 1fC to 128fC. The decay slope of the preamp can be adjusted by using another on-chip DAC to set the leakage compensation slope from 1.2µsec to greater than 160µsec. An analog MUX allows one of the 16 preamp outputs to be monitored at an external pin through a high speed, high capacitance drive buffer amp. The analog MUX can be disabled for normal operation. Two control bits control the C-R attenuator tap selection. The discriminator threshold DAC is a six bit current DAC that gives a near linear threshold adjustment of 10mV to 45mV. A 16 bit control register enables or disables individual channel outputs. This function is used for disabling noisy channels in operation.

TGLD serial control allows serial data to be transmitted to or read back from an individual chip among multiple TGLD chips and readout cards on a common serial control bus. Addressing is accomplished by setting six external pins to ground or Vdd to establish a geographical address and comparing this address with an address control word transmitted to all TGLDs on a particular row. The six bits represent which readout card of nine on a row, and which TGLD die of three on each ROC, is being addressed. Also included in the serial address control word is a control register address, signifying which control register to load the following control word. Additional bits in the address control word allow control words to be broadcast to multiple TGLDs when appropriate. This addressing scheme results in the ability to selectively address an individual TGLD, if needed, to establish serial data transmission. It is an important feature because the electronics is inaccessible after mounting in the chamber. A failed TGLD will not affect the serial data control of the other chips in this scheme. This increases the fault tolerence and the reliability of the overall system.

## VII. Test Results

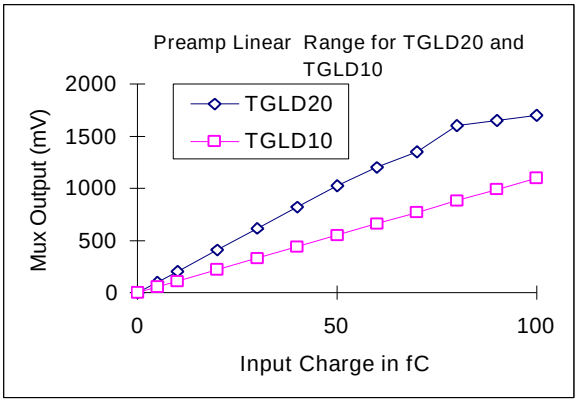


Figure 5. Preamp Linear Range as Measured for TGLD ASICs

TGLD chips with gains of 20mV/fC and 10mV/fC were fabricated and tested. The measured preamp gain between different channels on a chip as well as between different chips was within 5% of the designed value for both gain versions of the chip. The preamp showed good linearity over a 1.3V range. The preamp output curves are shown in Figure 5.

Measured and simulated discriminator threshold curves are shown in Figure 6. The curves show the three attenuation curves for measured(m) and simulated(s) threshold adjustments. Simulation data indicates the desired 4 to 1 adjustment range for all three attenuations. It also shows a proper overlap of threshold adjustment from minimum threshold to maximum threshold. The measured thresholds show that the discriminator picks up the smallest required signal in each attenuation curve. However, the measured range of the discriminator is only 3:1 for each attenuation curve. This produces some gapping from lowest threshold to the highest threshold. This discrepancy is attributed to noise surrounding the feedback loop of the discriminator as well as to on chip power supply variations during large signal differentiation.

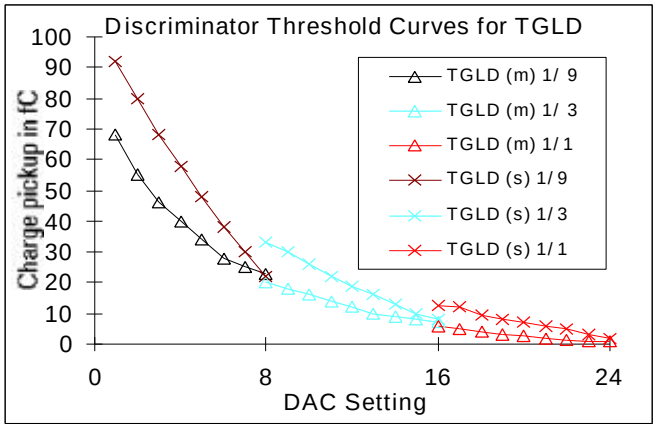


Figure 6. Discriminator Threshold Curves for TGLD_new

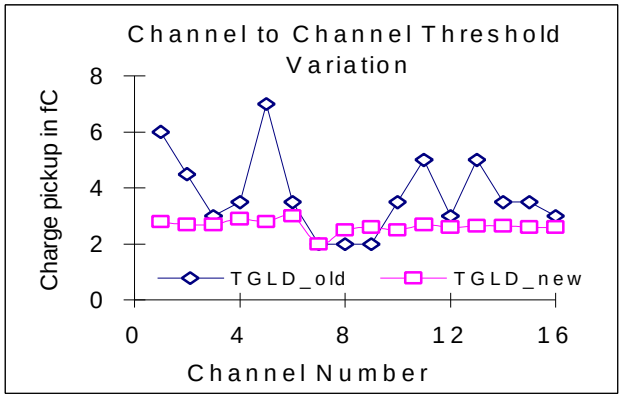


Figure 7. Channel to Channel Variation Comparison

The channel to channel threshold variation of the TGLD is improved by a factor of five from the previous version (TGLD_old). The TGLD_old design had 16 preamplifier-discriminator channels of 5mV/fC gain with controls, adjusts and bias generated external to the chip. It also had an active differentiator between the preamp output and the discriminator input. This active stage was found to have mismatch problems. This resulted in significant channel to channel variations especially at the lower threshold settings as shown in Figure 7.

The TGLD_new design replaces the active differentiator [3,4] with passive differentiator components. This includes a poly resistor and a poly-poly capacitor. The improvement in channel to channel threshold variations has been significant.

## VIII. Conclusions

TGLD 10mV and 20mV chips have been developed for the pad chamber tracking detector front-end electronics in PHENIX. These chips have been designed to accommodate the varying capacitances and charge sensitivities of the three PC detector types, PC1, PC2 and PC3. Both gain versions of the TGLD chip have been evaluated at Lund and ORNL. Test results indicate that the design requirements for gain, minimum threshold sensitivity and channel to channel threshold matching have been met. However, some problems with the new TGLD have been discovered. DC stabilization of the discriminator is a problem during large signal detection. Problems with threshold adjustment range limits and erratic triggering when more than half of the channels fire at once have been uncovered. These defects are associated with the design of the dc feedback loop around the discriminator and the way in which power is routed in the chip. Design revisions are in progress to correct these problems.

## IX. References


[1] C. L. Britton, et al., " TGV32: A 32-Channel Preamplifier Chip for the Multiplicity Vertex Detector at PHENIX," presented at the 1997 Nuclear Science Symposium.

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