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Bristol Babcock DPC 3330 Controller Evaluation

B. R. Whitus

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Instrumentation and Controls Division

BRISTOL BABCOCK DPC 3330 CONTROLLER EVALUATION

B. R. Whitus

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ABSTRACT

Tests were performed on a Bristol Babcock, Inc., Model DPC 3330 process control system to determine the suitability of both hardware and software for use as a low-cost distributed or stand-alone control system.

Results of the hardware tests verified that the hardware met or exceeded the company's published specifications for all test conditions except for the analog input common-mode rejection ratio (CMRR) measurement. The difference in measurement methods used during this test from the methods used by BBI was the reason for the difference in CMRR values. The unit was tested as a stand-alone controller because we did not have version 1.5 of Trolltalk-VAX software needed for the host VAX to support this unit.

The software test consisted of evaluations of only those Advanced Communication and Control Language (ACCOL) modules that have been added to Bristol Babcock controllers since previous evaluations were performed by this group. Except for the logger and scheduler modules, all the ACCOL II modules evaluated worked as described in the reference manual. The logger module did not work because of an error in the early version of the firmware installed in the Beta unit tested, and this failure should not occur in production units. The scheduler module will work as described; however, some of the modes seem redundant or incorrect.

The modular design of this system allows many possibilities for I/O point configuration. As a configuration example, a system with 20 analog inputs, 4 analog outputs, 16 discrete inputs, 16 discrete outputs, 2 counters, and 4 serial communications ports could be purchased for less than \$7000 (hardware only).

Overall, the DPC 3330 appears to be a suitable low-cost controller for use either as a stand-alone controller or as a node in a distributed network.

1. INTRODUCTION

This report describes the procedures for evaluating the performance of a Bristol Babcock DPC 3330 process control system using version 4.0 of the ACCOL Interactive Compiler (AIC) software. The objectives of this effort were to determine the suitability of both the hardware and software for application as a low-cost process controller in an industrial plant environment and to compare/contrast this controller with higher-cost Bristol Babcock controllers.

Tests were conducted on a Model DPC 3330 controller packaged as a NEMA-1 rack-mounted unit. See Fig. 1. This is a stand-alone unit and was tested as such. An IBM PS/2-80 personal computer with DOS version 3.3 was used for configuring, running diagnostics, and monitoring the controller. The controller was not tested as part of a distributed network because we did not have version 1.5 of Trolltalk-VAX host software that is required to support the DPC 3330.

Along with the evaluation tests of the DPC 3330 hardware, tests were performed on ACCOL II software modules that BBI has added since previous ACCOL evaluations performed by this group. The modules tested were: PDM, PDO, command, scheduler, storage, and logger.

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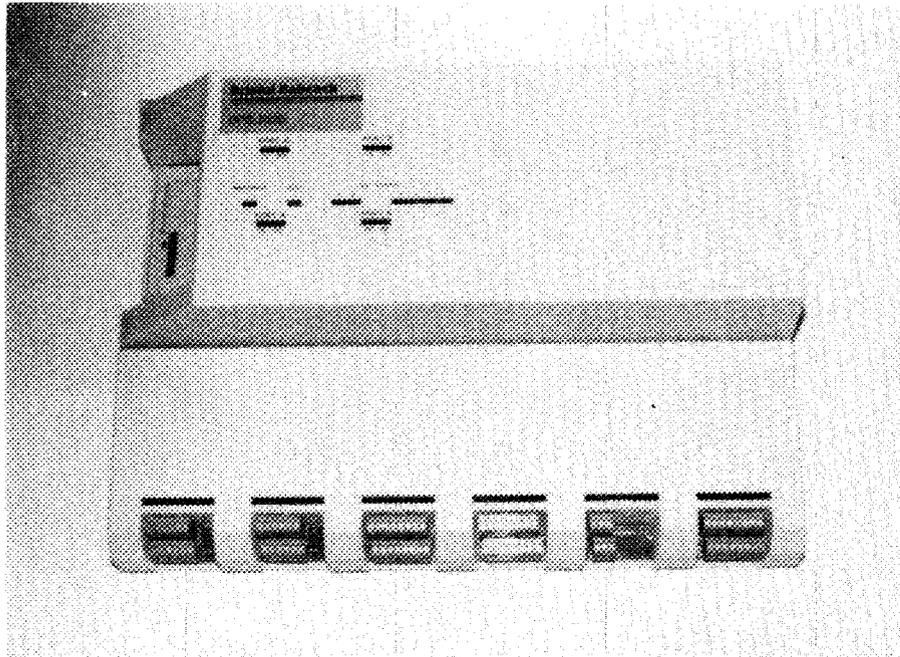


Fig. 1. Bristol Babcock DPC 3330.

2. TEST SETUP

2. EQUIPMENT

2.1.1.1 DPC 3330 Components

The DPC 3330 system tested consisted of the following components:

<u>Quantity</u>	<u>Description</u>
1	System interconnect board
1	CPU engine board
1	Communications engine board
2	Analog input module
1	Analog output module
1	Discrete input module
1	Discrete output module
1	High-speed counter module

2.1.1.1.1 System interconnect (SI) board. The SI board is the interconnection backplane for all plug-in PC boards and modules in the system. It also contains a 24-V dc input power supply which provides power for all I/O modules and PC boards in the system.

Watchdog relay contacts on the SI board provide indication of a controller failure to the user equipment. The watchdog relay is controlled by the CPU engine board. In addition to the watchdog relay, several other passive and active components are mounted on the SI board.

The SI board provides connections for the CPU engine board, two CE boards, two PC-bus boards, and 0, 6, or 12 I/O modules, depending on the packaging option. The DPC 3330 tested was packaged to accept six I/O modules.

2.1.1.1.2 CPU engine board. The CPU engine board contains the central processing unit, memory subsystem, watchdog timer, real-time clock, LED status logic, and the I/O bus. This board is based on the Intel iAPX 186 CMOS, 16-bit microprocessor chip.

The CPU engine board can be furnished with user-configurable RAM or factory-configured EPROM. RAM memory versions are backed by a battery located on the board that provides approximately 6 months of cumulative backup time. EPROM versions retain the application load without battery backup.

The standard CPU engine board has 64 kbytes of RAM and is expandable to 128 kbytes. At the time of test, the Bristol software supported only the basic 64 kbytes of RAM. Provisions are also made for a math coprocessor chip; however, at the time of test, this option also was not supported.

2.1.1.3 Communications engine (CE) board. The CE board contains serial communication controllers, interface drivers and receivers, and LED signal status indicators. A maximum of two CE boards can be plugged into the SI board.

Each CE board provides two serial ports (labeled A/C and B/D) that can be configured independently via switch selection for use with either RS-423 or RS-485 communication formats. Both ports consist of 15-pin, D-type connectors which are compatible with Bristol Babcock's RTU 3320, RDC 3350, UCS 3380, and CFE 3385 equipment lines.

The communication ports provide communications with personal computers (used as either a network monitor or an engineer's portable interface), another Bristol Babcock controller as part of a distributed network, or customer equipment using serial communications formats.

The data rates of both ports can be independently set. Data rates from 110 bytes/s to 9600 bytes/s are currently supported by the Bristol Babcock software. The unit under test contained one CI board, both ports of which were configured for RS-423 signal levels and a data rate of 9600 bytes/s.

2.1.1.4 Analog input (AI) module. The analog input module contains signal conditioning circuits, instrumentation amplifiers, a 12-bit analog-to-digital converter, and an I/O bus interface. Surge suppression is also provided for each AI channel. Each AI module has four input channels. The AI module is available in four versions:

- 0 to 10 V dc, 4 inputs;
- 1 to 5 V dc or 4 to 20 mA, 4 inputs;
- 0 to 10 V dc, 4 inputs, 250 V dc common mode; and
- 1 to 5 V dc or 4 to 20 mA, 4 inputs, 250 V dc common mode.

The 1- to 5-V dc module was tested.

2.1.1.5 Analog output (AO) module. The analog output module provides two analog output channels. Two versions of this module are available:

- 0 to 10 V dc, 2 outputs; and
- 1 to 5 V dc or 4 to 20 mA, 2 outputs.

The 1- to 5-mA/4-to 20-mA board was used for testing.

The AO module uses a 12-bit digital-to-analog converter chip set and I/O bus interface circuitry. Surge suppression is provided for each AO channel.

2.1.1.6 Discrete input (DI) module. The discrete input module provides optoisolation and signal conditioning for each discrete input. The DI processing circuitry consists of storage registers, "change of state" detection, interrupt generation, bus interface, and on-line test select circuitry. The DI module is available in the following four versions:

- 8 DIs, 24-V ac/dc input, 1-ms input filters;
- 8 DIs, 12-V ac/dc input, 30-ms input filters;
- 8 DIs, 24-V ac/dc input, 30-ms input filters; and
- 4 DIs, 120-V ac/dc, 30-ms input filters.

The DI module tested had eight 24-V dc inputs with 30-ms filters.

2.1.1.7 Discrete output (DO) module. The discrete output module contains an I/O bus interface, output status buffer, and control circuitry. Surge suppression is provided for each DO channel. The DO module is available in the following two versions:

- 8 DOs, open-collector outputs; and
- 4 DOs, relay contact outputs.

The 8-DO, open-collector output module was tested.

2.1.1.8 High-speed counter (HSC) module. The high-speed counter module contains four independent input conditioning circuits that provide optoisolation and debouncing. Each input may be sourced from either a dry contact or a differential signal source. Surge suppression is provided for all HSC channels.

2.1.2 Test Equipment

The following equipment was used to perform the tests and evaluations:

- power supply, dual, 0 to 40 V dc Lambda LPD422A;
- counter, HP 5316A;
- voltage calibrator, EDC MV105;
- multimeter, HP 3455A;
- function generator, Wavetek 145;
- decade resistance box, General Radio DB655; and
- oscilloscope, Kikusui COS6100M.

2.1.3 Computer

An IBM PS/2 Model 80 computer was used as the portable engineer's interface (PEI). The computer system consisted of the following components and options:

- computer, IBM PS/2-80;
- math coprocessor, Intel 80387;
- printer, Epson MX-100III; and
- external 5.25-in. floppy disk, PRS-2.

2.2 SOFTWARE

2.2.1 ACCOL II Interactive Compiler (AIC)

AIC is a fill-in-the-blank interactive program used to generate the program loads for the controller. AIC is used to access a large variety

of ACCOL software modules. The software modules are selected and configured to implement a control strategy. The object load file is then formed from the output of the AIC program using the LINK utility. Also, a documentation file may be generated using the ACDOC program. After the controller is loaded, the software modules are executed by controller microcode stored in PROM. Version 4.0, the first PC-DOS compatible version of AIC, was used during the tests.

2.2.2 System Tool Kit (STK)

The system tool kit is an on-line diagnostic program that runs on the PEI and permits the user to view and edit many aspects of a system while the system performs its normal duties. STK software allows the user to perform the following functions:

- download a controller over a serial port,
- examine a running task,
- display the configuration of communication ports,
- display buffer usage,
- display 16 signal values at a time,
- initialize and display the crash block area,
- display analog and logical data arrays,
- display or write any memory location in the controller, and
- send a custom message to a controller.

2.2.3 3330/3350/3380 Diagnostics

The 3330/3350/3380 diagnostic software is used to test and repair the controller hardware. Diagnostic tests are initiated from a PEI or the network host computer. Diagnostic tests were run on the DPC 3330 before initiation of the evaluation test to verify basic operation. In addition to the diagnostic programs, the controller can be forced to run a self-test via a manual reset button on the CPU engine board.

3. TEST PROCEDURES AND RESULTS

3.1 HARDWARE PERFORMANCE TESTS

3.1.1 Analog Input Accuracy

3.1.1.1 Procedure. The purpose of this test was to determine the basic accuracy of the input channels on the two analog input modules. A task was created in a test program load containing two ANIN modules to read all eight inputs. The measured input values were read using STK software. A voltage calibrator was connected to all analog inputs in parallel to provide the input test voltages. The input voltage was monitored with a high-accuracy digital voltmeter to establish the input voltage accuracy to 0.006% full-scale range (FSR). Eight measurements were taken at 0.5-V increments across the 4-V input span for all input channels. No calibration adjustments were performed before testing.

Absolute error was calculated as the voltage difference between the input value and the measured value and as a percent of span. Integral nonlinearity (INL) error was computed as the deviation of a reading from a straight line connecting the end point readings and expressed as percentage of span. Differential nonlinearity (DNL) was computed as the difference in the step between two readings and the expected step size. DNL error is expressed as a percentage of the expected step size.

3.1.1.2 Results. The measured values were identical for all input channels and are shown in column two of Table 1. The absolute error in volts, absolute error as a percentage of full scale, INL, and DNL are given in columns three through six respectively of Table 1. All readings were within the BBI accuracy specification of 0.1%.

Table 1. Analog input accuracy

Input	Reading	Absolute error (V)	Absolute error (%)	INL (%)	DML (%)
1.0000	0.9968	0.0032	0.0805	0.0000	0.0000
1.5000	1.4973	0.0027	0.0673	0.0265	0.0792
2.0000	1.9968	0.0032	0.0805	-0.0134	-0.1327
2.5000	2.4973	0.0027	0.0672	0.0052	0.0792
3.0000	2.9979	0.0021	0.0537	0.0178	0.0812
3.5000	3.4973	0.0027	0.0672	-0.0040	-0.1347
4.0000	3.9979	0.0021	0.0537	0.0067	0.0812
4.5000	4.4973	0.0027	0.0673	-0.0090	-0.1347
5.0000	4.9979	0.0022	0.0538	0.0000	0.0812

3.1.2 Analog Input Noise Rejection

3.1.2.1 Procedure. The test setup shown in Fig. 2 was used to measure dc common-mode rejection. Voltage source E1 was used to provide an in-scale input to the analog input channel while source E2 provided the common-mode voltage. The low-input lead contained a 1-k Ω resistor to simulate lead wire resistance. Input readings were taken with the common-mode voltage source set to 0, -10, and +10 V dc. The dc common-mode rejection ratio was calculated as:

$$\text{DCCMRR} = -20 \log \frac{V_{in}}{20V} \quad . \quad (1)$$

The test setup used to measure ac common-mode rejection ratio (ACCMRR) was the same as the setup used for DCCMRR except that a 10 Vp-p 60-Hz signal source was used as the common-mode voltage source. Sixty hertz was used as the test frequency because most noise sources in an industrial environment are 60 Hz or a multiple thereof. To determine the input reading variations caused by the common-mode input, an ACCOL II task was created to detect the high and low input values while continuously reading the input channel. The ACCMRR was calculated as:

$$\text{ACCMRR} = -20 \log \frac{V_{in}}{10V} \quad . \quad (2)$$

The test setup shown in Fig. 3 was used to determine the input modules' normal-mode rejection ratio.

The same ACCOL II task used to perform the ACCMRR test was used for this test. The ac signal source was set to 5 Vp-p so as not to exceed the maximum input voltage of the analog input module. The NMRR was calculated as:

$$\text{NMRR} = -20 \log \frac{V_{in}}{5V} \quad . \quad (3)$$

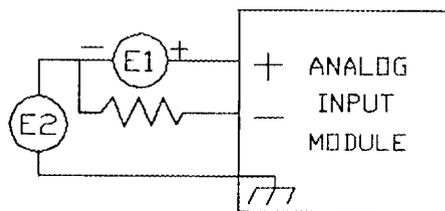


Fig. 2. CMRR test configuration.

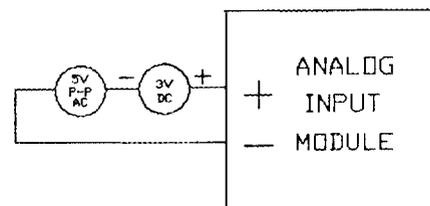


Fig. 3. NMRR test configuration.

3.1.2.2 Results. For the DCCMRR test, a 20-V common-mode voltage change caused the input readings to change 1.1 mV for a DCCMRR of 85 dB. The 10-Vp-p ac common-mode voltage caused input variations of 7.5 mV, resulting in an ACCMRR of 62 dB. The 5-Vp-p normal-mode voltage caused input variations of 256 mV, giving an NMRR value of 26 dB at 60 Hz. The noise rejection data are summarized in Table 2. The measured CMRR did not meet the specified value of 110 dB for common-mode voltages from dc to 60 Hz because BBI uses a different method to determine CMRR. Not using a resistance to simulate long input leads is one major difference in the CMRR test method used by BBI.

Table 2. Analog input noise rejection

DCCMRR	=	85 dB
ACCMRR	=	62 dB
NMRR	=	26 dB

3.1.3 Analog Input Impedance

3.1.3.1 Procedure. Measurements to determine the analog input impedance were taken using the setup shown in Fig. 4. Input reading changes caused by R_e from 0.0 to $1M\Omega$ were used to determine the input impedance. The input impedance (R_i) is given by:

$$R_i = \frac{E_{in} R_e}{E_g - E_{in}} \quad (3)$$

where E_g is the measured voltage with R_e shorted and E_{in} is the measured input voltage with R_e in series with the input.

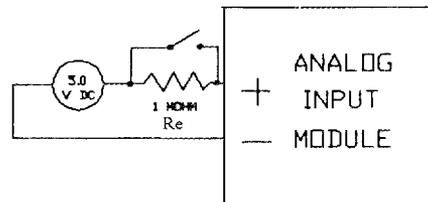


Fig. 4. Input impedance test.

3.1.3.2 Results. The measured voltage was 4.99785 with Re shorted and 4.97422 with Re in circuit. Using the measured data, Eq. (3) gives a value of 210 M Ω for Ri. The measured value of Ri at dc is much greater than the published value of 150 k Ω . The value specified by BBI is for an ac signal and is lower than the dc value because of the effect of the input filters. The input impedance is very high and should cause no loading problems with input sources.

3.1.4 Analog Input Pump-Out Current

3.1.4.1 Procedure. Pump-out current is sourced by the input circuit and flows through the input source and leads. The magnitude of the pump-out current is determined by measuring the voltage developed across a large-value resistor connected between the positive and negative input terminals. A possible source of error in this test is the pump-out current of the DVM used to make the measurement. To reduce error caused by the DVM, a measurement was made without the controller input connected, after which another measurement was made with the input connected. The difference between the two readings was used to determine the magnitude of the analog input pump-out current.

3.1.4.2 Results. The measured voltage across the resistor without the input connected was +2.0 mV. The voltage with the input connected was -20.0 mV. Therefore, the voltage error due to controller pump-out current was 22.0 mV. The magnitude of pump-out current calculated from the measured voltage and resistor value was 2.2 nA.

3.1.5 Analog Input Power Supply Rejection

3.1.5.1 Procedure. The purpose of this test was to determine if variations in the controller power supply input voltage would affect analog input accuracy. Minimum-scale and maximum-scale input voltages were measured with power supply input voltages of 22, 24, and 28 V.

3.1.5.2 Results. Varying the controller power supply input voltage over the specified operating range had no effect on the analog input readings.

3.1.6 Analog Input Reading Rate Effects

3.1.6.1 Procedure. During testing, a shift in input calibration was noticed when the execution rate of the task containing the ANIN modules was set to continuous. To determine the effect of task rate on calibration, a full-scale input was measured at task execution rates of 5.0, 1.0, 0.5, and 0.1 s and continuous.

3.1.6.2 Results. The measurements taken at the different task rates for a 5.000-V input are shown in Table 3.

The calibration changed slightly when the task rate was continuous. Even with the calibration shift at the continuous rate, all measurements were within the 0.1% accuracy specification.

Table 3. Analog calibration
vs task rate

<u>Rate</u>	<u>Reading</u>
C	4.9968
0.1	4.9979
0.5	4.9979
1.0	4.9979
5.0	4.9979

3.1.7 Analog Input Relay Noise Rejection

3.1.7.1 Procedure. The purpose of this test was to determine if EMI generated by devices such as relays mounted close to the DPC 3330 would affect the analog input measurements. To perform this test, a mechanical relay that controlled an electric fan was connected to a discrete output. One ACCOL II task alternately switched the relay on and off at its fastest operating rate. Another task read an analog input channel and stored high and low readings. The relay was physically moved around the DPC 3330 to see if EMI from the switching of 120 V ac to the fan would affect the analog input.

3.1.7.2 Results. The analog input measurements remained constant. The relay switching had no measurable effect on the analog inputs.

3.1.8 Analog Output Accuracy

3.1.8.1 Procedure. The purpose of this test was to determine the basic accuracy of the two output channels on the analog output module. A task created in the test program load assigned signal names to the output channels, and the module was configured for a 1.0- to 5.0-V output. During testing, STK software was used to set the outputs to the desired values. The outputs of the analog output module were measured at eight points across the 4.0-V span using a DVM with an accuracy of 0.006% FSR. Error calculations were performed as described in Sect. 3.1.1.1 for the analog input accuracy test. No calibration adjustments were performed on the module before the tests.

3.1.8.2 Results. The results of the measurements for output channels one and two are given in Tables 4 and 5. All output values were well within the 0.1% specification.

Table 4. Channel 1 output accuracy

Desired output	Measured output	Absolute error (V)	Absolute error (%)	INL (%)	DML (%)
1.0000	0.9998	0.0002	0.0050	0.0000	0.0000
1.5000	1.4995	0.0005	0.0125	-0.0233	-0.0700
2.0000	2.0000	0.0000	0.0000	0.0050	0.0900
2.5000	2.4996	0.0004	0.0100	-0.0140	-0.0900
3.0000	3.0000	0.0000	0.0000	0.0000	0.0700
3.5000	3.4997	0.0003	0.0075	-0.0100	-0.0700
4.0000	4.0001	-0.0001	-0.0025	0.0000	0.0700
4.5000	4.4997	0.0003	0.0075	-0.0100	-0.0900
5.0000	5.0002	-0.0002	-0.0050	0.0000	0.0900

Table 5. Channel 2 output accuracy

Desired output	Measured output	Absolute error (V)	Absolute error (%)	INL (%)	DML (%)
1.0000	0.9996	0.0004	0.0100	0.0000	0.0000
1.5000	1.4993	0.0007	0.0175	-0.0367	-0.0650
2.0000	1.9997	0.0003	0.0075	-0.0100	0.0700
2.5000	2.4993	0.0007	0.0175	-0.0260	-0.0900
3.0000	2.9998	0.0002	0.0050	-0.0067	0.0900
3.5000	3.4993	0.0007	0.0175	-0.0214	-0.1100
4.0000	3.9998	0.0002	0.0050	-0.0075	0.0900
4.5000	4.4992	0.0008	0.0200	-0.0211	-0.1300
5.0000	4.9998	0.0002	0.0050	-0.0080	0.1100

3.1.9 Analog Output Interaction

3.1.9.1 Procedure. To determine if the output of one of the analog output channels on the module affected the output of the other channel, the two output channels were set to all four combinations of 1.0 and 5.0 V.

3.1.9.2 Results. The test data are shown in Table 6. The only interaction was a 0.1-mV change on channel B at setting 1.0 V when channel A was changed from 1.0 to 5.0 V. This error is only 0.01% of the output, and therefore not significant.

Table 6. Analog output interaction data

Channel A setting	Channel B setting	Channel A output	Channel B output
1.0	1.0	0.9998	0.9996
5.0	5.0	5.0003	4.9998
1.0	5.0	0.9998	4.9998
5.0	1.0	5.0003	0.9995

3.1.10 Analog Output Setting Time

3.1.10.1 Procedure. The objective of this test was to determine the time required for the analog output to settle after a full-scale change. A task was created to alternately change the analog output setting from 1.0 to 5.0 V. The output response was observed using an oscilloscope connected to the output module to measure the rise and fall times. The only output loading was that of the scope probe.

3.1.10.2 Results. The measured rise time of the output was approximately 25 μ s and the measured fall time approximately 50 μ s. No overshoot was observed on either transition. The test equipment available did not allow precise measurement of setting time to $\pm 0.1\%$. However, the fast observed transition times and lack of overshoot indicate that the specification of 100 μ s setting time was met.

3.1.11 Analog Output Drive Capability

3.1.11.1 Procedure. This test was to verify the analog output accuracy over the specified range of output loading. With the module configured for a 1.0- to 5.0-V output, the actual output was measured with the output set to 1.0 and 5.0 V with resistive loads of 1 M Ω , 5000 Ω , 2500 Ω , and 1000 Ω (1000 Ω is the minimum value of load resistance that can be used without exceeding the output rating of the module). Next, the module was tested while configured for a 4- to 20-mA output. The

actual output was measured with the output set to 4.0 and 20.0 mA for loads of 250 and 650 Ω .

3.1.11.2 Results. The results of the voltage mode test are shown in Table 7. The output was within the 0.1% tolerance for all load values while operating in voltage mode.

Table 8 shows the test results with the output operated in current mode. The output was about 0.5% high for both tests, which is probably due to the error in the 250- Ω resistor used to determine the output. However, changing the load from 250 to 650 Ω resulted in a small (0.02%) output change, indicating good compliance of the output with different loads.

Table 7. Analog output loading (voltage mode)

Load resistance (Ω)	Measured 1.0-V output	1.0-V output error (%)	measured 5.0-V output	5.0-V output error (%)
1.0 M Ω	0.9995	0.05	5.000	0.00
5000	0.9995	0.05	5.001	-0.02
2500	0.9995	0.05	5.000	0.00
1000	0.9995	0.05	4.997	0.06

Table 8. Analog output loading (current mode)

Load resistance (Ω)	Measured 4.0-mA output	4.0-mA output error (%)	Measured 20.0-mA output	20.0-mA output error (%)
250	4.017	0.43	20.104	0.52
650	4.017	0.43	20.102	0.51

3.1.12 Analog Output Power Supply Rejection

3.1.12.1 Procedure. The purpose of this test was to determine if changes in the controller power supply input voltage would affect the analog output calibration. The output voltage was measured with output settings of 1.0 and 5.0 V with the power supply input voltage set to 22, 24, and 28 V.

3.1.12.2 Results. Varying the controller power supply input voltage over the specified operating range had no effect on the analog output.

3.1.13 Discrete Output Drive Capability

3.1.13.1 Procedure. The discrete output module tested had eight open-collector outputs, with the output drive capability specified as 100 mA. The output terminal voltage was measured with 6-, 10-, and 100-mA loads. Rise and fall times of the output were also checked with the 100-mA load connected. The channel output was exercised for the switching characteristics test by writing an ACCOL II task to alternately switch the output channel on and off as fast as possible.

3.1.13.2 Results. Discrete output voltages with the different test loads are shown in Table 9. Rise and fall times were both less than 0.2 μ s. In the test described in Sect. 3.1.7, the discrete output module was used to control a power switching relay, further verifying its output capability for a typical application.

Table 9. Discrete output loading

Load (Ω)	Output (V)	Output current (mA)
1000	0.64	6
600	0.66	10
60	0.74	100

3.1.14 Discrete Input Sensitivity and Speed

3.1.14.1 Procedure. An ACCOL II test was created to sample the discrete input module signals at a 10-Hz rate. The signals were then monitored using STK for the sensitivity test. To determine the input switching point, a dc voltage was applied to the input and increased until the input recognized a one. The dc input was varied around the threshold to determine if the input level had hysteresis.

To determine the discrete input module speed, a low-speed counter module was configured in the ACCOL II load using a discrete input as the counter input. The frequency measured by the counter was monitored using STK. A signal generator output was used as the input test signal, and generator frequency was increased until the counter ceased to measure the input signal.

3.1.14.2 Results. The dc input threshold was determined to be 15.5 V with no noticeable hysteresis.

When the discrete input was used as a counter input, the maximum operating frequency was 20 Hz. The 20-Hz frequency limit is reasonable considering that this input module had 30-ms filters.

3.1.15 High-Speed Counter Operation

3.1.15.1 Procedure. Two tests were performed on the high-speed counter module (HSC). The first test measured input sensitivity with the input configured for externally powered single-ended drive. A variable-amplitude function generator was connected directly to the input, and the generator output was adjusted until the counter input threshold was determined. The maximum operation frequency for the HSC was also determined.

A second test was devised to test the operation of the counter when configured for differential inputs. A circuit to provide open-collector differential outputs was constructed using TTL integrated circuits and driven by the Wavetek function generator. The HSC I/O module jumpers were configured for internally powered differential inputs. The maximum operating frequency was then determined for this configuration.

3.1.15.2 Results. For the single-ended externally powered configuration, the input sensitivity was 14 V_{p-p}, which is well within the specified tolerance of 24 V $\pm 10\%$. Operation was also correct with the inputs configured for internally powered differential inputs. For both tests, the counter operated to a frequency greater than 15 kHz, which was much better than the specified maximum frequency of 10 kHz.

3.2 ACCOL II SOFTWARE MODULE TESTS

3.2.1 Command Module

3.2.1.1 Procedure. A task was written that contained the command module and a digout module. The output and status terminals of the command module were wired to digout module outputs so that the status of these signals could be observed on the output module LEDs. All other command module terminals were assigned ACCOL II signal names in order to read and/or modify them using STK.

3.2.1.2 Results. The task rate was set to 1.0 s, the delay terminal to 20 s, and the transition terminal to 10 s. The output turned on properly after the delay period, and the status went true as expected

after the transition delay expired, if the limit switch signal had not gone true during the transition period. After each command transition, the status went false until after the transition period, if the limit switch signal was not true. The run-time accumulation and reset functions also worked as described. The command module worked exactly as described for all tests performed.

3.2.2 PDM Module

3.2.2.1 Procedure. A PDO (pulse duration output) module was used to provide the input for the PDM testing. The PDO module output was used to switch a discrete output wired externally to the discrete input used as the PDM module input. Signal names were assigned to the other PDO and PDM terminals for monitoring and modification with STK. The PDO resolution was always set to 20 ms/tick for this test.

3.2.2.2 Results. Basic operation was tested by applying various time duration signals to the PDM input using the PDO module and reading the resulting PDM input signal. The data for Mode 1 are shown in Table 10, and the data for Mode 2 are shown in Table 11. The state terminal was observed to go true after the deadband range had been exceeded. Track operation was tested by increasing the input pulse width to a value greater than the track range and noting that the pulse was rejected and the state terminal went true for one cycle. After the new pulse value was read for two consecutive cycles, the new value was set on the PDM input terminal and the state terminal turned off. All other functions also worked as described.

Table 10. PDM Mode 1 accuracy

Input duration (ticks)	Reading (% FS)
50	0.00
125	49.50
126	50.17
200	99.50
201	100.00

Table 11. PDM Mode 2 accuracy

Input duration (ticks)	Reading (% FS)
148	0.00
150	0.00
375	49.83
376	50.11
600	99.89
601	100.00

3.2.3. PDO Module

3.2.3.1 Procedure. The PDO (pulse duration output) module's raise and lower outputs were connected to a discrete output module to provide a visual indication of the output states. The high-limit and low-limit inputs were provided by a discrete input module which had toggle switches for easy switching of limit inputs. All other PDO module terminals were monitored and set using STK.

3.2.3.2 Results. Basic Mode 0 operation was tested while evaluating the PDM module. In addition, resolution changes, min-time, and correct input signal responses were verified. Lower output operation was also tested in Mode 0 with a negative input.

For Mode 1 testing, a 10-s task rate was used. With the low limit turned on and the control signal set to 25%, 2.5-s pulses were output for each cycle. For these conditions, the reset signal always indicated 25%. With the control signal set to 50% and the high limit true, 5-s lower pulses were generated and the reset signal indicated 50%. Next, with the control signal set to 10% and the PDO min signal set to 0.5 s, 0.5-s-lower pulses were generated on each cycle. In a similar manner, a 0.5-s output was generated on the raise terminal when the control signal was set to 110%. The state of the limit signals had no effect when the control signal was overrange or underrange.

Mode 2 is identical to Mode 1 except that the limit signals are not used to provide feedback. Mode 2 worked as specified, and the limit signals had no effect on operation.

Mode 3 also operated as specified, with output duration and direction corresponding to the difference between the control signal and the feedback signal. The limit signals had no effect in this mode.

3.2.4 Scheduler Module

3.2.4.1 Procedure. Toggle switches were read with a DI module to provide the scheduler module strobe, state, and reset inputs. The first three output terminals were assigned to the DO module to provide visual indication of their state on LEDs. All other scheduler input and output terminals were set and monitored with STK.

3.2.4.2 Results. In Mode 1, if rank values were specified, then the next output turned on or off was selected as described for Mode 3. If the rank signals were 0.0, then the module operated in Mode 1 as specified.

In Mode 2, if rank values were specified, then the operation matched the description for Mode 4. Mode 2 worked as described if all rank signal values were 0.0.

Mode 3 worked as described. In Mode 3, if ranks were not specified, then Mode 2 sequencing occurred.

Mode 4 worked as described. If ranks were not specified, the output sequenced as specified for Mode 2.

Since rank is not ignored in Modes 1 and 2, the modes seem to be duplicated. The reset and track inputs had the described effect on module operation in all modes.

3.2.5 Stepper Module

3.2.5.1 Procedure. The stepper module was placed in a task with ACCOL II signals assigned to all terminals. An 8×2 analog array was created with unique values in each location, and an 8×4 digital array was created for use in the stepper module test.

3.2.5.2 Results. Proper operation was verified for the following stepper module actions:

- The direction and strobe signals cause correct stepping.
- The hold-off signal prevents execution of a step operation.
- The index value selects output at the next strobe.
- Reset signal actuation loads the reset index.
- The track signal goes true when the active step matches the track index.
- The time signal correctly records the period of time that a row is executed.
- Digital-to-analog and analog-to-digital unit conversion works correctly.
- The step signal indicates the row being executed.

3.2.6 Storage Module

3.2.6.1 Procedure. ACCOL signals were assigned to all the module terminals, and four signal lists were created to perform the module test. The DPC 3330 does not provide for expansion memory, so all storage and retrieval was done using data arrays.

3.2.6.2 Results. Proper operation of the following storage module actions was verified:

- reading and writing to an analog list;
- reading and writing to a discrete list;
- reading and writing to a specific signal;
- accessing a particular row or column;
- clearing an array by turning on the reset terminal;
- converting discrete to analog and analog to discrete; and
- indicating errors 1, 2, 3, 4, and 7.

3.2.7 Logger Module

3.2.7.1 Procedure. A task was created to transmit the values of one analog signal list to a serial port using the logger module. The serial port was connected to a personal computer running terminal emulation software to monitor the port output.

3.2.7.2 Results. No information was transmitted to the port. The logger module status terminal indicated "unexpected I/O failure" during the test. After further testing and talking with a BBI applications engineer, we concluded the problem was due to an error in the early version of the controller firmware installed in our controller. BBI agreed to supply new PROMs to correct the problem, but the new PROMs had not arrived by the time the tests were concluded.

3.3 PERFORMANCE COMPARISONS

The DPC 3330, RDC 3350, and UCS 3380 are all based on a 6-MHz 80186-type CPU chip. With similar processors and the same clock rate, task execution speed would be expected to be about the same for all three controllers. Two tests were performed to verify the similarity of execution speeds of the DPC 3330 and RDC 3350 controllers. Since the UCS 3380 and RDC 3350 processor boards are very similar, a separate comparison using the UCS 3380 was not performed. The DPC 3330 is designed to accept a 12-MHz processor chip and a math coprocessor at a future time. These two enhancements should greatly increase the task execution rate of the DPC 3330, particularly for math-intensive tasks.

3.3.1 Procedure

The first task was designed to compare the basic I/O speed of the two controllers. It performed the following steps 10 times for each task execution:

- read 8 analog inputs,
- read 8 digital inputs,
- equated 2 analog output variables to the first 2 analog input variables,
- equated 8 digital output signals to the 8 digital input signals,
- loaded 2 analog outputs, and
- loaded 8 digital outputs.

The second load read two analog input channels that provided inputs to PID modules. The error outputs of the PID modules were then wired to analog output channels. The inputs were read, the PID calculations performed, and the outputs set 10 times for each task execution.

The two tasks were configured with AIC 4.0 for both the RDC 3350 and the DPC 3330. The system tool kit was used to measure the task execution rates.

3.3.2 Results

The measured execution times for both tasks on both controllers are shown in Table 12. As expected, the execution time is about the same on the RDC 3330 and the DPC 3350, with the DPC 3330 having a small performance edge.

Table 12. Task execution times
for speed comparisons

Task	3330 Time (s)	3350 Time (s)
I/O test	0.430	0.520
PID loops	0.375	0.425

4. OBSERVATIONS

4.1 PHYSICAL CONSTRUCTION

The overall construction of the DPC 3330 is about the same as that of a good personal computer. Most electrical connections in the controller are made using printed circuit edge connectors. The DPC 3330 has several features that should improve its reliability relative to the model RDC 3350:

- lower power consumption,
- only one cable used in the system, and
- greater use of VLSI for a lower component count.

The I/O board support and cover appear to have slight deficiencies in the physical design. The lower row of I/O cards is basically supported by edge connector friction only, with the cover possibly providing some support. When the unit is installed, care should be taken to route I/O wiring such that this wiring will not place downward force on the I/O modules; that position could cause them to work loose. The plastic covers are held in place by tabs that snap into the base. While working with this unit, two of the tabs broke. A Bristol Babcock representative has stated that the cover attachment has been redesigned to fix this problem.

All I/O wiring is made to "pluggable" terminal strips that allow quick I/O module or controller replacement. Since some failures may require field replacement of the entire unit, the field wiring should be installed to allow easy replacement of the complete controller. It should be possible to replace the entire controller in a typical installation in about 30 min.

The controller modules do not have identification numbers that indicate type and options. Checking component values with factory telephone support was required to determine the filter time constants for the DI module. If not corrected, this shortcoming could be a maintenance and startup problem.

4.2 DOCUMENTATION

The DPC 3330 user manual received with the controller was a preliminary issue. While overall the manual is quite good, the following three errors concerning switch settings and setup were found:

1. On pages 3E-6 and 3E-7, the 1- to 5-V/4- to 20-mA switch settings are the same for both modes of operation.
2. On page 3B-4, the wrong switch setting is shown for selecting whether or not the numeric processor (NP) chip is installed.

3. On page 3C-3, the communications board switch settings are unclear. The AIC user and reference manuals for version 4.0 are updated versions of previous manuals and now include the DPC 3330 controller and DOS- based software.

4.3 COMMUNICATIONS

The controller tested only supported asynchronous communications at a maximum data rate of 9600 bytes/s. This unit could be configured to communicate with a VAX host by connecting an asynchronous port on this unit to a port on a CFE 3385, UCS 3380, RDC 3350, or another DPC 3330 connected to the host. Several slave DPC 3330s can be connected to one port on a higher level in a multidrop configuration. Enhancements are planned for release in 1989 by BBI to allow asynchronous communications at rates up to 57.6 kbytes/s and synchronous communications at rates up to 187.5 kbytes/s using the RS-485 ports. Enhancement is planned for the DPC 3330, RDC 3350, UCS 3380 and CFE 3385. The DPC 3330 cannot connect directly to the Bristol Data Highway.

5. CONCLUSIONS

Results of our tests indicate that the performance of the DPC 3330 is acceptable and that both the hardware and software are suitable for application as a stand-alone controller. While no tests were performed using the DPC 3330 in a distributed network, it is expected that this controller would work equally well in that application.

When compared with other, more expensive, Bristol Babcock control systems, Model DPC 3330 is a very cost-effective small-size alternative. The disadvantages of the DPC 3330 compared to the RDC 3350 or UCS 3380 are:

- smaller I/O point capacity,
- lower network communication rate (currently),
- no manual panel capability, and
- no redundancy option available.

The advantages of the DPC 3330 compared to the RDC 3350 and UCS 3380 are:

- lower power consumption,
- flexible I/O configurations,
- low cost, and
- small size.

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