

OAK RIDGE NATIONAL LABORATORY LIBRARIES
3 4456 0549644 2

CENTRAL RESEARCH LIBRARY
DOCUMENT COLLECTION



OAK RIDGE NATIONAL LABORATORY
operated by
UNION CARBIDE CORPORATION
NUCLEAR DIVISION
for the
U.S. ATOMIC ENERGY COMMISSION



ORNL - TM - 1638
Part 12
COPY NO. - 66

DATE - September 19, 1967

NUCLEAR INSTRUMENT MODULE MAINTENANCE MANUAL

PART 12

OR GATE, ORNL MODEL Q-2612

J. L. Anderson

ABSTRACT

The circuit, application, maintenance procedures, and acceptance tests for a multiple input logical OR Gate are described. The circuit is constructed in a "1-unit" module of the ORNL Modular Reactor Instrumentation series Q-2600, and is intended for use in safety systems of reactors employing this series of instruments.

OAK RIDGE NATIONAL LABORATORY
CENTRAL RESEARCH LIBRARY
DOCUMENT COLLECTION
LIBRARY LOAN COPY
DO NOT TRANSFER TO ANOTHER PERSON
If you wish someone else to see this document, send its name with document and the library will arrange a loan.

NOTICE This document contains information of a preliminary nature and was prepared primarily for internal use of the Oak Ridge National Laboratory. It is subject to revision or correction and therefore does not represent a final report.

LEGAL NOTICE

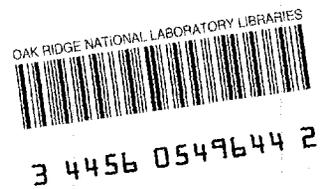
This report was prepared as an account of Government sponsored work. Neither the United States, nor the Commission, nor any person acting on behalf of the Commission:

- A. Makes any warranty or representation, expressed or implied, with respect to the accuracy, completeness, or usefulness of the information contained in this report, or that the use of any information, apparatus, method, or process disclosed in this report may not infringe privately owned rights; or
- B. Assumes any liabilities with respect to the use of, or for damages resulting from the use of any information, apparatus, method, or process disclosed in this report.

As used in the above, "person acting on behalf of the Commission" includes any employee or contractor of the Commission, or employee of such contractor, to the extent that such employee or contractor of the Commission, or employee of such contractor prepares, disseminates, or provides access to, any information pursuant to his employment or contract with the Commission, or his employment with such contractor.

CONTENTS

	Page
1. DESCRIPTION	4
1.1 General	4
1.2 Construction	4
1.3 Application	4
1.4 Specifications	4
1.5 Applicable Drawings	5
2. THEORY OF OPERATION	6
2.1 General	6
2.2 Circuit Description	6
3. OPERATING INSTRUCTIONS	9
3.1 Installation	9
3.2 Operating Controls	9
3.3 Connections	9
4. MAINTENANCE INSTRUCTIONS	9
4.1 General	9
4.2 Periodic Maintenance	9
4.3 Calibration	9
4.4 Troubleshooting	10
5. REPLACEABLE PARTS LIST	10
6. ACCEPTANCE TEST PROCEDURE	10
6.1 Test Equipment	10
6.2 Acceptance Test	11



1. DESCRIPTION

1.1 General

The OR Gate circuit is a logic element intended for use in the safety systems of nuclear reactors. The circuit accepts up to eight logic or bistate input signals, each of which is either "normal" (-10 v) or "trip" (0 v). The output is "normal" (-10 v) only if all eight of the inputs are normal. If any one or more of the input signals is in the "trip" state, then the output is also in the "trip" (0 v) state.

1.2 Construction

The OR Gate is constructed in a single module 1.40 in. wide, 4.72 in. high, and 11.90 in. deep. It is a standard "1-unit" plug-in module of the ORNL Modular Reactor Instrumentation series depicted on ORNL Drawings Q-2600-1 through Q-2600-6.

The circuit is constructed on a printed circuit board mounted within the module and is unshielded.

1.3 Application

The OR Gate is used in reactor safety systems to combine the several information signals of a safety channel into a single action output where it is desired to cause safety action when any one or more of the several signals is in the "abnormal," or "trip," state. The circuit is designed to accept only logic level signals, that is, -10 ± 2 v corresponding to the "normal" level and 0 ± 1.2 v corresponding to the "trip" level. In the usual application, the inputs to the OR Gate will come from the logic level outputs of Fast Trip Comparators, ORNL model Q-2609, in the information signal paths. The OR Gate output will normally drive a group of Magnet Control Amplifiers.

1.4 Specifications

1. Number of inputs: Eight,
2. Logic levels: Normal level is -10 ± 2 v and abnormal (trip) level is 0 ± 1.2 v.
3. Action: When all inputs are "normal," the output shall be "normal." When any one or more of the inputs is "abnormal," the

output shall be "abnormal." Open-circuited inputs are interpreted as "abnormal," and if any one or more inputs is open-circuit, the output shall be "abnormal."

Inputs should be bistable; consequently, response to intermediate voltage levels is undefined except that, in general, the output should be approximately equal to the least negative of the input signals.

- | | |
|-------------------------------|--|
| 4. Input impedance: | 5000 ohms resistive (each input). |
| 5. Maximum load: | 1000 ohms. |
| 6. Response time: | 50 μ sec maximum total time to change states. |
| 7. Power required: | -25 \pm 0.25 v dc with regulation of \pm 0.1%. |
| 8. Ambient temperature range: | 0 to 55°C. |

1.5 Applicable Drawings

The following list gives the drawing numbers (ORNL Instrumentation and Controls Division drawing numbers) and subtitles and the fabrication specification number for the OR Gate:

- | | |
|-------------|----------------------------|
| 1. Q-2612-1 | Circuit. |
| 2. Q-2612-2 | Details. |
| 3. Q-2612-3 | Metalphoto Panel. |
| 4. Q-2612-4 | Printed Circuit Board. |
| 5. Q-2612-5 | Assembly. |
| 6. Q-2612-6 | Parts List. |
| 7. SF-239 | Fabrication Specification. |

The following list gives the drawing numbers and subtitles for the Plug-In Chassis System:

1. Q-2600-1	Assembly.
2. Q-2600-2	Details.
3. Q-2600-3	Details.
4. Q-2600-4	Details.
5. Q-2600-5	Details.
6. Q-2600-6	Module Extender Assembly and Details.

2. THEORY OF OPERATION

2.1 General

The OR Gate is a diode-transistor logic circuit designed to provide a trip signal to a group of magnet control amplifiers when any one or more of the eight information signal inputs is in an abnormal state. Each information signal has two possible states: either normal, -10 ± 2 v, or abnormal, 0 ± 1.2 v. The Fast Trip Comparator which normally supplies the input signal has a limited driving capability that, in turn, limits the minimum allowable input impedance of the OR Gate to 5000 ohms. The OR Gate output must drive a 1000-ohm load with the output at -10 ± 2 v. The output is 0 ± 1.2 v when any input signal is in a trip state. The rise time, or time required to change state, is less than 50 μ sec.

2.2 Circuit Description

The circuit diagram of the OR Gate is shown in Fig. 1. To simplify the circuit description, assume temporarily that there is no voltage drop across a forward-biased diode and no current flow through a reverse-biased diode. Now consider the circuit conditions with all eight inputs open-circuited. If we further assume that the base current of Q1 is negligible, then a simple voltage divider is formed by resistors R1 through R9, since diodes D9 through D24 are forward biased. Since R1 through R8 have equal resistance, the voltage at the base of Q1 can be represented by

$$V = \frac{\frac{1}{8} R1}{\frac{1}{8} R1 + R9} (-25 \text{ v})$$

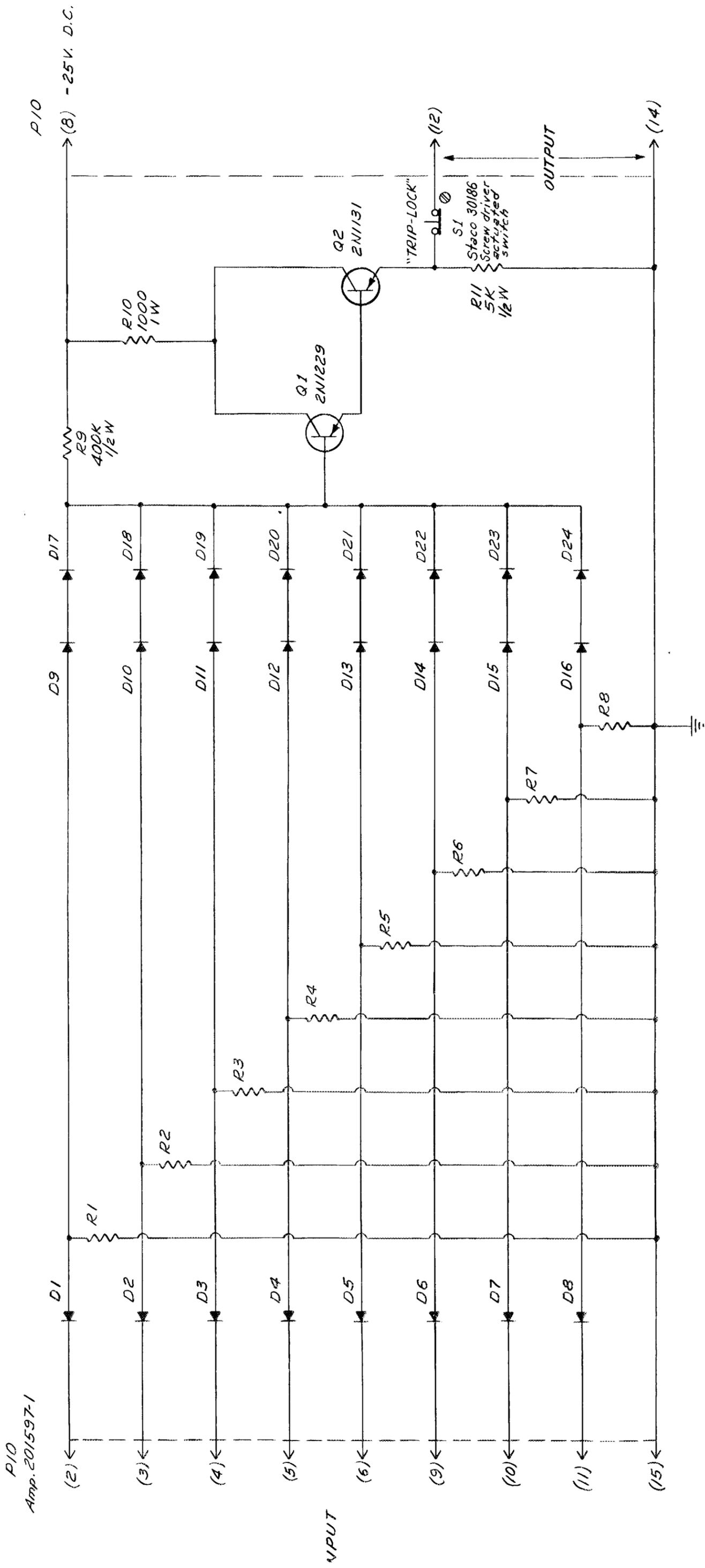


Fig. 1. "OR" Gate Circuit.

$$= \frac{\frac{5}{8}}{\frac{5}{8} + 400} (-25) = -0.04 \text{ v.}$$

If only one input (pin 2) is open-circuited, and the other seven inputs are held at -10 v , the voltage across each resistor R2 through R9 is -10 v , and diodes D10 through D16 and D18 through D24 are reverse biased. This leaves diodes D9 and D17 conducting, and the voltage at the base of Q1 becomes

$$V = \frac{R1}{R1 + R9} (-25)$$

$$= \frac{5}{5 + 400} (-25) = -0.31 \text{ v.}$$

Either of these voltages is well within the specified tolerance for nominal "zero" output. Q1 and Q2 are emitter followers to provide current gain and, ignoring base-emitter voltage drops, the output is equal to the voltage at the base of Q1. If the open input (pin 2) is grounded, D1 becomes reverse biased, and the output is unchanged from the open-circuit case. Any intermediate number of inputs at -10 v or 0 v will fall somewhere between the two cases calculated; thus, the condition that the output be $0 \pm 1.2 \text{ v}$ when any one or more of the inputs is in the zero state is accomplished.

When all eight inputs are held at -10 v , the base of Q1 and, consequently, the output are also -10 v . Note that, if all of the inputs are not equal, the output will be equal to (in general) the least negative of the signals. These arguments apply no matter which input or combination of inputs is selected, since all input circuits are essentially identical up to the base of Q1.

The diode and transistor voltage drops were neglected for the preceding description, but in fact, they are not negligible. Two diodes are placed in series in each input circuit (D9 and D17, for example) to compensate for the nearly equal, but opposite, base-emitter drops in Q1 and Q2. All diodes and transistors are silicon so that the junction drops will compensate each other and to minimize reverse leakage. The actual base current of Q1 is about $10 \mu\text{a}$ at the maximum specified output current, and has a negligible effect on the voltage levels.

Limiting-resistor R10 is included in the collector circuits of Q1 and Q2 to limit the current to a value that will not cause damage to the transistors when the output is accidentally short circuited.

A normally closed, screw driver actuated, locking pushbutton S1 is provided to open the output circuit for testing or for channel isolation.

3. OPERATING INSTRUCTIONS

3.1 Installation

The OR Gate is a module of the ORNL Modular Reactor Instrumentation series. Like the other modules in this series, it has standard connectors and dimensions and has a pin- and hole-code on the rear plate so that the module will not be inserted in a wrong location in a drawer. The module is installed by placing it in its proper location, inserting the module firmly, and tightening the thumb screw. The module may be plugged in with power on without damage.

3.2 Operating Controls

The only control on the module is a locking pushbutton on the front panel which, when depressed, causes the output to be zero or "tripped."

3.3 Connections

All connections are made through the rear connector P10 when the module is inserted.

4. MAINTENANCE INSTRUCTIONS

4.1 General

This module is designed to operate continuously with a minimum of maintenance and no adjustments. Should a failure occur, any part listed in the Replaceable Parts List, Sect. 5, can be replaced.

4.2 Periodic Maintenance

The OR Gate circuit will be tested routinely as a part of the overall safety tests; that is, the OR Gate must function properly if other tests of the system are to be successful. No specific maintenance procedures other than this testing are indicated.

4.3 Calibration

No calibration is required. Proper operation may be assured by performing an acceptance test (Sect. 6).

4.4 Troubleshooting

The most likely sources of trouble are either excessive leakage (I_{cbo}) of transistor Q1 or low current gain (H_{fe}) of both Q1 and Q2. Other possible troubles are faulty diodes, either shorted or open-circuit. Because some diodes are used two-in-series, an input-output test might not reveal a faulty diode. Diodes D9 through D24 should be checked individually with an ohmmeter. It should not be necessary to remove the diodes from the circuit to check them.

5. REPLACEABLE PARTS LIST

A description and an ORNL Stores number for all replaceable parts are given in Table 1.

Table 1. Replaceable Parts List

Part No.	ORNL Stores No.	Description
Q1	06-996-1840	Transistor, PNP, 2N1229, Hughes.
Q2	06-996-1710	Transistor, PNP, 2N1131, T.I.
D1 thru D24	06-995-5820	Diode, silicon, 1N457A.
D1 thru R8, R11	06-932-0133	Resistor, 5000 ohms $\pm 1\%$, 1/2 w, Stemag, type SLAK.
R9	06-932-0215	Resistor, 400 kilohms $\pm 1\%$, 1/2 w, Stemag, type SLAK.
R10	06-932-0587	Resistor, 1000 ohms $\pm 5\%$, 1 w, Stemag, type A-2.

6. ACCEPTANCE TEST PROCEDURE

6.1 Test Equipment

The following test equipment is required:

1. Regulated dc power supply, Hewlett-Packard 721 A, or equal
2. Two power supplies or volt-boxes, 0 to -10 v
3. DC voltmeter with $\pm 3\%$, or better, accuracy
4. Temperature test chamber.

6.2 Acceptance Test

1. Connect the power supply from pin 9 to pin 14 (ground) and adjust to -25 v. Connect all eight inputs (pins 2, 3, 4, 5, 6, 9, 10, and 11) to the volt-box adjusted to -10 v.
2. Measure the output voltage (pin 12). With all eight inputs at -10 v, the output should be -10 ± 2 v.
3. Disconnect one input (pin 2) and leave it floating. The output should be 0 ± 1.2 v. Ground the disconnected input. There should be no change.
4. Connect pin 2 to a second volt-box adjusted to -1.0 v. The output may increase slightly but still must be within 1.2 v of zero.
5. Repeat steps 3 and 4 for each of the inputs in turn, one at a time.
6. With all inputs connected to the volt-box, readjust the voltage to -8.0 v. The output may change somewhat, but it must be within -10 ± 2 v.
7. Connect a 1000-ohm load resistor to the output, and repeat steps 3 and 4 for at least 2 inputs, one at a time, and repeat step 6.
8. Place the OR Gate in a temperature test chamber and allow about 15 min for the module to reach an equilibrium temperature of 60°C . Repeat all tests at this temperature.
9. Depress the "Trip" pushbutton on the front panel. The output should drop to zero.

INTERNAL DISTRIBUTION

- | | | | |
|--------|------------------|--------|--|
| 1-20. | J. L. Anderson | 52. | G. R. Owens |
| 21. | D. S. Asquith | 53. | R. W. Peelle |
| 22. | A.E.G. Bates | 54-56. | W. Ragan |
| 23. | C. J. Borkowski | 57. | J. L. Redford |
| 24-33. | W. D. Brown | 58. | P. Rubel |
| 34-35. | C. T. Carney | 59. | J. B. Ruble |
| 36-38. | O. C. Cole | 60. | G. S. Sadowski |
| 39. | C. C. Courtney | 61-62. | R. W. Tucker |
| 40. | R. A. Dandl | 63. | D. D. Walker |
| 41. | J. T. De Lorenzo | 64. | K. W. West |
| 42. | E. P. Epler | 65. | H. N. Wilson |
| 43. | C. S. Harrill | 66-67. | Central Research Library |
| 44. | C. F. Holloway | 68. | Document Reference Section |
| 45. | G. A. Holt | 69-73. | Laboratory Records Department |
| 46. | W. H. Jordan | 74. | Laboratory Records, ORNL R.C. |
| 47. | W. E. Lingar | 75. | ORNL Patent Office |
| 48. | C. E. Mathews | 76-90. | Division of Technical Information
Extension |
| 49. | T. L. McLean | 91. | Laboratory and University Division,
ORO |
| 50. | R. V. McCord | | |
| 51. | L. C. Oakes | | |

EXTERNAL DISTRIBUTION

92. E. H. Cooke--Yarborough, Electronics Division, AERE, Harwell, England
93. J. B. H. Kuper, Brookhaven National Laboratory
94. E. Siddall, AECL, Chalk River, Ontario